Errata

Title & Document Type: 8112A 50 MHz Programmable Pulse Generator Operating and Service Manual

Manual Part Number: 08112-90004

Revision Date: 1992-01-01

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

Operating, Programming and Servicing Manual

HP 8112A 50 MHz Programmable Pulse Generator

SERIAL NUMBERS

This manual applies directly to instruments with serial number 3205G010006 and below.
If your instrument has a higher serial number, refer to Appendix C *Updating* which contains manual changes for later instruments. Be sure to examine this supplement for changes which apply to your instrument, and record these changes in the manual.

HP Part No. 08112-90004
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E0192

Notice

Subject Matter Notice

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Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date on the title page and back cover of the manual only changes when a new edition is published. When an edition is reprinted, all the prior updates to the edition are incorporated. No information is incorporated into a new edition unless it appears in a prior update.

Edition	Print Date	Manual Part No.	
1	February 1984	08112-90002	E0284
1	January 1992	08112-90004	E0192

Safety

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions and warnings in this manual must be heeded.

Preface

Introduction

This manual describes the following procedures for the HP 8112A 50MHz Programmable Pulse Generator:

- Installation
- Operation
- Programming
- Performance Test
- Adjustment
- Service

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards

[redacted]

facility, and to the calibration facilities of other International Standards Organization members.

Warranty

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, HP will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. The Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, software, or firmware will be

Exclusive Remedies

The remedies provided herein are the Buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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Introduction

General

This manual describes the following procedures for the HP 8112A 50 MHz Programmable Pulse Generator:

- Installation
- Operating
- Programming
- Testing Performance
- Adjustment
- Servicing

A Microfiche version of this manual is available on 4×6 inch microfilm transparencies (refer to title page for order number). The microfiche package also includes the latest Manual Changes supplement and all relevant Service Notes.

Instruments Covered by This Manual

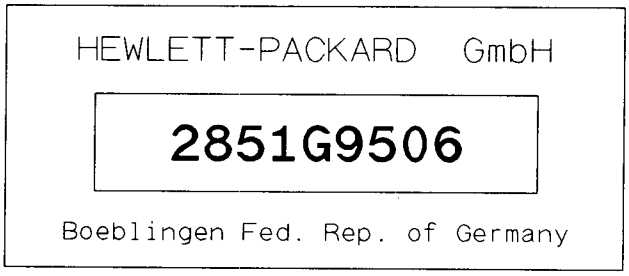


Figure 1-1. Serial Number Plate (FRG)

Attached to the rear of the instrument is a serial number plate (Figure 1-1). The first four digits only change when there is a significant modification to the instrument, the last five digits are assigned sequentially to instruments. *This manual applies directly to the instruments with the serial numbers quoted on the title page.* For instruments with higher serial numbers, refer to the Manual Change sheets in Appendix C *Updating*. To keep this manual up-to-date, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement by quoting the part-number and print-date of this manual, both of which appear on the title page.

Instrument Description

The HP 8112A Programmable Pulse Generator operates over the frequency range 1 Hz to 50 MHz with a maximum 32 V peak-to-peak output signal delivered into a 50 Ω/high impedance load. Instrument capabilities include:

- Fixed 5 ns transition times.
- 6.5 ns to 95 ms variable rise and fall times.
- Variable delay in all modes
- High and Low Level Limit for device under test (DUT) protection.
- HP-IB programmable.
- Easily accessible memory for up to 9 sets of mode and parameter selections.

The self-prompting operation and HP-IB programmability of the HP 8112A ensure that it is quick and easy to use in stand-alone and automatic-test applications. Self-test and fault diagnosis are performed each time the instrument is switched on. Error recognition (and prompt) helps the operator to recover from incorrect front panel or programming operation.

Note

Throughout this manual, instrument keys are shown as [Key] in the text. "Key" is the key name which appears above the key on the instrument front panel.

HP 8112A Options

Opt 910 Option 910 is an extra Operating and Service Manual.

Opt W30 Extended Repair Service for the instrument.

Accessories

Included

The HP 8112A is supplied complete with the following:

Item	HP Part Number
750 mA fuse for 220/240 V operation	2110-0813
or	
1.5 A fuse for 100/120 V operation	2110-0043
and	
Power cable	See Chapter 3 *Installation*

Available

The following accessories are available for the HP 8112A:

Item	HP Part Number
Carrying handle (Bail Handle Kit)	HP 5062-4001
Rack mount kit (single HP8112A)	HP 5062-3972
Rack mount kit (Two instruments)	HP 5062-3974
Lock Link kit for use with HP 5062-3974	HP 5062-3994

Recommended Test Equipment

The recommended test equipment and accessories required to maintain the HP 8112A, are listed in Table 1-1. Alternative equipment may be substituted, provided that it meets or exceeds the critical specifications given in the tables.

Table 1-1. Recommended Test Equipment

Instrument	Recommended Model	Required Characteristics	Alternative	Use*
Counter	HP 5335A with OPT 040	50 MHz, Start/Stop, TI, A to B	HP5345A	P, A
Digital Voltmeter	HP 3458A	DC 0.01 V–50 V, .004% acc. Pulse amplitude facility	HP 3456A HP 3478	P, A, T P,A,T
Function Generator	HP 8116A	20 MHz, THD $\leq$.1%	HP3324A #002	P, A
Digitizing Scope	HP 5412xT	>10 GHz Bandwidth <30 ps Transition times Flatness = 5%	HP 54100D	P, A
or	HP 5450A	< 100 MHz , 50Ω inputs		P, A
Signature Analyzer	HP 5005B			T
Power Supply	HP 6237B	0 - 20 V	HP 3324A	P, A, T
Attenuator	HP 33340C	20 dB, 2W		P, A, T
Adaptor		SMA to BNC		P, A, T
Terminators	HP 11048C HP 10100C	10 W, 50 Ω, ±0.1 % 2 W, 50 Ω		P, A T

* P = Performance Test; A = Adjustments; T = Troubleshooting

2

Specifications

Introduction

All specifications in the following sections describe the warranted performance of the instrument:

- Timing parameters
- Output parameters
- Waveform characteristics

All specifications apply with a 50 Ω load, after a 30 minute warm-up period, and are valid for ambient temperature in the range 15°C to 35°C. Refer to the General Characteristics section of this chapter for the performance derating factor to be used outside this temperature range (within the specified operating range of 0°C to 55°C) .

All operating characteristics given in the following sections describe typical performance figures which are non-warranted:

- Trigger modes
- Control modes
- Output Modes
- Inputs and Outputs
- Additional features
- General characteristics

Timing Parameters

Common Specifications

Unless otherwise stated, specifications are quoted for 50% amplitude in normal mode, fastest transitions.

Resolution

3 digits, best case 100 ps

Accuracy

± 5% of programmed value ±2 ns

Repeatability

Factor 4 better than accuracy

Jitter

max 0.2% of programmed value +100 ps

Period (PER)

Range

20.0 ns to 950 ms

Delay (DEL) (after Trigger Out)

Range

75.0 ns to 950 ms (max:PER+55 ns)

Accuracy

±5% of programmed value ±5 ns

Double Pulse (DBL) (interval between leading edges)

Range

20.0 ns to 950 ms (max:PER–WID)
DEL and DBL are mutually exclusive

Pulse Width (WID)

Range

10.0 ns to 950 ms (max: PER–10 ns)

Duty Cycle (DTY)

Range

1% to 99%, subject to Width specification

Resolution

1

Accuracy

±10% of programmed number
WID and DTY are mutually exclusive

Linear Transitions (between 10% and 90% amplitude)

Range

6.5 ns to 95 ms, leading edge (LEE) and trailing edge (TRE) independantly programmable within 1:20 ratio

Note

Delay, Width, and Transitions are under-programmable to ensure that the specified minimum values can always be obtained.

Output Parameters

Note Output voltages are specified for a 50 Ω load. Output voltages double when driving a high impedance load.

High Level (HIL) −7.90 V to +8.00 V

Low Level (LOL) −8.00 V to +7.90 V

Resolution

3 digits (10 mV)

Level accuracy

±1% of programmed value ±3% of amplitude ±40 mV

Repeatability

factor 4 better than accuracy

Settling time

100 ns +LEE

Preshoot, Overshoot, Ringing

±5% ±10 mV (variable transitions)
± 10% ±10 mV (fixed transitions)

Operating Characteristics

The following sections give non-warranted information on the typical operating characteristics of the instrument:

- Trigger modes
- Control modes
- Output modes
- Inputs and Outputs
- Additional features
- General characteristics

Trigger Modes

The external trigger signal referred to in this section is applied to the **EXT INPUT** BNC connector on the instrument front panel. The trigger level and sense are adjustable. An external trigger can be simulated by pressing the [MAN] key.

The [1 PULSE] key gives an additional pulse in Gate and External Burst modes.

Normal A continuous pulse train is generated.

Trigger Each active input edge triggers a single pulse (or double pulse if DBL is selected)

Gate Active input level enables pulse train, last pulse always complete. Width and period of first pulse may deviate 10% from subsequent pulses.

External Width Pulse recovery, input edges toggle output.

External Burst Each active input edge triggers a burst of pulses [BUR] (1 to 1999 pulses). Width and period of first pulse may deviate 10% from subsequent pulses.

Control Modes

An external control signal applied to the **CTRL INPUT** BNC connector can be used to modulate the output signal.

Period, Delay, Double pulse and Width Control 1 V to 10 V voltage at Cntrl Input varies the selected parameter over one decade. Eight non-overlapping decades cover the range specified under "Timing Parameters". Display shows max value available in selected range.

High-level Control −8 V to +8 V input varies HIL over the same range irrespective of LOL.

Settling time (within 5% of final value)

200 μs

Output Modes

Complement	Selectable on/off
Disable	Disconnects output, default at switching on.
Limit	Implements present output levels as output limits.
Fixed transitions	5 ns from 10% and 90% amplitude, 3.5 ns from 20% to 80% amplitude
Cosine transitions	Up to 25% faster between 10% and 90% of amplitude than linear transitions
Linear transitions	±3% linearity

Inputs and Outputs

External Input	**Threshold level**	±10 V adjustable
	Minimum amplitude	500 mV (p-p)
	Maximum Input voltage	±20 V
	Minimum pulse width	10 ns
	Input impedance	10 kΩ
	Trig slope	off, pos, neg, both (Trigger and Ext Width only)
Control Input	**Bandwidth**	1 kHz
	Input voltage limits	±20 V
	Input impedance	10 kΩ
Trigger Output	**High level**	+2.4 V into 50 Ω +4.8 V into high impedance
	Low level	0 V
	Duty cycle	50%
	Output impedance	50 Ω
	Propagation Delay (EXT INPUT to TRIG OUTPUT)	25 ns

	External voltage limits	−0 V, +5 V
Main Output	**Amplitude**	100 mV to 16 V (200 mV to 32 V) pp
	Reflections	< 10%
	Source Impedance	50 Ω
	Short circuit capability	Maximum peak current 150 mA for up to 1 hour (15°C to 35°C)
	External voltage limits	±5 V

Additional Features

Set Sets up square wave, delay min. LEE, TRE=10% PER or fixed

Non-Volatile Memory

Power down location	saves current settings
9 programmable locations	each stores a complete setup
Standard settings location	100 μs, 1 V pulse at 1 kHz

Self-test The instrument performs a self-test when switched on, and by HP-IB command.

Error detection Visual and Status Byte indication of incompatible settings, under-range control voltage, and clipped amplitude (excessive transition time).

HP-IB Capability The HP 8112A is fully programmable except for the External Input trigger level.

Capability codes SH1, AH1, T6, L4, SR1, RL1, PP0, DC1, DT1, C0

Learn modes All or individual parameters can be programmmed and uploaded

Service request Initiated by syntax and operating errors, returns error number

Status byte Returns text of operating-error message

Message Times

Time to receive and execute a message

5 ms (Offset 30 ms)

Time to send a message

Status byte	15 ms
Learn string	1 ms per character, Status byte:15 ms

General Characteristics

Environmental

Storage temperature range	-40°C to 70°C
Operating temperature range	0°C to 55°C
Humidity range	Up to 95% RH between 0°C and 40°C

Power supply

- 100/120/220/240 V rms (selectable) +5%, -10%
- 48–440Hz
- 120 VA maximum

Weight

Net	5.9 kg (13 lbs)
Shipping	8.0 kg (18 lbs)

Dimensions

- 89 mm high (3.5 in)
- 213 mm wide (8.4 in)
- 445 mm deep (17.5 in)

Recalibration period 1 year recommended

3

Installation

Introduction

This chapter provides installation instructions for the HP 8112A. It also includes information about initial inspection and damage claims, preparation for use, packaging, storage and shipment.

Safety Considerations

The HP 8112A is a Safety Class 1 instrument (instrument with an exposed metal chassis that is directly connected to earth via the power supply cable).

Before operation review the instrument and manual, including the red safety page, for safety markings and instructions. These must then be followed to ensure safe operation and to maintain the instrument in safe condition.

Initial Inspection

Warning

To avoid hazardous electric shock, do not perform electrical tests when there are signs of shipping damage to any part of the outer covers or panels.

Inspect the shipping container for damage. If the container or cushioning material is damaged, keep it until the contents of the shipment have been checked for completeness and the instrument has been verified both mechanically and electrically.

The contents of the shipment should be as shown in the shipping document plus any accessories that were ordered with the instrument. Procedures for checking the operation of the instrument are given in Chapter 8 *Performance Tests*.

If the contents are incomplete, mechanical damage or defect is apparent, or if the instrument does not pass the operators checks, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without awaiting settlement.

Power Requirements and Line Voltage Selection

Caution

BEFORE APPLYING AC LINE POWER TO THE HP 8112A, ensure that the instrument is set to the local line voltage and the correct line fuse is installed in the fuse holder.

The instrument requires a power source of 100, 120, 220 or 240 V rms (+5%, -10%) at a frequency of 48–440 Hz single phase. The maximum power consumption is 120 VA.

The line voltage selector switches can be seen through the left hand side of the instrument cover towards the rear. The line voltage selector is set at the factory to the most commonly used line voltage for the country of destination. The instrument power fuse is located on the rear panel.

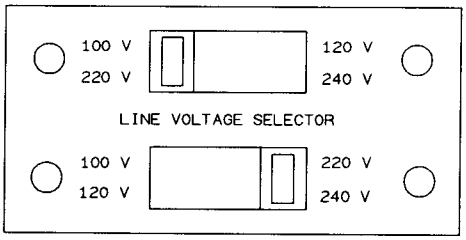


Figure 3-1. Line Voltage Selector Switches

Caution

Do not change the Line Voltage Selector switch settings with the instrument switched ON, or with power connected via the rear panel.

To change the selected line voltage:

1. Remove the power cord.
2. Remove the instrument top cover by releasing the captive securing screw at the rear, and sliding the cover off.
3. Using a screwdriver, move the switches to the required position for the voltage to be used.
4. Replace the instrument top cover.
5. Fit the correct power fuse for the selected operating voltage.

Table 3-1. Line Voltage and Fuse Selection

Line Voltage	Fuse Type	HP Part Number
100 V / 120 V	1.5 A	2110-0043
220 V / 240 V	750 mA	2110-0813

Power Cable

Warning

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:

- **If the instrument is to be energized via an auto transformer for voltage reduction, ensure that the Common terminal is connected to the grounded pole of the power source**
- **The power cable must only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.**
- **Before switching on the instrument, the protective ground terminal of the instrument must be connected to the protective conductor of the power cable. This is verified by using the power cord which is supplied with the instrument.**
- **Intentional interruption of the protective ground connection is prohibited.**

In accordance with international safety standards, the HP 8112A is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type of cable shipped with each instrument depends on the country of destination. Refer to Figure 3-2 for the part numbers of the available cables.

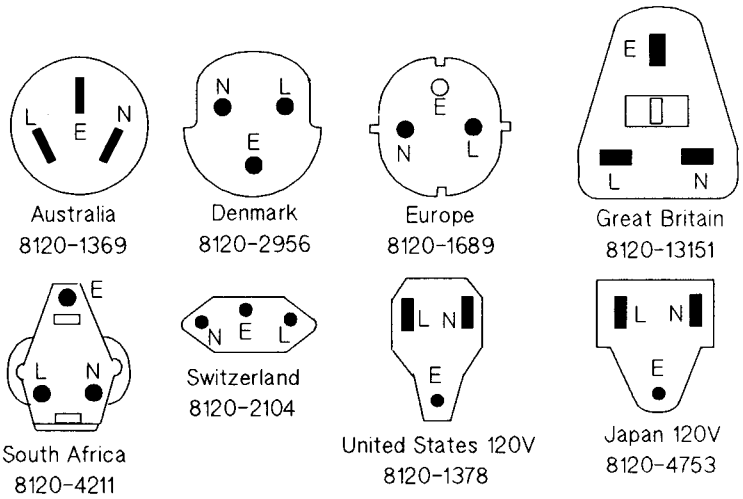


Figure 3-2. Power Cables & Plug Identification

The following work should be carried out by a qualified electrician - all local electrical codes being strictly observed. If the plug on the cable does not fit the power outlet, or the cable is to be attached to a terminal block, cut the cable at the plug end and re-wire it.

The color coding used in the cable will depend on the cable supplied. If a new plug is to be connected, it should meet local safety requirements and include the following features:

- Adequate load-carrying capacity (see specifications in Chapter 2).
- Ground connection.
- Cable clamp.

HP-IB Connector

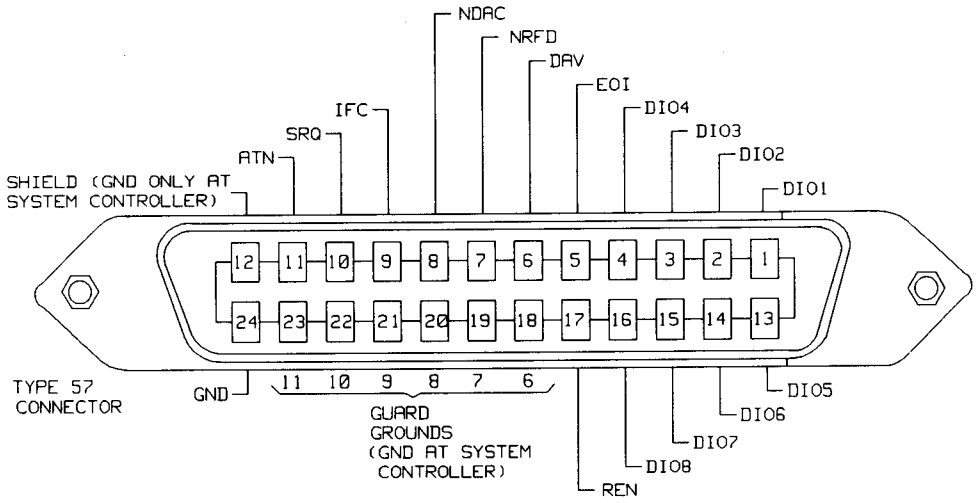


Figure 3-3. HB-IB Connector

The rear panel HP-IB connector (Figure 3-3), is compatible with the connector on Cable Assemblies 10833A, B, C and D. If a cable is to be locally manufactured, use male connector, HP part number 1251-0293.

HP-IB Logic Levels

The HP 8112A HP-IB lines use standard TTL logic, the levels being as follows:

- True = Low = digital ground or 0 Vdc to 0.4 Vdc,
- False = High = open or 2.5 Vdc to 5 Vdc.

All HP-IB lines have LOW assertion states. High states are held at 3.0 Vdc by pull-ups within the instrument. When a line functions as an input, approximately 3.2 mA of current is required to pull it low through a closure to digital ground. When a line functions as an output, it will sink up to 48 mA in the low state and approximately 0.6 mA in the high state.

Caution

The HP-IB line screens are not isolated from ground.

Operating Environment

Warning 

The HP 8112A is not designed for outdoor use. To prevent potential fire or shock hazard, do not expose the HP 8112A to rain or other excessive moisture.

Temperature The HP 8112A may be operated in temperatures from 0°C to 55°C.

Humidity The HP 8112A may be operated in environments with humidity up to 95% (0°C to +40°C). However, the HP 8112A should be protected from temperatures or temperature changes which cause condensation within the instrument.

Instrument Cooling

The HP 8112A is equipped with a cooling fan mounted inside the rear panel. The instrument should be mounted so that air can freely circulate through it. When operating the HP 8112A, choose a location that provides at least 75 mm (3 inches) of clearance at the rear, and at least 25 mm (1 inch) of clearance at each side. Failure to provide adequate air clearance will result in excessive internal temperature, reducing instrument reliability.

Claims and Repackaging

If physical damage is evident or if the instrument does not meet specification when received, notify the carrier and the nearest Hewlett-Packard Service Office. The Sales/Service Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

Storage and Shipment

The instrument can be stored or shipped at temperatures between −40°C and +75°C. The instrument should be protected from temperature extremes which may cause condensation within it.

Return Shipment to HP

If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing owner, return address, model number and full serial number and the type of service required.

The original shipping carton and packing material may be re-usable, but the Hewlett-Packard Sales/Service Office will also provide information and recommendations on materials to be used if the original packing is no longer available or reusable. General instructions for repacking are as follows:

1. Wrap instrument in heavy paper or plastic.
2. Use strong shipping container. A double wall carton made of 350-pound test material is adequate.
3. Use enough shock-absorbing material (3 to 4 inch layer) around all sides of the instrument to provide a firm cushion and prevent movement inside container. Protect control panel with cardboard.
4. Seal shipping container securely.
5. Mark shipping container FRAGILE to encourage careful handling.
6. In any correspondence, refer to instrument by model number and serial number.

4

Operating

Introduction

This chapter explains the use of all controls, indicators and connectors on the front and rear panels of the HP 8112A. Figure 4-1 and Figure 4-12 show the front and rear panel respectively. Each group of controls is explained in subsequent sections of this chapter under the following headings:

- Switching On
- Trigger Mode Selection
- External Trigger Controls
- Control Mode Selection
- Transition Mode Selection
- Parameter Selection
- Rear Panel

Examples are given in Chapter 5.

Before applying power to the HP 8112A:

1. Read the red Safety Summary sheet at the front of this manual.
2. Ensure the Line Voltage Selector switches are set properly for the power source to be used. Refer to Chapter 3 on instrument installation if necessary.

Caution

Do not change the Line Voltage Selector switches with the instrument switched on or with power connected to the rear panel.

3. Ensure that the device under test cannot be overdriven by the HP 8112A output (16 V p-p into 50 Ω; 32 V p-p into high impedance).
4. Ensure that the maximum external voltage applied to the HP 8112A falls within these limits: −5 V to +5 V dc).

Caution

Do not apply an external voltage greater than ±5 V, or electrostatic discharge to the output connector.

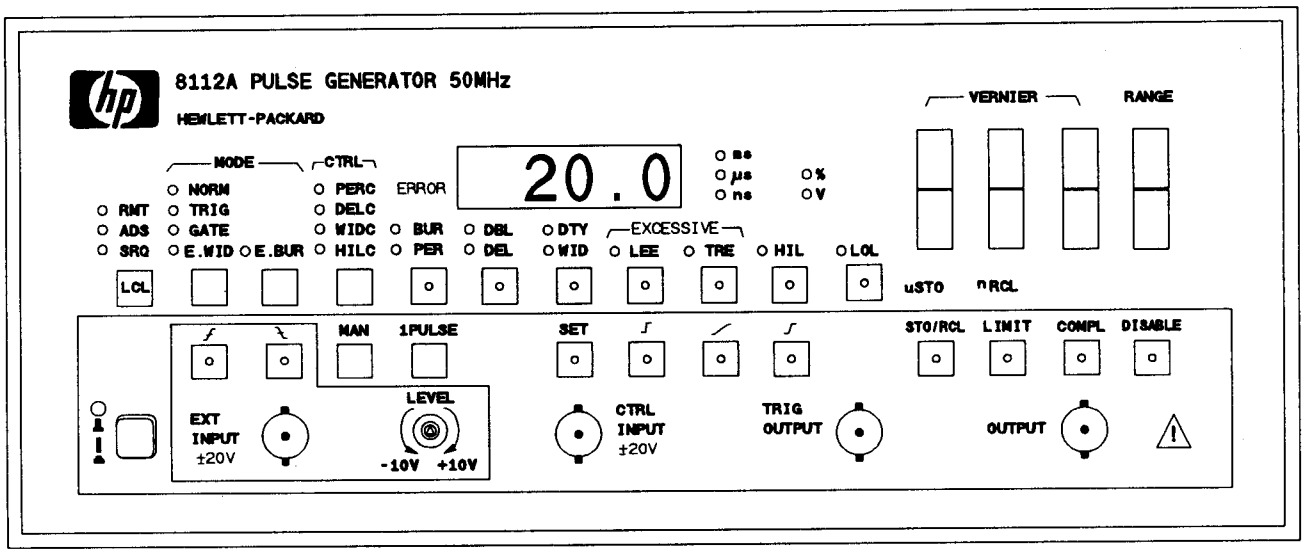


Figure 4-1. HP 8112A Front Panel

Switching On

The HP 8112A performs a "self test" when the power is switched on. All the front panel LEDs should light momentarily. If a fault is detected, the word "ERROR" is illuminated and an error code is displayed on the front panel digital display. The possible error codes are:

▢	A key is stuck in the depressed position.
E01	Fail RAM test
E11	Fail Period Timing test
E12	Fail Delay Timing test
E13	Fail Width Timing test
E14	Fail Slope Generation test

E21 Fail Output Amp +ve Offset test

E22 Fail Output Amp -ve Offset test

E31 to E39 Fail Overall tests

E41/42 The output amplifier is faulty.

E51 and 52 Fail Burst Counter tests

Refer to Chapter 10.1 *Troubleshooting* for more information on the error codes and their causes.

When the self-test is completed successfully, the instrument automatically assumes the operating state which was active when it was last switched off, except that the output is disabled to protect the unit under test. If the instrument battery has failed, the Standard Parameter Set is selected.

Standard Parameter Set

The Standard Parameter Set exists for two reasons:

- If the instrument RAM becomes corrupted due to battery failure, the Standard Parameter Set will be selected when the instrument is switched on to give an error free display.
- If an invalid combination of Operating and Control modes is selected, switching the instrument off and on again, or selecting RCL 0, will revert to the Standard Parameter Set. The Standard Parameter Set is detailed below.

Trigger mode	NORM	Normal
Control mode	CTRL	Off
Burst	BUR	0001 #
Period	PER	1.00 ms

Selecting Trigger Mode

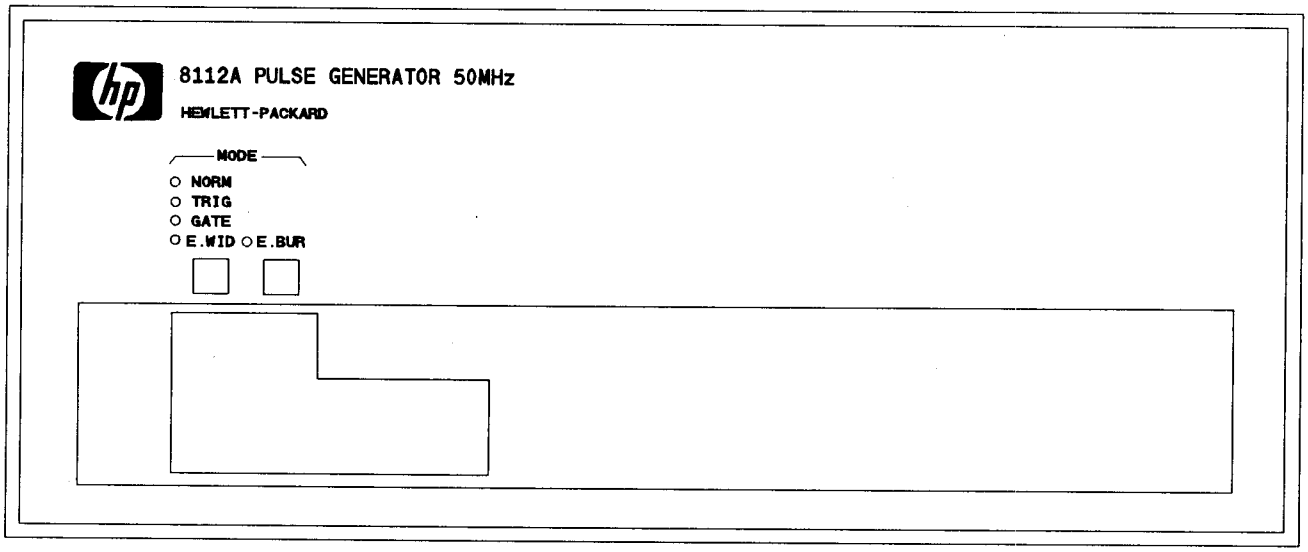


Figure 4-2. Trigger Mode Controls

Mode Selection

The currently active mode is shown by LED indicator. The trigger mode can be cycled through available options by pressing the key below the mode indicators.

The standard instrument offers the following trigger modes:

NORM In normal mode a continuous pulse stream is generated.

TRIG In trigger mode each active input edge triggers a single output cycle.

GATE In gate mode the active level of the external input signal enables output period. The first output cycle is synchronous with the active trigger slope. The last output cycle is always completed.

E.WID This mode can be used for recovery of external signal with selectable transition times and output levels.

E.BUR In external burst mode each active external trigger generates a pre-programmed number of pulses (1 to 1999). Minimum time between two bursts is 100 ns.

Controlling the External Trigger

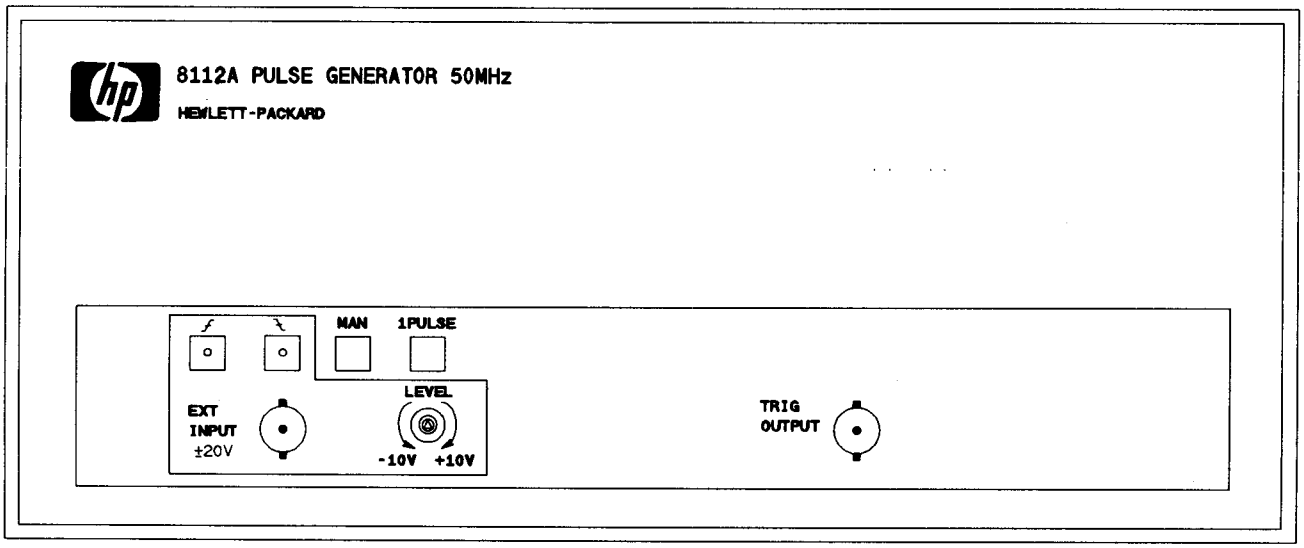


Figure 4-3. External Trigger Controls

The external trigger signal required in some trigger modes must be applied to the **EXT INPUT** BNC connector.

Caution

Do not apply voltages outside the range ±20 V to the EXT INPUT connector.

Trigger Slope

Select a positive or negative trigger slope by pressing the [⨍] or [⨍] key respectively. The current slope is indicated by the LED on the key.

The trigger can be switched off by pressing the currently active key again. Both key LEDs will then be off.

Trigger Level

Trigger level can be varied in the range ±10 V using the LEVEL adjuster.

Manual Trigger
[MAN]

This key can be used to simulate the external trigger signal.

Single Pulse
[1 PULSE]

This key initiates a single pulse in TRIG, GATE, and E.BUR modes.

Trigger Output

The trigger output provides a timing reference signal synchronised to the main output signal. Output levels are 0 and 2.4 V into 50 Ω. Delay from trigger input to trigger output is 25 ns.

Selecting Control Mode

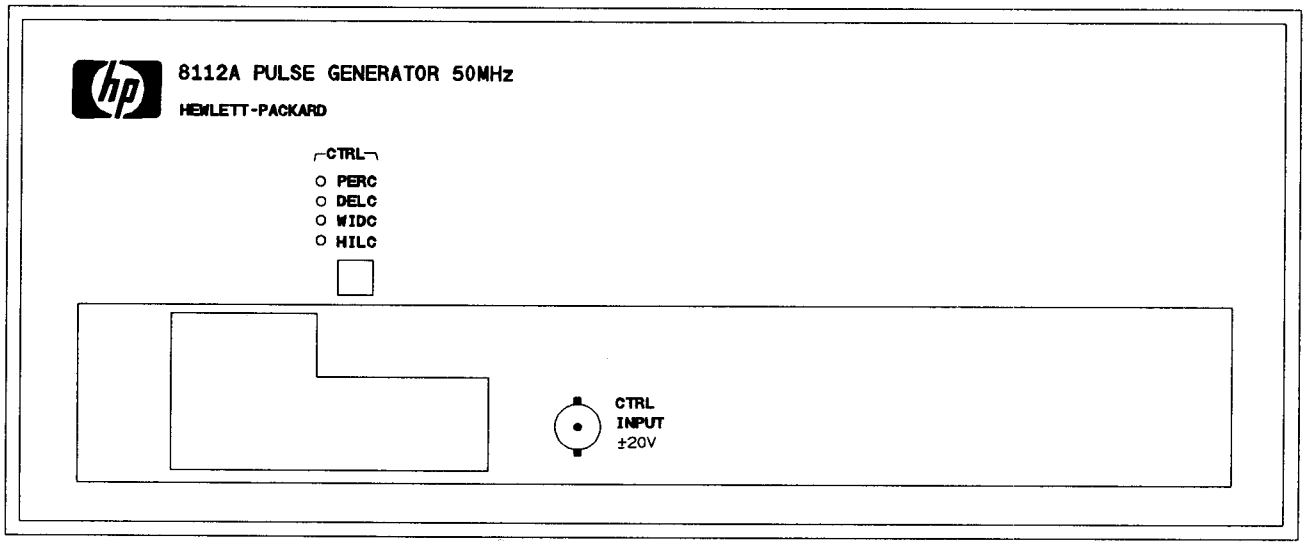


Figure 4-4. Control mode controls

Control Input

An analog signal can be applied to the control input to modulate or control the HP 8112A output signal. This external input may be any waveform in the range ±20 V. However, the overall range within which the instrument actually responds to a control signal, is 1.0 V to 10 V, as shown below.

Caution

Do not apply voltages outside the range ±20 V to the CTRL INPUT connector.

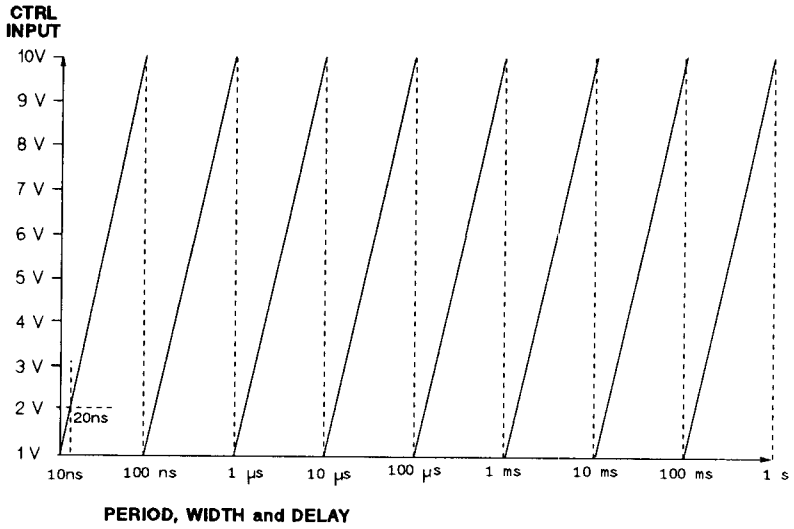


Figure 4-5. Relationship Between Control Input Voltage and Controlled Parameter

Mode Selection

Depending on the control mode selected, the output signal may be either Period, Delay, Width, or High Level controlled, by an external voltage applied to the CTRL INPUT.

The control mode can be cycled through available options by pressing the key below the mode indicators and the currently active mode is shown by an LED indicator. Table 4-1 indicates the permitted combinations of control and operating modes.

Table 4-1. Operating/Control Mode Combinations

CTRL	MODE				
	NORM	TRIG	GATE	EWID	EBUR
PERC	X		X		X
DELC	X	X	X		X
DBLC	X	X	X		X
WIDC	X	X	X		X
HILC	X	X	X	X	X

Period Control (PERC)

Control input sensitivity is +1.0 V to +10.0 V (+2.0 V to +10 V in the 20 ns to 100 ns range) and period ranges from 20 ns to 1 s are available in eight non-overlapping decades. See Figure 4-5.

The decade is selected by setting PER within that decade, i.e. PER=3 μs would mean than control input voltage cycling between 1 V and 10 V, will control the period between 1 μs and 10 μs. Whatever the value you select for PER, the upper limit for that decade is displayed (10 μs if 3 μs was selected as above). The vernier keys are inoperative and the Range key is used to change range.

Delay Control (DELC)

Control input sensitivity is +1.0 V to +10.0 V. Minimum delay is 75 ns and a maximum delay of 1 second is obtainable.

Note

In DBL mode the time **between** pulses will be varied by the control input, when DELC is selected.

See Figure 4-5.

Width Control (WIDC)

Control input sensitivity is +1.0 V to +10.0 V and width range 10 ns to 1 s in eight non-overlapping decades. See Figure 4-5.

High Level Control (HILC)

High Level control is available in the range −8.0 V to +8.0 V. It is important to note that while the Low Level (LOL) value can be set to a maximum of +7.95 V in 50 mV steps, the LIMIT facility

becomes non-operational in this Control mode, and the button LED will blink. See Figure 4-6.

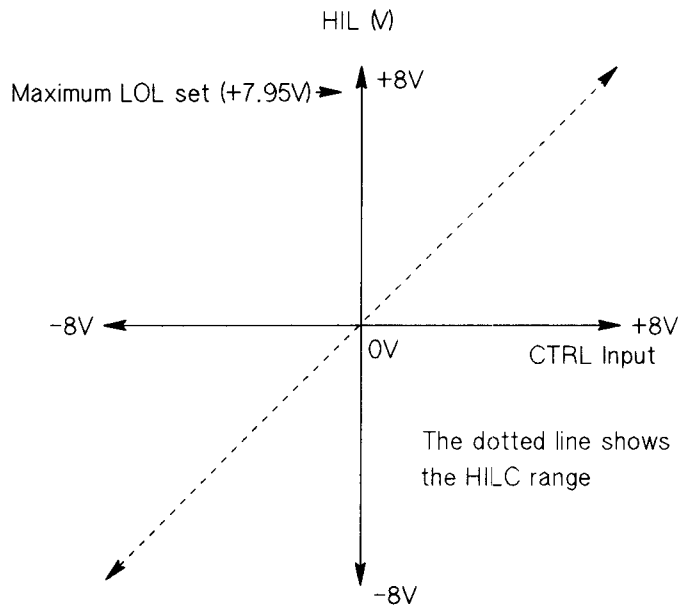


Figure 4-6. High Level Control Capabilities

Setting Transition Modes

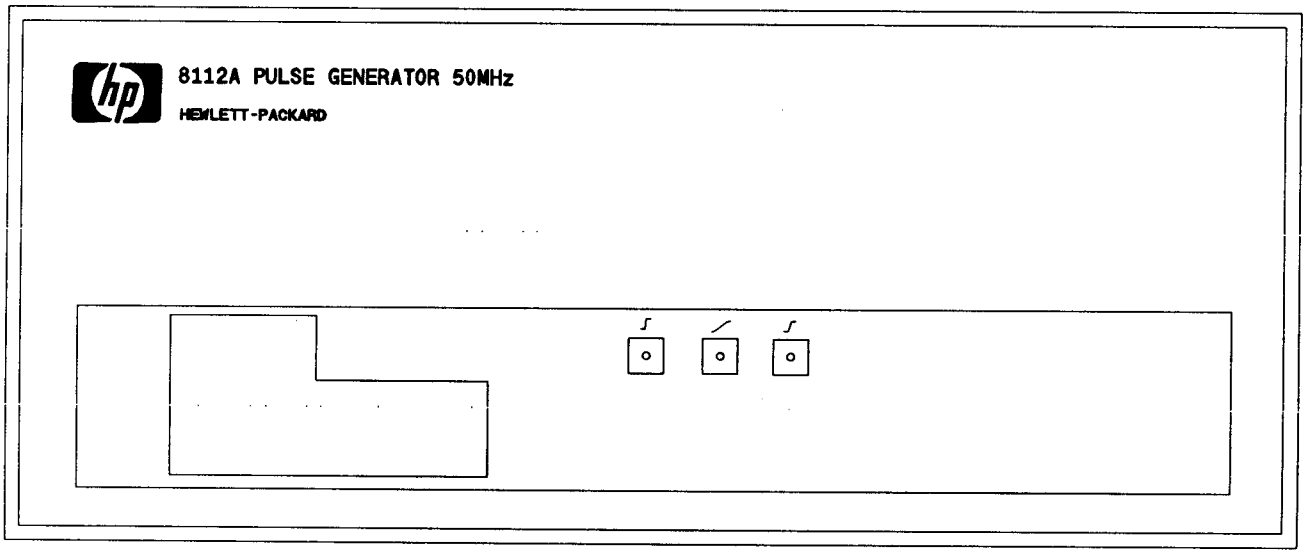


Figure 4-7. Transition Controls

The transition mode keys enable the operator to select the type of pulse transition and to vary transition time.

Fixed This key provides a fixed transition of 4.5 ns. You cannot adjust the LEE or TRE parameters when this key is operated (lit).

Linear Permits both the leading and trailing edges of the HP 8112A output pulse to be programmed independently of each other, in the range 6.5 ns to 95 ms, by setting values for LEE and TRE. Maximum permissible ratio is 1:20.

Gaussian This key is the same as the linear mode key except that edges are co-sinusoidal in shape. It is important to note that the actual rise and fall times of the transitions will be up to 25% faster than the selected and displayed value for slopes of greater than 50 ns duration. For slopes less than 50 ns, transition times tend increasingly towards the displayed value.

The reason for this variation is that selected values are based only upon times between 10% and 90% of total trigonometric transition. Values between 0 to 10% and 90% to 100% are not taken into account by the HP 8112A instrument.

Transition Ranges

There are seven overlapping ranges for linear and gauss transitions, and it is important to note the following:

- Within any range, the maximum ratio of the leading edge transition time to the trailing edge transition time is 1:20 and vice versa.
- When you move the currently active slope to higher or lower range than the non-active slope, the latter will be automatically pulled into the same range.

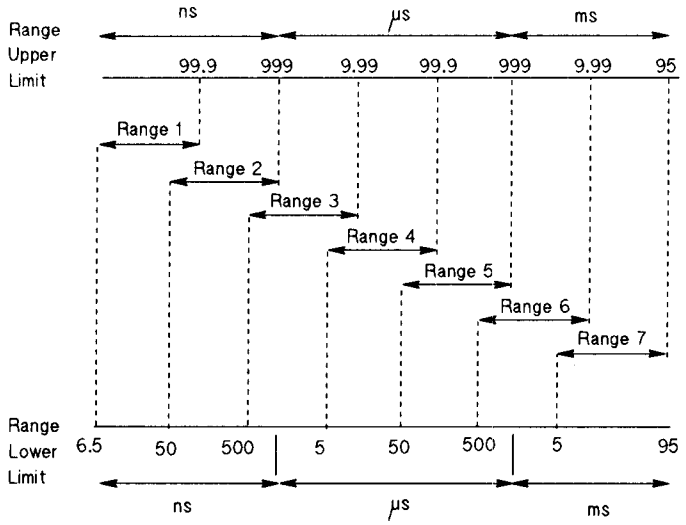


Figure 4-8. LEE and TRE ranges

Up and Down-ranging, Using the VERNIER keys

There is an overlap between all ranges.

When the currently active slope is altered so that it falls within a range above or below the non-active slope, the value of the non non-active slope automatically increases/decreases in value by a factor of 10 or 100, depending on where it lay within the overlap.

Figure 4-9, Table 4-2 and Table 4-3 illustrate the technique of passing Range "Break Points".

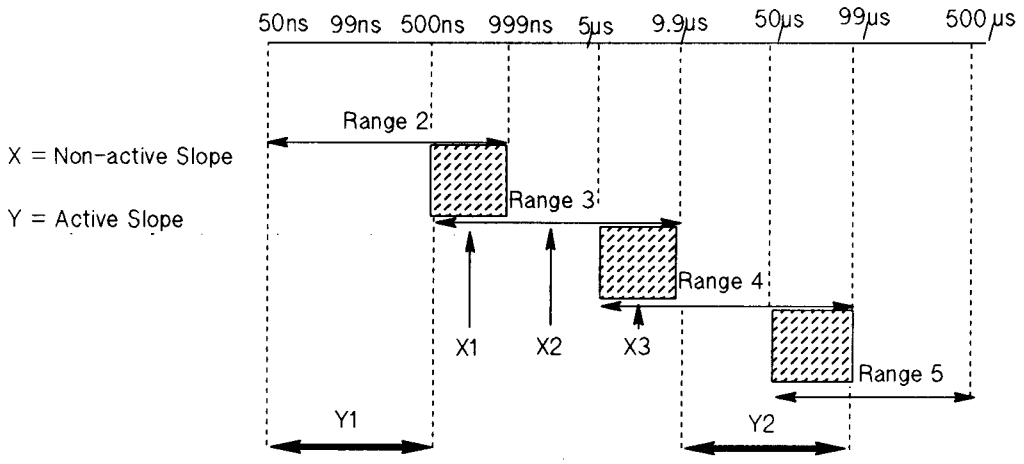


Figure 4-9. Ranging examples

Table 4-2.
Active slope moves from Range 3 to Range 2 (Y1)

Inactive slope	Change Value	Reason
X1	no change	in a shared overlap, range 2/3
X2	÷10	not in overlap
X3	÷10	in overlap with higher range (4)

Table 4-3.
Active slope moves from Range 3 to Range 4 (Y2)

Inactive slope	Change Value	Reason
X1	×100	in shared overlap
X2	×10	not in overlap
X3	no change	in overlap with higher range

Up and Down-ranging Using the RANGE key

When this key is used to move a currently active slope up or down a range, the non-active slope will be automatically pulled into the **Same Decade** as the active slope setting. This effect is particularly usefull for fast ranging between decades.

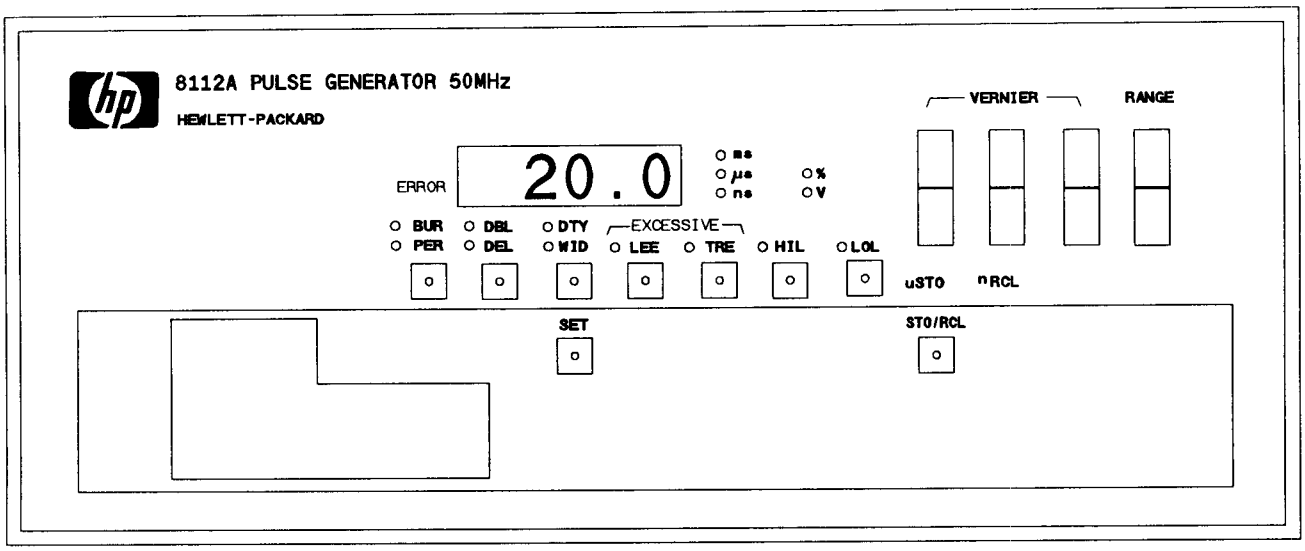


Figure 4-10. Parameter controls

The parameters available for selection depend on the currently selected modes. All parameters are described below.

Selection

Pressing a parameter key selects the parameter indicated by the illuminated mnemonic above the key.

The current value of the selected parameter is shown on the digital display. The parameter units are indicated by the LEDs to the right of the display.

Adjustment

The currently selected parameter is adjusted using the [VERNIER] and [RANGE] rocker keys. Each [VERNIER] key increments or decrements the corresponding digit in the digital display. Similarly, the [RANGE] key increases or decreases the parameter value by a factor of 10.

Period/Burst Key

[PER]

When selected, allows the period of the HP8112A output signal to be set and or adjusted.

[BUR]

In EBUR mode, this key is used to set the number of pulses (between 1 and 1999) which will comprise the burst.

Delay/Double Key

(DEL)

Enables the operator to set the desired delay between TRIG OUTPUT pulse and HP 8112A OUTPUT pulse.

(DBL)

When selected, double pulses are output, their characteristics being defined by the parameter settings. The width of each pulse is either equal to the WID setting or half the DTY setting. The range of delay between the two pulses is 20 ns to 950 ms.

Width/Duty Key

(WID)

Enables pulse width to be set between 10 ns and 950 ms.

(DTY)

Pulse duty cycle is variable from 1% to 99%. Percentage values are shown on the digital display.

Leading and Trailing edge Keys (LEE) (TRE)

These two keys are used in conjunction with TRANSITION MODE keys. It is possible to increase or decrease rise and fall times of output pulses. Should you select a rise or fall time which degrades the HIL or LOL settings, an *EXCESSIVE* message will illuminate above the two keys and the key associated with the incompatible parameter will flash.

High and Low level Keys (HIL) (LOL)

When either of these keys is selected, the corresponding level may be set.

Note 

The selected HIL value is inoperative in the HILC mode.

Set Key (SET)

This key causes the HP 8112A to assume a factory programmed parameter set as follows:

NORM	Active
PER	Active
WID	50% of PER
LEE	10% of PER
TRE	10% of PER

SET is automatically eliminated by selection of any other mode or parameter key or by pressing PER again.

Store and Recall Key

STO/RCL

The HP 8112A has the capability to store nine complete sets of mode and parameter information in it's memory.

To store settings, press STO/RCL. The digital display now reads ⊔⊓X, where X is the file identity number (1 to 9). The right hand vernier key is used to alter the value of X, to determine which file the parameter set will be stored as. Now press the bottom of the left hand vernier key and the current instrument settings will be stored in the selected file.

To recall settings, press STO/RCL. The digital display now reads ⊔⊓X, where X is the file identity number (1 to 9). The right hand vernier key is used to alter the value of X, to determine which parameter set file will be recalled. Now press the bottom of the center vernier key and the instrument settings will be altered to those of the stored file which has been selected.

Note

RCL 0 reverts the instrument to it's standard setting, see Chapter 2.

If no settings have been stored, the instrument will revert to standard settings whichever file number is selected for recall.

Selecting Output Mode

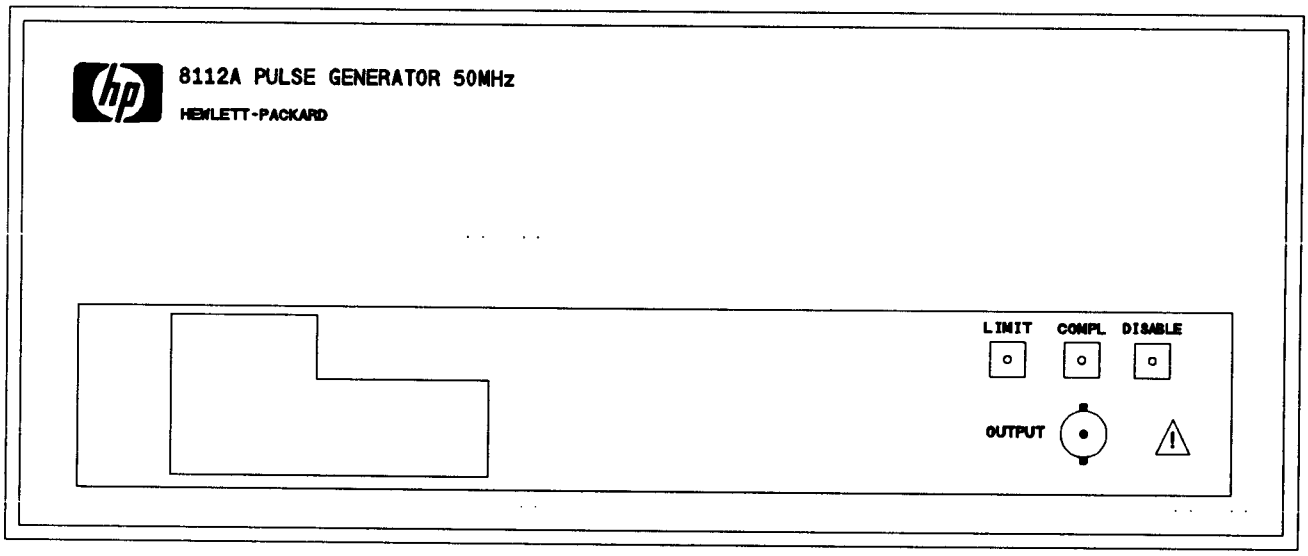


Figure 4-11. Output controls

Limited Output
LIMIT

Pressing the LIMIT key sets the current high and low output levels (HIL,LOL) as output limits which cannot be exceeded until limited output mode is switched off. While limited output mode is active, the high and low output levels (HIL,LOL) can be varied within the output limits.

Limited output mode is switched off by pressing the LIMIT key again.

The LIMIT key LED is lit when this mode is active.

Caution

Limit does not work when using HILC mode, the LIMIT key will flash if HILC is selected to remind you that it is no longer active.

Complement Output
COMPL

Pressing the COMPL key complements the instrument output, pressing the key again returns the instrument output to normal.

The COMPL key LED is lit when the output is complemented.

Disabled Output
DISABLE

Pressing the DISABLE key disables the instrument output, pressing the key again enables the output.

The DISABLE key LED is lit when the output is disabled.

Caution

Do not apply an external voltage greater than ±5 V, or electrostatic discharge to the output connector.

Rear Panel

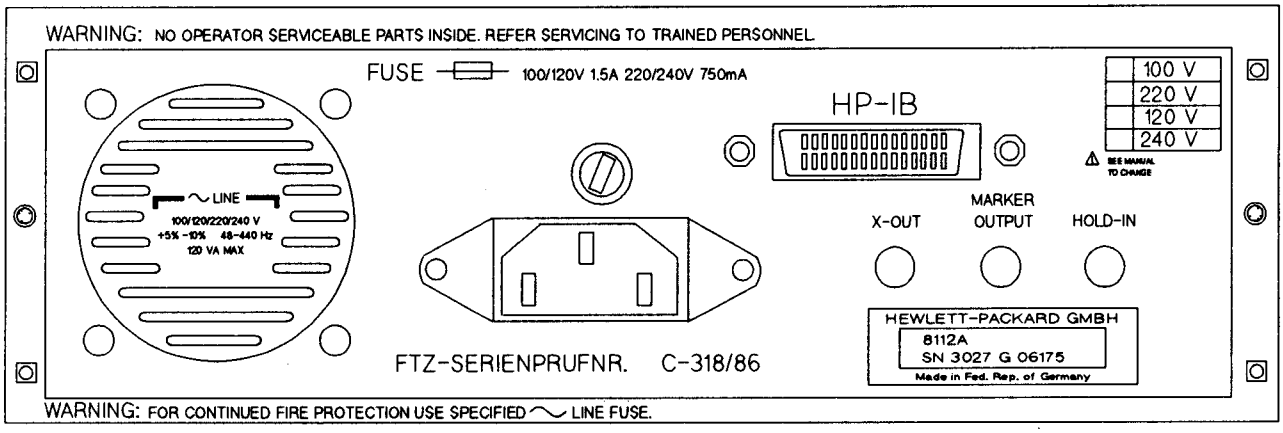


Figure 4-12. Rear panel

HP-IB Connector Refer to Figure 3-3 for a definition of the HP-IB connector pins. Refer to "Setting the HP-IB Address" in Chapter 6 if you want to know how to set the instrument's HP-IB address.

X-Out Not used with HP 8112A.

Marker Output Not used with HP 8112A.

Hold In Not used with HP 8112A.

Fuse The fuseholder accepts standard fuses to provide instrument protection in case of current overload. Refer to Table 3-1 for appropriate fuse selection.

5

Operating Examples

Introduction

To obtain an output from the HP 8112A it is only necessary to set the mode, period and transition type. Then press the green [SET] key. A stable error free pulse train is generated and you can then alter parameter values, and external input and control modes to derive your desired output.

Triggering Examples

The following examples show how the HP 8112A instrument can be set up for each type of trigger mode. The examples list the basic operating steps in the order in which they would normally occur after switching on.

In the applications section, examples are given of how the HP 8112A can be used in common design and test situations.

Normal Mode

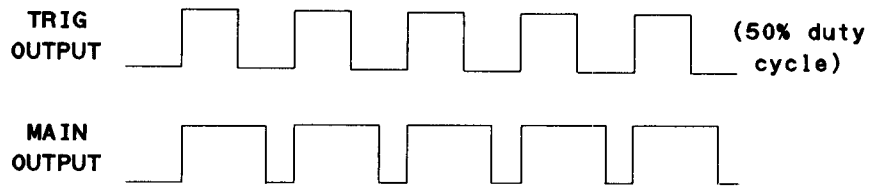


Figure 5-1. Typical output in Normal mode

1. Switch the instrument on using the line switch.
2. If neccessary, select normal mode by repeatedly pressing the standard mode key until the NORM LED is lit.
3. Select the Transition mode by pressing the key with the appropriate symbol. The parameter window will be automatically illuminated.

4. Select each output parameter in turn by pressing its associated key. Adjust the parameter value using the [VERNIER] and [RANGE] keys. Refer to Chapter 4 *Operating* for additional information on parameter adjustment.
5. If a Control Function is required, select the required mode by repeatedly pressing the control mode key until the required mode is lit. Apply the Control signal to the CTRL INPUT connector. Refer to Chapter 4 *Operating* for more permissible combinations of Operating and Control modes.

Note

You may wish to set up Output Limits as described in Chapter 4 *Operating* to protect the device under test.

6. Press the [DISABLE] key to turn off output disable mode and enable the output (LED extinguished).

Trig Mode

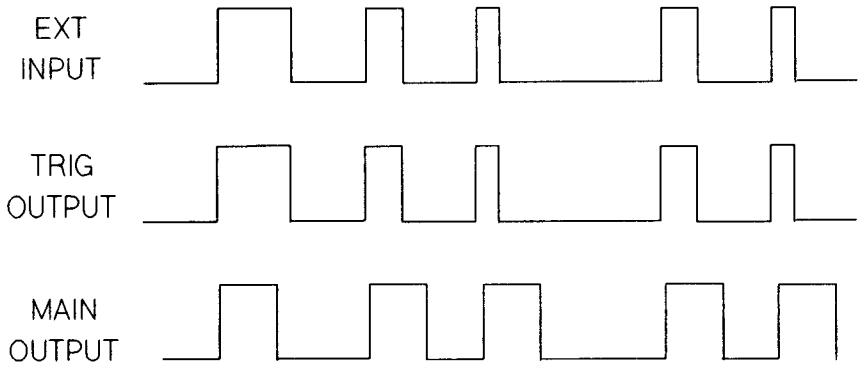


Figure 5-2. Typical signals in Trigger mode

1. Switch the instrument on using the line switch.
2. If neccessary, select Trig mode by repeatedly pressing the standard mode key until the TRIG LED is lit.
3. Apply the external trigger signal to the EXT INPUT and select trigger slope and level as required. Refer to Chapter 4 *Operating* for information on the trigger controls. Triggering can also be simulated using the [MAN] key.
4. If a modulated output is required, select the required modulation using the [CTRL] key. Apply the modulating signal to the CTRL INPUT connector. Refer to Chapter 4 *Operating* for more information on modulating the output signal.
5. Select the Transition mode by pressing the key with the appropriate symbol. The parameter window will be automatically illuminated.

6. Select each output parameter in turn by pressing its associated key. Adjust the parameter value using the [VERNIER] and [RANGE] keys. Refer to Chapter 4 *Operating* for additional information on parameter adjustment.
7. If a Control Function is required, select the required mode by repeatedly pressing the control mode key until the required mode is lit. Apply the Control signal to the CTRL INPUT connector. Refer to Chapter 4 *Operating* for more permissible combinations of Operating and Control modes.

Note

You may wish to set up Output Limits as described in Chapter 4 *Operating* to protect the device under test.

8. Press the [DISABLE] key to turn off output disable mode and enable the output (LED extinguished).

Gate Mode

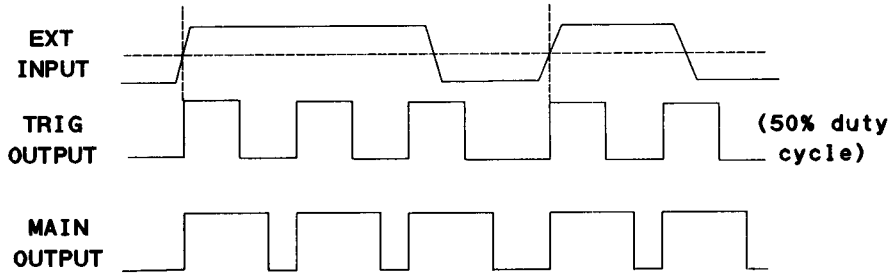


Figure 5-3. Typical signals in Gate mode

1. Switch the instrument on using the line switch.
2. If neccessary, select gate mode by repeatedly pressing the standard mode key until the GATE LED is lit.
3. Apply the external gating signal to the EXT INPUT and select trigger slope and level as required. Refer to Chapter 4 *Operating* for information on the trigger controls. Triggering can also be simulated using the [MAN] key.
4. Select the Transition mode by pressing the key with the appropriate symbol. The parameter window will be automatically illuminated.
5. Select each output parameter in turn by pressing its associated key. Adjust the parameter value using the [VERNIER] and [RANGE] keys. Refer to Chapter 4 *Operating* for additional information on parameter adjustment.

6. If a Control Function is required, select the required mode by repeatedly pressing the control mode key until the required mode is lit. Apply the Control signal to the CTRL INPUT connector. Refer to Chapter 4 *Operating* for more permissible combinations of Operating and Control modes.

Note

You may wish to set up Output Limits as described in Chapter 4 *Operating* to protect the device under test.

7. Press the (DISABLE) key to turn off output disable mode and enable the output (LED extinguished).

External Width Mode

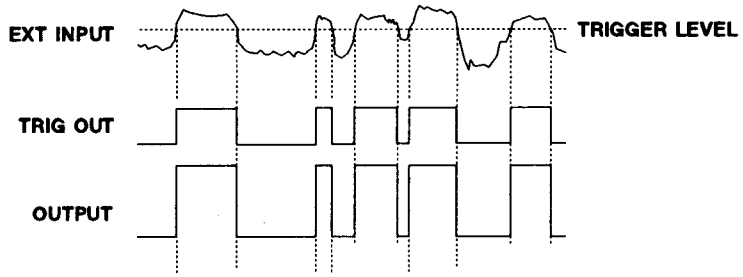


Figure 5-4. Typical signals in External Width mode

1. Switch the instrument on using the line switch.
2. If neccessary, select external width mode by repeatedly pressing the standard mode key until the E.WID LED is lit.
3. Apply the E.WID signal to the EXT INPUT and select trigger slope and level as required. Refer to Chapter 4 *Operating* for information on the trigger controls.
4. Select the Transition mode by pressing the key with the appropriate symbol. The parameter window will be automatically illuminated.
5. Select each output parameter in turn by pressing its associated key. Adjust the parameter value using the (VERNIER) and (RANGE) keys. Refer to Chapter 4 *Operating* for additional information on parameter adjustment.
6. If a Control Function is required, select the required mode by repeatedly pressing the control mode key until the required mode is lit. Apply the Control signal to the CTRL INPUT connector. Refer to Chapter 4 *Operating* for more permissible combinations of Operating and Control modes.

Note

You may wish to set up Output Limits as described in Chapter 4 *Operating* to protect the device under test.

7. Press the [DISABLE] key to turn off output disable mode and enable the output (LED extinguished).

External Burst Mode

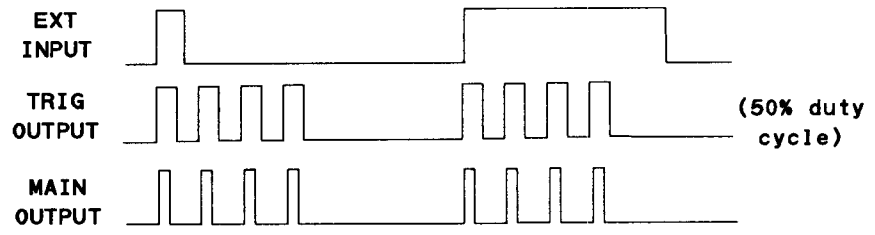


Figure 5-5. Typical signals in External Burst mode

1. Switch the instrument on using the line switch.
2. If neccessary, select external burst mode by repeatedly pressing the standard mode key until the E.BUR LED is lit.
3. Apply the E.BUR signal to the EXT INPUT and select trigger slope and level as required. Refer to Chapter 4 *Operating* for information on the trigger controls.
4. Select the Transition mode by pressing the key with the appropriate symbol. The parameter window will be automatically illuminated.
5. Select each output parameter in turn by pressing its associated key. Adjust the parameter value using the [VERNIER] and [RANGE] keys. Refer to Chapter 4 *Operating* for additional information on parameter adjustment.
6. If a Control Function is required, select the required mode by repeatedly pressing the control mode key until the required mode is lit. Apply the Control signal to the CTRL INPUT connector. Refer to Chapter 4 *Operating* for more permissible combinations of Operating and Control modes.

Note

You may wish to set up Output Limits as described in Chapter 4 *Operating* to protect the device under test.

7. Press the [DISABLE] key to turn off output disable mode and enable the output (LED extinguished).

Applications

Analog Applications

Fixed transition mode

The fixed transition time (5 ns), is ideally suited for step response measurements such as:

- Transient behaviour of amplifiers (transient time, overshoot, ringing, settling time).
- Reverse recovery time of transistors and diodes.
- Characterization of capacitors (equivalent serial resistance, inductance, high frequence capacitance).

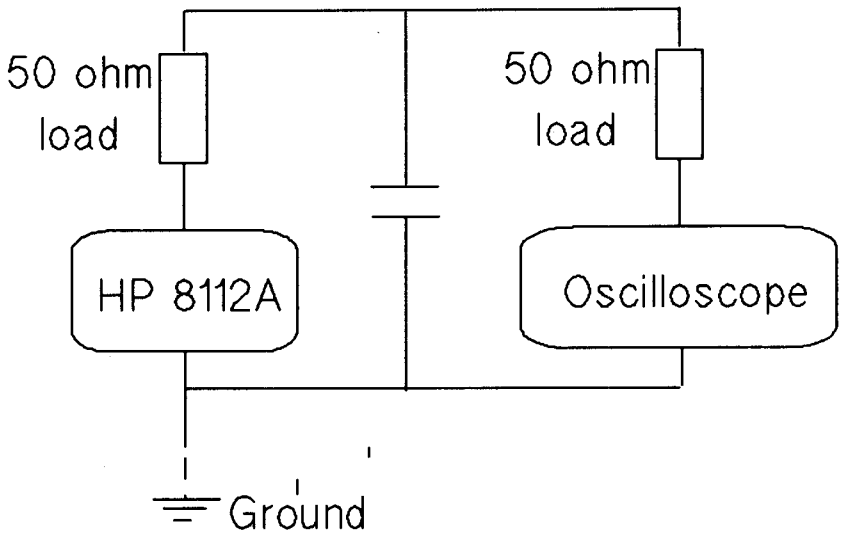


Figure 5-6. Capacitance circuit

Linear transition mode

Independantly variable leading and trailing edges between 6.5 ns and 95 ms can be used to generate ramps or sawtooth waveforms for:

- Stimulation of hydraulic or pneumatic devices
- Mechanical tests
- Hysteresis of Schmidt trigger circuits
- Stress testing of capacitors and thyristors by measuring maximum allowed voltage increase per time (max. dV/dt)

Cosine shaped transition modes (Gaussian)

Independantly variable cosine shaped leading and trailing edges between 6.5 ns and 95 ms can be used to generate smooth transitions which do not include high frequencies for:

- Communications, reduced reflections and crosstalk

- Simulation of bandpass filtered signals such as data transmission over telephone lines
- Generation of haversines

Digital Applications

Fixed transition mode

Can be used for stimulation of fast logic components and circuits as follows:

- Clock generation
- Producing known good data inputs for logic sub assemblies and modules
- Integrated circuit parameter settings
  - maximum clock speed
  - noise sensitivity and threshold level verification
  - set-up time
  - hold time
  - propagation delay
  - minimum clock pulse width

Linear variable transition mode

- Reduced relations and crosstalk
- Driving CMOS devices
- Parametric tests with manufacturer-recommended transition times

Cosine shaped transition mode

- Simulation of degraded pulses, for example after storage on a magnetic medium

6

Programming

General

In remote mode, all HP 8112A settings, except EXT INPUT trigger level, are programmable via the HP-IB. The HP 8112A also provides error messages and can report operating parameters when requested by the controller.

This chapter describes the valid programming mnemonics and syntax for the HP 8112A. Example program statements are based on HP BASIC 5.0/5.1 for the HP 9000 Series 200/300 controllers. Example program statements also assume that the instrument HP-IB address is 12 decimal.

This manual does not discuss the HP-IB protocol or hardware. For detailed information on the HP-IB refer to any of the following publications:

- IEEE Interface Standard 488–1975
- ANSI Interface Standard MC1.1.
- HP Publication 59401-90030
- HP Publication 5952-0058
- HP Publication 5952-0156

Setting the HP-IB Address

The HP 8112A's HP-IB address is set at the factory to 12 decimal. The address is stored in the instrument's RAM, along with the current instrument settings.

Note

- *You can only change the address in NORMal trigger mode, immediately after switching the instrument on.* Pressing the [LCL] key at any other time displays the current address while the key is depressed, but no change is possible.
- When allocating HP-IB addresses make sure no instruments on the bus have the same address.
- If the RAM battery fails, the HP-IB address is set to 12 when the instrument is switched on.

To change the instrument's HP-IB address:

1. Switch the instrument on.
2. If the instrument is NOT in NORM trigger mode:
   a. Select NORM trigger mode.
   b. Switch the instrument off and on again.
3. Press the [LCL] key. The current HP-IB address is displayed on the frontpanel.
4. Use the vernier keys to change the address.

5. Press the [LCL] key again to set the new address.

Local, Remote and Local Lockout

Local mode

In this mode the RMT LED is off, the front panel is used to operate the instrument and programming messages are ignored.

You can select local mode in the following ways:

- Switching the HP 8112A on.
- Pressing the [LCL] key, if Local Lockout is inactive.
- Sending an HP-IB Local command to the instrument from the system controller (use the LOCAL statement in BASIC 5.0/5.1).

```
LOCAL 712
```

The output signal and all instrument settings remain unchanged following a change from remote to local mode.

Remote mode

In this mode the RMT LED is illuminated and programming messages received via the HP-IB are interpreted (parsed) and used to control the instrument. The front panel controls are disabled apart from:

- The [LINE] switch.
- The trigger LEVEL adjust knob.
- The [LCL] key, if Local Lockout is inactive.

You can select remote mode by sending an HP-IB Remote Enable command from the system controller (use the REMOTE statement in BASIC 5.0/5.1).

```
REMOTE 712
```

The output signal and all instrument settings remain unchanged following a change from local to remote mode.

Local Lockout

The [LCL] key can be disabled by sending an HP-IB Local Lockout command from the system controller (use the LOCAL LOCKOUT statement in BASIC 5.0/5.1).

```
LOCAL LOCKOUT 712
```

This ensures that only the system controller can return the instrument to Local mode, except when the instrument is switched off and on again.

It is recommended that all programming applications use this facility, because if a programming message is interrupted by pressing the [LCL] key during data transmission from the system controller, the HP 8112A may be left in an unknown state.

Abbreviations used in this Document

EOL Sequence	End of Line Sequence (used for termination). Character(s) at the end of a line or message
EOI Signal	End-or-Identify Signal (separate HP-IB signal line used for terminating a message)
CR	carriage-return; ASCII character with the ASCII-code 13
CST	current settings command (used to read the current instrument state)
LF	line-feed; ASCII character with the ASCII-code 10
STB	Status Byte Register
RQS	Request Service Bit
SRQ	Service Request
SPOLL	Serial Poll (used to determine whether a device is requesting service; returns the value of the Status Byte Register)
PPOLL	Parallel Poll (not supported by the HP 8112A)
Learn String	ASCII string returned after a CST command; contains all necessary commands to set the HP 8112A to its present state. The Learn String may later be sent back to the device to place it in this state.

Terminators

The HP 8112A accepts the following terminators:

- CR/LF (the default EOL sequence)
- EOI only
- CR/LF and EOI
- LF and EOI

Note

LF alone is not accepted as terminator when the HP 8112A is connected to a HP9000 Series 200/300 controller. When connected to other controllers, the HP 8112A may accept LF as terminator.

The HP 8112A itself, terminates a data message sent to the computer with:
CR/LF followed by a SPACE character

The EOI line is not polled by the HP 8112A.

Programming

To select an operating mode or to set a parameter to a specific value, the appropriate ASCII mnemonic must be sent to the HP 8112A.

Example:

To set the Operating Mode to TRIG, the ASCII mnemonic M2 has to be sent to the HP 8112A.

HP Basic Statement for this is:

```
OUTPUT 712;"M2"
```

When programming parameters, such as Period, Delay or Width, the ASCII mnemonic must be followed by the value and the appropriate unit. The ASCII mnemonic, the value and unit may be separated by a comma or space character. For better readability it is recommended to use a space character.

Example:

To set the Period to 2.2 ms, the ASCII mnemonic PER followed by the new value 2.2 and the unit MS must be sent to the HP 8112A.

HP Basic Statement for this is:

```
OUTPUT 712;"PER 2.2 MS"
or
OUTPUT 712;"PER2.2MS"
```

Note

Program commands can be a combination of upper case or lower case ASCII characters, whereas the responses are always returned in uppercase.

Multiple Commands

You can send multiple programming commands on the same line. The commands may be separated by a comma or a space character. It is recommended to separate the commands with a comma, because this makes it easier to read such a programming message.

Examples:

`OUTPUT 712;"M1,CTO,PER 1.25 MS"`	*Commands separated with commas*
`OUTPUT 712;"M1 CTO PER 1.25 MS"`	*Commands separated with space characters*
`OUTPUT 712;"M1CTOPER 1.25 MS"`	*Commands not separated*

Commands which change modes are processed before commands which set parameters, irrespective of the command order within the programming message. If your application requires a parameter change to occur before a mode change, use seperate programming messages for the two commands.

The HP 8112A can be programmed into an error condition in just the same way as when using the front panel. For example, attempting to program a larger LOL than HIL:

```
OUTPUT 712;"HIL 1 V,LOL 2 V"
```

Refer to "Error, Fault and Status Reporting" for details of error, fault and status reporting using the HP-IB.

Selecting Trigger Modes

Standard Trigger Modes

Action	Mnemonic
Select NORM	M1
Select TRIG	M2
Select GATE	M3
Select E.WID	M4
Select E.BUR	M5

Trigger Control

Action	Mnemonic
Select trigger off	T0
Select positive trigger slope	T1
Select negative trigger slope	T2
Select both	T3

Example `OUTPUT 712;"M3,T1"` *Select GATE mode with a positive trigger slope.*

Selecting Control Modes

Action	Mnemonic
Switch off control mode	CT0
Select PERC	CT1
Select DELC	CT2
Select WIDC	CT3
Select HILC	CT4

Example `OUTPUT 712;"CT2"` *Select Delay Control*

Selecting Output Waveform Mode

Action	Mnemonic
Select fixed	W1
Select linear	W2
Select gaussian	W3
Select mode off	SM0
Select mode on	SM1

Example `OUTPUT 712;"W2,SM1"` *Select linear output waveform transitions*

Setting Parameters

Note

A parameter programming mnemonic is the same as its front panel description, DEL = delay for example.

Timing parameters

Action	Mnemonic	Value Delimiter
Set period	PER	NS = nanoseconds
Set delay	DEL	US = microseconds
Set double pulse	DBL	MS = milliseconds
Set width	WID	
Set leading edge	LEE	
Set trailing edge	TRE	
Set duty cycle	DTY	%

Example `OUTPUT 712;"PER 10 MS,DTY 30 %"` *Set period to 10 ms, set duty cycle to 30%.*

Level parameters

Action	Mnemonic	Value Delimiter
Set high level	HIL	V = volts
Set low level	LOL	V = volts

Example

```
OUTPUT 712;"HIL 2 V,LOL -1.25 V"
```

Set high level to plus 2 V, low level to minus 1.25 V

Burst Parameter

Action	Mnemonic	Value Delimiter
Set burst number	BUR	#

Example

```
OUTPUT 712;"BUR 375"
```

Provides a burst of 375 output pulses

Vernier

Action	Mnemonic
Most signicant digit up	MU
Second significant digit up	SU
Least significant digit up	LU
Most signicant digit down	MD
Second significant digit down	SD
Least significant digit down	LD

Example

```
OUTPUT 712;"HIL 5 V,SD,SD,SD"
```

Set high level to 5 V and decrement in three steps of 100 mV.

Range Change

Action	Mnemonic
Next higher range	RU
Next lower range	RD

Example

```
OUTPUT 712;"RU"
```
Change vernier range upwards

Stored Parameters

Action	Mnemonic	Value Delimiter
Store parameter set	STO	1.... 9 Set ident
Recall parameter set	RCL	0 = Standard
		1.... 9 Stored set

Example

```
OUTPUT 712;"STO 5"
```
Store current parameters set on instrument as setting number 5

```
OUTPUT 712;"RCL 0"
```
Revert instrument to standard parameter settings

Excessive Slope Calculation

Action	Mnemonic
Excessive slope calculation off	SR0
Excessive slope calculation on	SR1

Example

```
OUTPUT 712;"SR0"
```
Switches off calculation of excessive slope (speeds up program execution)

Reading parameters

The HP 8112A provides special commands with which information can be read by the computer. These commands are called Talker Function Commands. After Sending a Talker Function Command the HP 8112A will return a response message. A response message remains in the HP 8112A output queue until it is read or another command is issued.

For example, to read the current value of the Period, the following commands are necessary:

```
OUTPUT 712;"IPER"
ENTER ;A$
PRINT "8112A PER= ";A$
```

Note

After the Interrogate Parameter commands (IPER, IDEL, IDBL, etc.) the HP 8112A does not return only the numeric values, instead it returns an ASCII-response that contains the command to set the interrogated parameter to its present value.

If the current period is set to 1 ms, the variable A$ will contain the string "PER 1.00 MS" after conducting the example above.

It is possible to read the current setting of a parameter using the interrogation mnemonics listed here:

Standard

- IPER
- IDEL
- IDBL
- IDTY
- IWID
- ILEE
- ITRE
- IHIL
- ILOL
- IBUR

The HP 8112A reply has the same format as that used when setting the parameter, for example:

```
PER 10MS
```

The reply length is always 12 characters.

It is also possible to read all the instrument settings in one go using the CST mnemonic. Refer to "Reading the Current Settings"

Example

```
DIM B$[12]                  Dimension string allocates 12 characters of memory for reply.
OUTPUT 712;"IDEL"           Request current delay setting.
ENTER 712;B$                Read reply into allocated memory.
PRINT "8112A DEL= ";B$      Print the reply.
```

Selecting Output Modes

Output Controls

Action	Mnemonic
Switch off output limits	L0
Switch on output limits	L1
Switch off complementary output	C0
Complement output	C1
Enable output	D0
Disable output	D1

Example

```
OUTPUT 712;"L1,D0"
```

Switch on output limits and enable the output signal.

Reading the Current Settings

The Current Setting interrogate command CST tells the HP 8112A to send a response that contains all necessary commands to set the device to its present state. The response message, called (ASCII) learn string, can be retransmitted as a program message without alteration.

The learn string may be altered in the computer before retransmitting it. Since the learn string is made up of the several independent commands, it is possible to send parts of the learn string (complete commands) to the instrument.

Note

The description of the example program LRN_DEMO in Chapter 7 *Programming Examples* contains more details about the usage of the CST command. Also refer to the example program INTERROG.

When the HP 8112A replies with a string containing all current settings. The data is always in the same order:

```
M1,CT0,T1,W1,SM0,L0,C0,D1,BUR 001 #,PER 1.00 MS,DBL 200 US,DEL 65.0 NS,
DTY 50 %,WID 100 US,LEE 10.0 NS,TRE 10.0 NS,HIL 0.30 V,LOL -0.70 V
```

Example

```
DIM B$[153]                          Allocate memory for maximum reply length
OUTPUT 712;"CST"                     Request current settings of instrument
ENTER 712;B$                         Read reply into allocated memory
PRINT "8112A settings are:  ";B$     Print the reply.
```

Timing

The time taken for the HP 8112A to receive and implement a programming message can be divided into three parts:

Data Transmission Time

Send

This is the time taken to transmit the programming message over the HP-IB, which is 130 μs ms per ASCII character (7.6 kByte/sec). The system controller is free to continue with its program after this time.

Answer

This is the time taken by the HP 8112Ato transmit a message when error reporting or learn mode. Time is 1 ms per character, status byte < 15 ms

Implementation Time

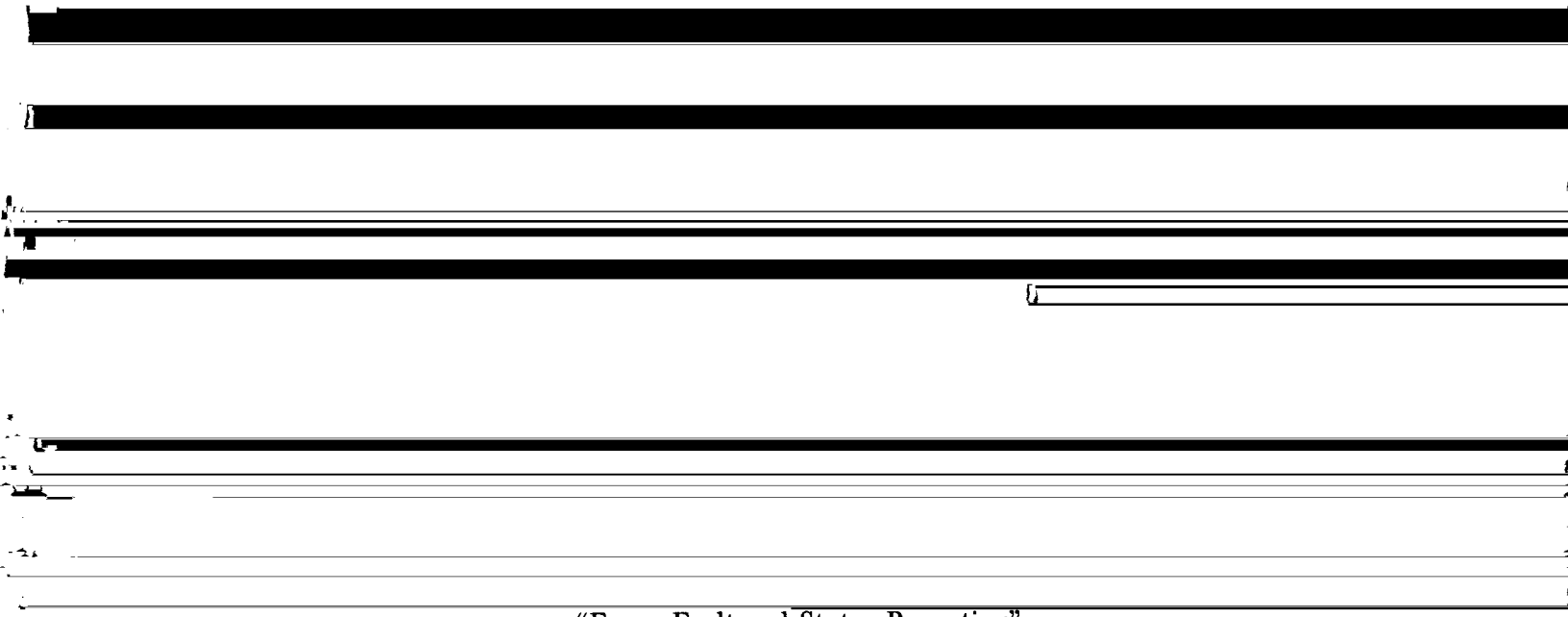
This is the time taken by the HP8112A to interpret and carry out all the commands in received message. Typical implementation times vary between 4 ms for select mode to 185 ms to recall a parameter set. Typical implementation times for various commands are given in the following table.

Table 6-1.

Command(s)	Implementation Time	Without Excess Slope calc.
Mode change	< 4 ms	
Control modes	< 50 ms	
Level	< 90 ms	
Burst	< 12 ms	
Timing (not in duty mode)	< 50 ms	< 25 ms
Duty cycle	< 80 ms	< 50 ms
Period (DTY active)	< 80 ms	< 50 ms
Store	6 ms	
Recall	180 ms	150 ms
Norm/Compl	< 4 ms	
Enable/Disable	< 4 ms	
Limit	< 4 ms	

The timings given are worst case. When parameter settings are combined into one programming message, the combined implementation time can be up to 40% more efficient.

The Buffer Not Empty flag in the HP 8112A status byte is set during this time. The system controller can therefore monitor this flag to [illegible] when a programming message has been implemented. Refer to



"Error, Fault and Status Reporting".

Hardware Settling Time

The hardware requires time to settle after a change. This sometimes takes longer than the time taken to interpret and execute the message, typically <5 ms.

Error, Fault and Status Reporting

HP-IB Status Byte

The HP 8112A is provided with the capabilities of requesting service from the controller (the computer) whenever the instrument detects an error.

To be able to determine if an error was caused, Status Reporting Structures are required. For this purpose the instrument contains the Status Byte register:

The Status Byte Register (STB) is composed of seven single-bit "summary-messages". Each of the bits 0 thru 5 summarizes a specific type of error. For example, bit 0 represents all types of Limit errors. (See the operating manual of the HP 8112A) Bit 6 of the STB is the Request Service (RQS) Bit and is set whenever a service request is caused. Bit 7 indicates whether the Buffer is empty or not.

After a Serial Poll (SPOLL) the complete Status Byte is cleared. The Status Byte is updated after every command received by the HP

Bit	Meaning
0	LIMIT ERROR (Causes SRQ)
1	TIMING ERROR (Causes SRQ)
2	SYNTAX ERROR (Causes SRQ)
3	SLOPE ERROR (Causes SRQ)
4	DUTY CYCLE ERROR (Causes SRQ)
5	INPUT ERROR (Causes SRQ)
6	SERVICE REQUEST (=SRQ)
7	BUFFER NOT EMPTY

The SRQ bit generates an interrupt at the system controller to indicate that the instrument requires attention. You can use this facility as the basis of interrupt driven error handling in your programming application.

The SRQ, Programming Error, Syntax Error and System Error bits are latched until the status byte is polled by the system controller. The other status bits represent the current condition at the time the status byte is read.

You can obtain more detailed information about timing and programming errors using the interrogate error (**IERR**) mnemonic. The HP 8112A responds with a string describing the current error conditions. The descriptions are covered in subsequent parts of this section.

```
DIM E$[45]                  Allocate memory for error string
OUTPUT 712;"IERR"           Request error information
ENTER 712;E$                Read reply into allocated string
PRINT "8112A Error= ";E$
```

Limit Error (Bit 0)

There are two types of error which set the limit error bit in the status byte. The conditions which cause them and the description used by the HP 8112A when replying to an **IERR** command are listed below. The limit error bit is not latched, therefore a transient error is only recorded by generating an SRQ.

Note

More than one error condition can occur at one time. When using the **IERR** command ensure that you allow for a reply containing more than one error description.

IERR Description	Comments
LIMIT ERROR	This error appears only when the limit is on and:

	a. the programmed High-level is greater than the limited High-level b. the programmed Low-level is lower than the limited Low-level
LIMIT-HILC	This error appears only when the limit is on and: a. High-level control has been selected b. no High-level limit is possible as HILC is an external control voltage

Timing Error (Bit 1)

There are two types of error (shown for NORM mode only) which set the timing error bit in the status byte. The conditions which cause them and the description used by the HP 8112A when replying to an **IERR** command are listed below. The timing error bit is not latched, therefore a transient error is only recorded by generating an SRQ.

Note

More than one error condition can occur at one time. When using the **IERR** command ensure that you allow for a reply containing more than one error description.

IERR Description	Comments
DELAY ERROR	■ Delay value is greater than Period value. i.e. PER 1 ms, DEL 1.1 ms ■ The front panel LEDs flash to indicate the invalid settings. ■ The ERROR LED is on
WIDTH ERROR	■ Width value is greater than Period value. i.e. PER 1 ms, WID 1.1 ms ■ The front panel LEDs flash to indicate the invalid settings. ■ The ERROR LED is on

Syntax Error (Bit 2)

This error occurs when the HP 8112A cannot understand a programming message. e.g DDY 50% instead of DTY 50%. The bit is latched until cleared by reading the status byte.

Slope Error (Bit 3)

This error is caused by excessive slope. The conditions which caused it and the description used by the HP 8112A when replying to an **IERR** command are listed below. The slope error bit is not latched, therefore a transient error is only recorded by generating an SRQ.

Note

More than one error condition can occur at one time. When using the **IERR** command ensure that you allow for a reply containing more than one error description.

IERR Description	Comments
EXCESSIVE SLOPE	

- No valid waveform at the output:
  a. LEE > WID×0.8 or (PER×DTY/100)×0.8
  b. TRE > (PER-WID)×0.8 or PER-(PER×DTY/100))×0.8
  c. TRE ≥ (DBL-WID)×0.8 or DBL-(PER×DTY/200))×0.8
  d. TRE ≥ (PER-DBL-WID)×0.8 or PER-DBL-(PER×DTY/200))×0.8
- No calculation with "SR1"

The "EXCESSIVE SLOPE" error message and calculation can be suppressed with the SR0 command. This will reduce programming time.

Example

```
OUTPUT 712; "SR0"
```

This is particularly useful for character strings where a multiple of the same timing parameter is programmed such as

```
OUTPUT 712;"SR0"
FOR A = 1 to 100
OUTPUT 712; "PER (CHR$ A) MS"
NEXT A
```

Immediately upon receiving the new PERIOD value, the HP 8112A would calculate the excessive slope error for each period time interval. By suppressing "EXCESSIVE SLOPE", new settings for Period are accepted by the instrument without any calculation, and a reduction in programming time of typically 30 ms may be achieved.

Note

In the permanently stored Mode/Parameter settings in the HP 8112A ROMs, "SR" is set to "0" (zero). If these settings are recalled as current settings, the Service Request function can be re-activated by programming "SR" to "1".

```
OUTPUT 712; "SR1"
```

The [LCL] key re-activates the Excessive Slope Error.

Duty Cycle Error (Bit 4)

There are three types of error which set the duty cycle error bit in the status byte. The conditions which cause them and the description used by the HP 8112A when replying to an **IERR** command are listed below. The timing error bit is not latched, therefore a transient error is only recorded by generating an SRQ.

Note

More than one error condition can occur at one time. When using the **IERR** command ensure that you allow for a reply containing more than one error description.

IERR Description	Comments
DTY-PERC	Duty cycle not available in PERC. An external voltage controls the Period and **NOT** the Duty Cycle
DTY-WIDC	As above. External voltage controls the Width and **NOT** the Duty Cycle
DTY-TRIG	An external trigger signal generates the Period. The displayed Duty Cycle is calculated from the internal Period. DTY is not confirmed with the external period

Input Error (Bit 5)

There are four types of error which set the input error bit in the status byte. The conditions which cause them and the description used by the HP 8112A when replying to an **IERR** command are listed below. The timing error bit is not latched, therefore a transient error is only recorded by generating an SRQ.

Note

More than one error condition can occur at one time. When using the **IERR** command ensure that you allow for a reply containing more than one error description.

IERR Description	Comments
EWID-PERC	The external trigger input signal is passed through to the output. A Control input cannot alter period, delay, or width. Identical returns are EWID-DELC and EWID-WIDC
TRIG-PERC	Both inputs will attempt to control the period. This is not possible.
GATE-TRIG slope	Both EXT INPUT slopes selected. Either leading edge or trailing edge may be specified but not both.
EWID-TRIG slope	As above. Either leading edge or trailing edge may be specified but not both.

Service Request (Bit 6)

This bit indicates that a service request has occurred. The bit is latched until cleared by reading the status byte.

Buffer not Empty (Bit 7)

This bit is set when there is data in the HP 8112A input buffer. You can monitor this bit to determine if the instrument has finished interpreting a long programming message.

HP-IB Universal Commands

The HP 8112A supports the following HP-IB Universal commands:

Note

These are HP-IB commands, NOT instrument programming commands. They are not used in programming messages. If you require more information on the HP-IB protocol and hardware refer to "General" for a list of references.

HP-IB Mnemonic	Description	BASIC 5.0/5.1 equivalent
DCL	Device Clear	CLEAR 7
SDC	Selected Device Clear	CLEAR 712
LLO	Local Lockout	LOCAL LOCKOUT 7
GTL	Go to Local	LOCAL 712 / LOCAL 7
GET	Group Execute Trigger	TRIGGER 712 / TRIGGER 7
UNL	Unlisten	SEND 712;UNL
UNT	Untalk	SEND 712;UNT
SPE	Serial Poll Enable	SPOLL(712)
SPD	Serial Poll Disable	
MLA	My listen address	selectable
MTA	My talk address	selectable

DCL An HP-IB DCL command causes the HP 8112A to load its standard parameter set. The instrument remains in its current mode (local or remote).

SDC An HP-IB SDC command causes the HP 8112A to load its standard parameter set and enter remote mode.

GET An HP-IB GET command simulates an external trigger to the HP 8112A in TRIG, E.BUR and E.SWP modes.

Hints for solving Problems that might occur

Reading the Status Byte

When programming the HP 8112A it must be considered that the instrument needs some time to:

- receive the commands
- interpret the commands
- update the Status Byte.

The hardware settling time must also be considered. (See Chapter 2 *Specifications* for more details).

When a command is sent to the HP 8112A, the device places all received characters into a buffer. Interpretation of the command(s) starts as soon as a valid terminator is received.

To determine if the buffer is empty or not, read the Status Byte by conducting a SPOLL. If bit 7 is set (decimal value of the STB is bigger than 127) then the buffer is not yet empty.

Whenever the status byte is read directly after sending a command, the HP 8112A should be given sufficient time to update the status byte. The time needed, varies with the type and number of the commands sent. For single commands 100 to 200 ms should be adequate.

Example:

```
10    CLEAR 712
20    A = SPOLL(712)
30    !
40    OUTPUT "WID 10 MS"    ! causes error
50    WAIT .2               ! give HP 8112A time to update the STB
60    PRINT "Status Byte:";A
70    END
```

If the wait period in line 50 is too low, the value of the Status Byte printed in line 60 will be 128. This indicates that the buffer is not yet empty. An adequate wait period (here 200 ms) will give the HP 8112A enough time to process the command and update the status byte. As expected, the value of the status byte printed in line 60 will therefore be 74.

Terminators

HP 8112As with the new firmware (starting with serial number 2851G07381) work correctly with the terminators listed on page 3. Devices with older firmware will hang up when receiving both CR/LF and EOI. Therefore termination with both CR/LF and EOI should be avoided when programming devices with old firmware.

Note

Since some controllers cannot (easily) be configured so that they do not to use CR/LF and EOI as terminator, the EOI line of some older devices is disconnected.

Users of some non-HP versions of BASIC may experience difficulty in terminating with CRLF alone, i.e. EOI cannot easily be turned off. If this is the case, a jumper setting inside the instrument allows EOI line to be ignored. To set this jumper proceed as follows:

- Remove rear feet and top cover
- Transfer jumper A3W3 at the center of the microprocessor board A3 from the factory setting *EOI* to position **3**.

The HP 8112A (with old and new firmware) does not pull the EOI line. The device terminates all messages with CR/LF and a space character.

Possible Problem with SPOLL

If the HP 8112A is the only instrument on the bus, the SPOLL statement may cause the instrument to "hang up".

Either of the following will clear the fault:

1. Use an HP-IB cable of not less than 2m length. Or:
2. Use a user-defined function to interrogate the status byte instead of the usual SPOLL statement.

In the following program, line 20 causes a syntax error so that a SRQ is generated. Lines 40 to 130 show how the status byte can be interrogated with a user-defined function:

```
10   A=712
20  OUTPUT A;"XYZ"
30   WAIT .05
40   PRINT "Status byte:",FNSpoll(A)
50  END
60  DEF FNSpoll(A)
70   S_code=A DIV 100
80   H_addr=A MOD 100
90   SEND S_code;UNL MLA TALK H_addr CMD 24
100  ENTER S_code USING "#,B";Stb
110  SEND S_code;CMD 25 UNT
120  RETURN Stb
130 FNEND
```

Interrogate Timing

After receiving an interrogate command, the HP 8112A needs some time until it is ready to send the response to the computer. If the device is not yet ready, it will send the string NO MESSAGE instead of the response. Should your computer be too fast for the HP 8112A, it will be necessary to force the computer to wait a few hundred milli-seconds before reading the response after an interrogate command.

The HP 8112A needs time to interpret and implement the commands which it receives. You need to allow for this in your controller program. A summary of programming timings is given in Table 6-1.

7

Programming Examples

Introduction

The following examples are an introduction to programming the HP 8112A using HP BASIC 5.0/5.1 for the HP 9000 Series 200/300 controllers. The examples cover the following subjects:

General Examples

- Testing communication with the HP 8112A.
- Performing the instrument self-test.
- Using the *Buffer not Empty* flag.

Common Task Examples

Program	Description
DEL_WID	Shows how to program and increment/decrement some HP 8112A parameters
SPOLL_2	Shows how to service a SRQ by directly conducting a SPOLL
INTR_2	Shows how to service SRQ's by using interrupts and print the error bits which are set in the status byte
ERROR_DEMO	Demonstrates how to determine which error bits are set in the status byte
LRN_DEMO	Shows how to read the Learn String with the CST command and how to send it back to the HP 8112A
INTERROG	Demonstrates the usage of all types of interrogate commands offered by the HP 8112A

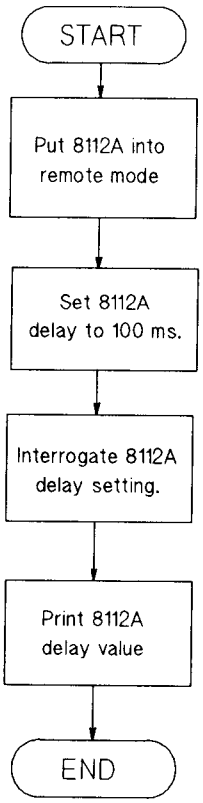
Note

In the examples it is not strictly necessary to put the HP 8112A into remote mode using the REMOTE 712 command because:

- The CLEAR 712 statement used to initialise the instrument also selects remote mode.
- The OUTPUT statement itself selects remote mode.

However, the REMOTE statement is included for completeness.

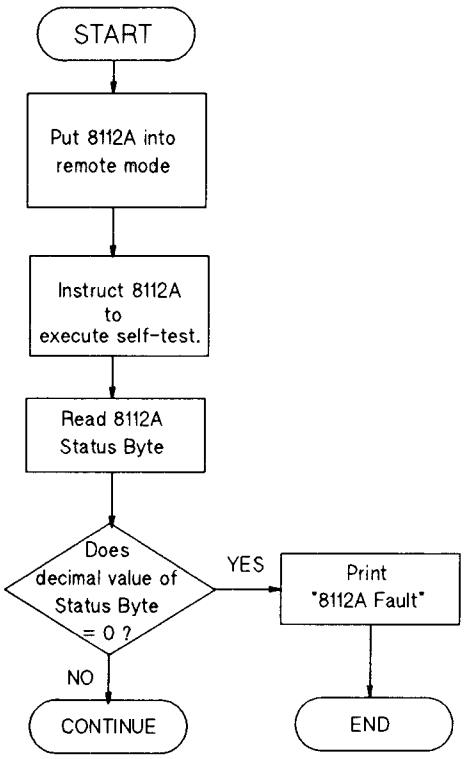
Testing communication



Programming applications should include an initial check that the HP 8112A is communicating correctly. A suitable quick check is to set a parameter to a particular value and then read it back, as illustrated by the flow chart and program example given here.

```
1     !                                Comments:
10    Adr=712                          !Device address of the HP 8112A
20    CLEAR Adr                        !Initialize Interface, set HP 8112A to
30    CLEAR SCREEN                     !Standard setting, and clear screen
40    A=SPOLL(Adr)                     !Clear the Status Byte
50    !
60    !        Program to check TALK/LISTEN FUNCTION
70    !
80    !                                                    (Visual Indicators)
90    !
100   REMOTE Adr                       !Enable Remote Control of HP 8112A
110   !                                                    (RMT LED on)
120   !
140   OUTPUT Adr;"DEL 100MS"           !Set HP8112A delay to 100 ms
150   !                                                    (RMT and ADS LED's on,
160   !                                                     DEL key LED on,
170   !                                                     '1.00 ms' displayed)
180   OUTPUT Adr;"IDEL"                !"Interrogate Delay" command
200   !
210   ENTER Adr;A$                     !Input data from HP 8112A
220   !
250   PRINT A$                         !Print on screen
260   !                                                  (Printout " DEL 100 MS")
270   !
290   LOCAL Adr                        !Return HP 8112A to local operating mode
300   !
320   END
```

Performing self-test

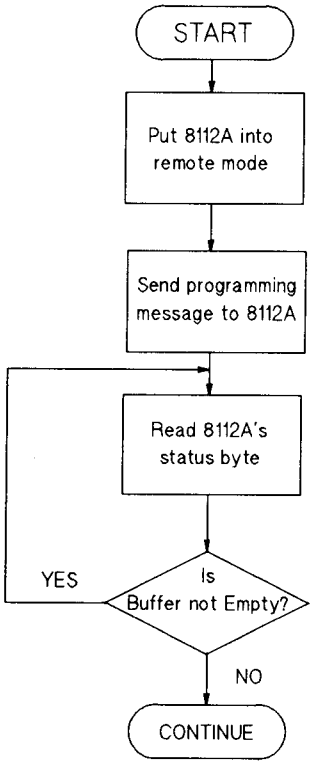


The HP 8112A RAM/Hardware self-test can be initiated via the HP-IB using the **EST** message. If a fault is detected, the HP 8112A sets the System Failure and Service Request bits in its HP-IB Status Byte. Refer to Chapter 6 *Error reporting* for more information on the Status Byte.

```
1     !                                Comments:
10    Adr=712                          !Device address of the HP 8112A
20    CLEAR Adr                        !Initialize Interface, set HP 8112A to
25    !                                !Standard setting and remote mode
30    CLEAR SCREEN                     !
40    A=SPOLL(Adr)                     !Clear the Status Byte
50    !
60    !        Program to check RAM and HARDWARE
70    !
80    !                                                  (Visual Indicators)
100   REMOTE Adr                       !Enable Remote Control of HP 8112A
110   !                                                  (RMT LED on)
140   OUTPUT Adr;"EST"                 !"Execute Self Test" command
150   !                                                  (RMT and ADS LED's on)
160   WAIT 1000                        !Time for HP 8112A internal processing
170   !
180   A=SPOLL(Adr)                     !Read and clear Status Byte
190   !
200   IF A=#0 THEN                     !If Status Byte is zero, HP 8112A has a fault
210   !
220   !   PRINT "HP 8112A FAULT WITH ERROR";A-64
230   !                                !Print fault message on screen which is Error
240   !                                !code minus the decimal value of the
250   !                                !Service Request
260   !
270   END IF
280   !
290   LOCAL Adr                        !Set HP 8112A to local operating mode
300   !
310   END
```

HP 8112A Self-test

Using the Buffer Not Empty Flag



The Buffer Not Empty flag indicates that the HP 8112A is currently interpreting a programming message. You can use the flag to make the system controller wait until a message has been implemented before proceeding. This is an alternative to using the WAIT statement with a fixed delay.

```
10    !                                  Comments:
20    Adr=712                            !Address of the HP 8112A
30    CLEAR Adr                          !Initialize interface, set HP 8112A to
40    !                                  !standard setting and remote mode
50    CLEAR SCREEN
60    A=SPOLL(Adr)                       !Clear the status byte
```

```
60    !
70    OUTPUT Adr;"M2,T1,W2,PER 10 US,DEL 80NS, WID 2.5 US"
80    !                                  !Select trigger mode with triggering on
90    !                                  !positive slope, linear transition output
100   !                                  !and change period, delay and width
110   !
130   REPEAT                             !Keep polling the HP 8112A status byte
140      A=SPOLL(712)                    !until Buffer Not Empty flag returns to
150   UNTIL BIT(A,7)=0                   !zero indicating the command message has
160   !                                  !been implemented
170   !
180   LOCAL Adr                          !Return HP 8112A to local mode
190   !
200   !
210   END
```

Common Task Examples

These are more comprehensive program listings which provide further examples of multiple commands involving program loops and sub routines

Program DEL_WID

Purpose

This program shows how to program and change some of the HP 8112A parameters periodically. In this example every 2 second Delay will be incremented by 1 ms while Width is decremented by 2 ms.

Comments

The interface is initialized and the HP 8112A is set to the standard settings (see Chapter)

Lines 100 to 120 setup period, delay, width, high-level, and low-level and line 130 enables the output.

The test signal is now output from the HP 8112A.

In the "Width and delay loop" (lines 250 to 350), every 2 second delay is incremented by 1 ms while width is decremented by 2 ms. The current values are printed in the Display subroutine (lines 440 to 490).

Width finally reaches the value of 2 ms.

Note

The output is not automatically disabled when the program is exited.

```
10    ! Program name: DEL_WID
20    !-------------------------------------------------------------
30    ! This example shows how to program and increment some HP8112A
40    ! parameters (width and delay).
50    !
60    Addr=712       ! Device address of the HP8112A
70    CLEAR Addr     ! initialize interface and set HP8112A to standard setting
80    A=SPOLL(Addr) ! clear the status byte
90    !
100   OUTPUT Addr;"PER40MS"            ! Set Period to 40 ms
110   OUTPUT Addr;"DEL9MS,WID22MS"     ! Set Delay to 9 ms, Width to 22 ms
120   OUTPUT Addr;"HIL2.5V,LOL-2.5V"   ! High Level=2.5V, Low Level=-2.5V
130   OUTPUT Addr;"DO"                 ! Enable Output
140   !
150   CLEAR SCREEN
160   PRINT "The test signals are output now."
170   PRINT
180   !
```

```
190   PRINT "Every two seconds delay is incremented by 1 ms and width is decremented"
200   PRINT "by 2 ms ..."
210   PRINT
220   !
230   ! Delay and Width loop
240   !
250   FOR I=0 TO 10
260     New_del=9+I*1
270     New_wid=22-I*2
280     !
290     GOSUB Display   ! Print the values for the Setup and Hold time
300     !
310     OUTPUT Addr;"DEL";New_del;"MS"
320     OUTPUT Addr;"WID";New_wid;"MS"
330     !
340     WAIT 2
350   NEXT I
360   !
370   LOCAL Addr  ! Turn HP8112A back to Local mode
380   PRINT
390   PRINT "End of the program DEL_WID."
400   STOP
410   !
420   !-------------------------------------------------------------
430   !
440 Display:! Display the current values of Delay and Width
450         PRINT "Delay = ";
460         PRINT USING "ZZ.DD,#";New_del
470         PRINT " ms            Width = ";
480         PRINT USING "ZZ.DD,"" ms""":New_wid

490         RETURN
500   END
```

Program SPOLL_2

Purpose

The main purpose of this program is to demonstrate how to service an SRQ directly in the program. It also demonstrates how to:

initialize the interface of the HP 8112A and set it to the standard setting
clear the status byte
conduct a serial poll (SPOLL)
return the instrument to local mode

Important program lines

```
130  CLEAR 712              Initialize the HP 8112A interface and
                            set it to the standard setting
170  A=SPOLL(712)           Read the status byte to clear it
210  OUTPUT 712;"XXX"       Case a syntax error
270  A=SPOLL(712)           Conduct a serial poll
280  PRINT "SPOLL= ";A      Print the result
310  LOCAL 712              Return the HP 8112A back to local
                            mode
```

Comments

Initialization section

The interface is initialized. The HP 8112A is set to the Standard Setting and the status byte is cleared

Main section

In the main section "XXX" is sent over the HP-IB to the instrument (line 210) but it is not a valid command so it causes a syntax error

Since the instrument needs some time to parse "XXX", the computer should wait a sufficient amount of time before conducting the following SPOLL (line 270). This is done by forcing the computer to wait for 0.1 seconds (line230).

The HP 8112A detects a syntax error and therefore sets the syntax error bit of the Status Byte. As a result, bit 6 of STB is set and a SRQ is generated. The result of the SPOLL printed in line 160 will be value 68.

After every SPOLL the complete status byte is cleared. This means the RQS bit is reset after the first SPOLL.

Note

The status byte is updated after every command received by the HP 8112A

Without the synchronization with the WAIT command (line 230), the SPOLL would be conducted whilst "XXX" is being parsed. At this moment there is neither a syntax error or SRQ active. The resultant SPOLL would be 128, indicating that the HP 8112A command buffer is not empty. (See Chapter 6 *Error, fault and status reporting*.

```
10    ! Name of this program: SPOLL_2
20    !-----------------------------------------
30    ! This program demonstrates that the HP8112A's
40    ! SRQ is cleared after SPOLL.
50    !
60    CLEAR SCREEN
70    CLEAR 712        ! Initialize Inteface and HP8112A
80    A=SPOLL(712)     ! clear status byte
90    !
100   !
110   A=SPOLL(712) ! read the status byte with SPOLL
120   PRINT "SPOLL before the syntax error = ";A
130   PRINT
140   PRINT "XXX is output. This will cause a syntax error."
150   OUTPUT 712;"XXX"      ! Cause a syntax error.
160   WAIT .1  ! give HP8112A time to receive "XXX" and update the Status Byte
170   !
180   A=SPOLL(712)
190   PRINT "1st SPOLL after syntax error = ";A
200   WAIT .1
210   A=SPOLL(712)
220   PRINT "2nd SPOLL after syntax error = ";A
230   PRINT
240   WAIT 2
250   A=SPOLL(712)
260   PRINT "SPOLL after waiting 2 seconds = ";A
270   PRINT
280   !
290   PRINT "End of the program SPOLL_2."
300   LOCAL 712
310   END
```

INTR_2

Purpose This program demonstrates how to use interrupts to service SRQs.

Comments

Setup section (lines 110 - 120):

The interrupt service subroutine Service_srq is set up. SRQs from interface 7 are enabled to cause an interrupt.

Main section

A SPOLL is conducted to show the value of the STB before the syntax error. The computer is forced to wait 2 seconds (line 190) for the SRQ before exiting the program.

Subroutine section

The Service_srq subroutine. This subroutine conducts a SPOLL. Then the value and the bits which are set in the Status Byte are printed.

```
10    ! Name of this program: INTR_2
20    !-------------------------------------------------------
30    ! This program demonstrates how to use interrupts to service
40    ! a SRQ from the HP8112A.
50    !
60    CLEAR SCREEN
70    !
80    CLEAR 712
90    A=SPOLL(712) ! clear status byte
100   !
110   ON INTR 7,2 CALL Service_srq  ! Setup service routine for SRQ
120   ENABLE INTR 7;2       ! Enable only service requests for interrupt.
130   !
140   A=SPOLL(712)
150   PRINT "SPOLL before the syntax error: ";A
160     !
170     PRINT "Syntax error caused"
180     OUTPUT 712;"XXX"
190     WAIT 2  ! Wait 2 seconds, to enable the HP8112A to request service
200     !
210   PRINT "End of the main program."
220   PRINT "End of the program INTR_2."
230   LOCAL 712
240   END
250   !
260   !=============================================================
270   !
280   ! Subroutine for servicing the interrupts.
```

```
290   !
300   SUB Service_srq
310     PRINT "-----------------------------------------"
320     PRINT "SRQ from HP8112A --> Main Program interrupted."
330     PRINT
340     Print_spoll ! read the Status Byte and print the results
350     PRINT
360     PRINT "End of the interrupt routine."
370     PRINT "-----------------------------------------"
380     ENABLE    ! Enable interrupts again.
390   SUBEND
400   !
410   SUB Print_spoll
420     ! The subroutine Print_spoll conducts a SPOLL to read the Status Byte.
430     ! Errors as indicated by the set bits are printed.
440     A=SPOLL(712)
450     PRINT "Value of the Status Byte (read with SPOLL): ";A
460     PRINT
470     PRINT "Service requested because of:"
480       IF BIT(A,5) THEN PRINT "- Input Error"
490       IF BIT(A,4) THEN PRINT "- Duty Cycle Error"
500       IF BIT(A,3) THEN PRINT "- Slope Error"
510       IF BIT(A,2) THEN PRINT "- Syntax Error"
520       IF BIT(A,1) THEN PRINT "- Timing Error"
530       IF BIT(A,0) THEN PRINT "- Limit Error"
540   SUBEND
```

ERROR_DEMO

Purpose

This program demonstrates how to determine which error bit(s) are set in the HP8112 Status Byte. Also it is shown how to get a more detailed description of an error with the interrogate error command IERR. Both functions are performed by the subroutine Print_errors.

Important program lines and their function

```
750   OUTPUT 712;"IERR"   Interrogate error
760   ENTER 712;A$        Read the response and store it
```

Comments

After an interrogate error command IERR the HP8112A returns a more detailed description of errors. The different error descriptions are separated by commas. If no error is active then the string "NO ERROR" is returned.

Note

The WAIT 2 statements in the program are only used to emphasize the functions of the program.

```
10    ! Name of this program: ERROR_DEMO
20
!-----------------------------------------------------------------"
30    ! This program demonstrates how to determine which error bit(s)
40    ! are set in the HP8112A's Status Byte. Also it is shown how to
50    ! get a more detailed description of an error with the
60    ! "Interrogate Error" (IERR) command. Both functions are performed
70    ! in the subroutine Print_errors.
80    !
90    CLEAR SCREEN
100   !
110   CLEAR 712    ! intialize interface and HP8112A
120   A=SPOLL(712) ! clear status byte
130   !
140   PRINT "Now Period is 1 ms, Width is set to 10 ms."
150   PRINT "This causes width and slope error (Width>Period) "
160   PRINT "-------------------------------------------------------"
170   !
180   OUTPUT 712;"WID10MS" ! set width to 10 ms (causes width error)
190   !
200   WAIT .1 ! HP8112A needs time to execute a command and update the
210           ! Status Byte.
220           !
230   GOSUB Print_errors
240   !
250   DISP "Pausing, press Continue to continue."
260   PAUSE
270   CLEAR SCREEN
280   !
290   PRINT "Now Width is set to 500 us. This removes the cause for the errors."
300   PRINT "-----------------------------------------------------------------"
310   !
320   OUTPUT 712;"WID500US"
330   !
340   WAIT .1 ! HP8112A needs time to execute a command and update the
350           ! Status Byte.
360   !
370   GOSUB Print_errors
380   !
390   PRINT
400   PRINT "End of the program ERROR_DEMO."
410   LOCAL 712
420   STOP
430             !
440 Print_errors:! prints the errors set in the Status Byte and uses the "IERR"
450             ! command to get more detailed descriptions of the errors.
460   !
```

```
510   PRINT
520   WAIT 2
530   !
540     PRINT "The following bits are set in the Status Byte:"
550       PRINT
560       WAIT 2
570       IF A=0 THEN PRINT "        No bit is set."
580       IF BIT(A,7) THEN PRINT "        Bit 7 --> Buffer Not Empty"
590       IF BIT(A,6) THEN PRINT "        Bit 6 --> Service Request"
600       IF BIT(A,5) THEN PRINT "        Bit 5 --> Input Error"
610       IF BIT(A,4) THEN PRINT "        Bit 4 --> Duty Cycle Error"
620       IF BIT(A,3) THEN PRINT "        Bit 3 --> Slope Error"
630       IF BIT(A,2) THEN PRINT "        Bit 2 --> Syntax Error"
640       IF BIT(A,1) THEN PRINT "        Bit 1 --> Timing Error"
650       IF BIT(A,0) THEN PRINT "        Bit 0 --> Limit Error"
660       PRINT "-------------------------------------------------"
670     !
680     ! Use the IERR command to get more detailed information.
690     !
700     WAIT 2
710     PRINT "More detailed decription read with the IERR command:"
720     WAIT 2
730     !
740     DIM A$[200]
750     OUTPUT 712;"IERR"   ! "Interrogate Error" command
760     ENTER 712;A$
770     PRINT A$
780     ! NOTE: The HP8112A's Status Byte is updated after every command.
790     !       In this program the Status Byte was cleared by
800     !       reading it with SPOLL before the IERR command was conducted.
810     !       To restore the previous status, the Status Byte has to be
820     !       cleared again.
830     WAIT .1      ! give HP8112A time to finish internal processing
840     A=SPOLL(712) ! clear the Status Byte
850     !
860     WAIT 2
870     PRINT
880     PRINT "================================================="
890     !
900     RETURN
910     !
20    END
```

LRN_DEMO

Purpose This program demonstrates the Learn String's usage:

- Reading the current Learn String with CST
- Sending the Learn String back to the HP8112A
- Time taken for transferring the Learn String is printed
- Recalling a setting from a location is shown (RCL0)

Comments There is no direct command in the Learn String which indicates the active parameter of the two modes: DELAY/DOUBLE and WIDTH/DTY. Instead the command of the active parameter is preceded by the non-active parameter's command. The two examples below will help to understand this structure.

Learn String (Delay Mode active)

M1,CT0,T1,W2,SM0,L0,C0,D1,BUR 0001 #,PER 1.00 MS,DBL 200 US, DEL 65.0
NS,DTY 50 %,WID 100 US,LEE 10.0 NS,TRE 10.0 NS,HIL +1.00 V,LOL +0.00 V,

Learn String (Double Mode active)

M1,CT0,T1,W2,SM0,L0,C0,D1,BUR 0001 #,PER 1.00 MS,DEL 65.0 NS,DBL 200
US, DTY 50 %,WID 100 US,LEE 10.0 NS,TRE 10.0 NS,HIL +1.00 V,LOL +0.00 V,

Please refer to the listing of the program for the exact usage of the commands above.

Note 

The Learn String consists of upto 153 ASCII characters.

The time for transferring Learn Strings may vary with different settings.

```
10    ! Program name: LRN_DEMO
20    !-----------------------------------------------------------------
30    ! Function: Demonstration of the Learn String's usage:
40    !             - Reading the current Learn String with "CST"
50    !             - Sending the Learn String back to the HP8112A
60    !           Additional features:
70    !             - Time taken for transfering the Learn String is printed
80    !             - Recalling a setting from a location is shown
90    !
100   CLEAR SCREEN
110   !
120   CLEAR 712     ! initialize interface and HP8112A
```

```
130   A=SPOLL(712)  ! clear Status Byte
140   !
150   DIM A$[153] ! The Learn String consists of 153 ASCII characters.
160   !
170   PRINT "Recalling setting from location 0 (Standard Setting) ..."
180   OUTPUT 712;"RCL0"
190   !
200   PRINT
210   PRINT "Reading the current setting ...";
220   Oldtime=TIMEDATE
230   !
240   OUTPUT 712;"CST"  ! read the current setting
250   ENTER 712;A$
260   !
270   Timetaken=((TIMEDATE-Oldtime) DIV .001)/1000
280   PRINT " ... finished."
290   PRINT "This took ";Timetaken;" seconds."
300   PRINT
310   PRINT "The current Learn String is:"
320   PRINT A$
330   PRINT
340   !
350   WAIT 4
360   PRINT "Period is set to 999 ms."
370   OUTPUT 712;"PER999MS"
380   WAIT 4
390   !
400   PRINT
410   PRINT "Sending the Learn String back to the HP8112A ...";
420   !
430   Oldtime=TIMEDATE
440   !
450   OUTPUT 712;A$
460   !
470   Timetaken=((TIMEDATE-Oldtime) DIV .001)/1000
480   PRINT " ... finished."
490   PRINT "This took ";Timetaken;" seconds."
500   PRINT
510   PRINT "End of the program LRN_DEMO."
520   !
530   LOCAL 712
540   END
```

INTERROG

Purpose This program demonstrates the usage of all types of interrogate commands offered by the HP8112A.

Comments Please refer to the listing of the program for the exact usage of the commands.

Below is a screen dump of the results printed when running the program.

The interrogate parameter set commands IRCL0..9 return the Learn String of the given setting with a prefix that indicates from which location the Learn String was loaded. For example, after the command IRCL5 the response returned will start with the prefix SET 5:. This prefix must be cut off, if the Learn String shall be sent back to the HP8112A.

The current setting of the HP8112A can be stored in another location with the command STO 1..9. For example, STO 3 stores the current setting in location 3.

Screen dump of the results printed when running the program INTERROG

```
The current setting of the HP 8112A is:
 M1,CT0,T1,W2,SM0,L0,C0,D1,BUR 0001 #,PER 1.00 MS,DBL 200 US,DEL 65.0 NS,DTY 50
%,WID 100 US,LEE 10.0 NS, TRE 10.0 NS, HIL +1.00 V,LOL +0.00 V,

The current setting of location 5 is:
 SET5:M1,CT0,T1,W2,SM0,L0,C0,D1,BUR 0001 #,PER 1.00 MS,DBL 200 US,DEL 66.0 NS,D
TY 90%,WID 500 US,LEE 100 US, TRE 100 US, HIL +1.00 V,LOL -4.56 V,

Width and slope error caused.
Errors read with IERR:  WIDTH ERROR , EXCESSIVE SLOPE

Response after IPER command:   PER 1.00 MS
Response after IHIL command:   HIL +1.00 V
Response after IBUR command:   BUR 0001 #

End of the program INTERROG
```

Program listing

```
10    ! Program name: INTERROG
20    !-----------------------------------------------------------------------
30    ! Function: Demonstrate the usage of all types interrogate commands
40    !           offered by the HP8112A.
50    !-----------------------------------------------------------------------
60    !
```

```
70    CLEAR SCREEN
80    !
90    CLEAR 712     ! initialize interface and HP8112A
100   A=SPOLL(712)  ! clear status byte
110   !
120   ! Learn String interrogate function CST (Current Setting)
130   !
140   DIM Setting$[153]
150   OUTPUT 712;"CST"
160   ENTER 712;Setting$
170   !
180   PRINT "The current setting of the HP8112A is:"
190   PRINT Setting$
200   PRINT
210   PRINT
220   !
230   ! Interrogate Parameter Set IRCL0..9
240   !
250   OUTPUT 712;"IRCL 5"   ! read setting from location 5
260   ENTER 712;Setting$
270   !
280   PRINT "The current setting of location 5 is:"
290   PRINT Setting$
300   PRINT
310   PRINT
320   !
330   ! Interrogate Error IERR
340   !
350   DIM A$[100]
360   OUTPUT 712;"WID1MS"   ! cause width and slope error
370   PRINT "Width and slope error caused."
380   !
390   OUTPUT 712;"IERR"     ! read error(s)
400   ENTER 712;A$
410   !
420   PRINT "Errors read with IERR: ";A$
430   PRINT
440   !
450   OUTPUT 712;"WID1US"   ! correct error
460   !
470   ! Interrogate Error commands (here: shown: IPER, IWID, and IPWD)
480   !
490   OUTPUT 712;"IPER"
500   ENTER 712;Period$
510   !
520   PRINT "Response after IPER command: ";Period$
```

```
580   !
590   OUTPUT 712;"IBUR"
600   ENTER 712;Burst$
610   !
620   PRINT "Response after IBUR command: ";Burst$
630   !
640   PRINT
650   PRINT "End of the program INTERROG."
660   !
670   LOCAL 712
680   END
```

8

Testing Performance

Introduction

This chapter lists a number of test procedures designed to test the electrical performance of the HP 8112A against the Specifications and Operating Characteristics given in Chapter 2 *Specifications*. The tests described are in two groups, Performance tests which check warranted Specifications and Verification tests which verify Operating Characteristics.

Performance Tests

- Period
- Delay
- Double Pulse
- Pulse Width
- Constant Duty Cycle
- Output Levels
- Transition Times
- Pulse Performance

Verification Tests

- Trigger, Gate, External Width and External Burst modes
- Man, 1 Pulse, Limit, Complement and Disable
- Store and Recall Functionality
- Period Control
- Delay Control
- Width Control
- High-Level Control
- HP-IB Capability

The tests can be used for incoming inspection, troubleshooting or preventative maintenance. Note that to prove that the instrument is within specification, only the Performance Tests have to be carried out. The test results can be recorded on a copy of the Test Records which follow the test procedures. Test results recorded at incoming inspection can be used for comparison after carrying out maintenance, repair or adjustments.

The tests must be performed with the HP 8112A in its normal operating condition, that is, with all shields, connections and the case in place.

Test Equipment

Table 8-1. Test Equipment

Instrument	Recommended Model	Required Characteristics	Alternative	Use*
Counter	HP 5335A with OPT 040	50 MHz, Start/Stop, TI, A to B	HP5345A	P, A
Digital Voltmeter	HP 3458A	DC 0.01 V–50 V, .004% acc. Pulse amplitude facility	HP 3478A HP 3456	P, A, T P,A,T
Function Generator	HP 8116A	20 MHz, THD ≤.1%	HP3324A #002	P, A
Digitizing Scope	HP 5412xT	>10 GHz Bandwidth <30 ps Transition times Flatness = 5%	HP 54503A	P, A
or	HP 5450A	< 100 MHz , 50Ω inputs		P, A
Signature Analyzer	HP 5005B			T
Power Supply	HP 6237B	0 - 20 V	HP 3324A	P, A, T
Attenuator	HP 33340C	20 dB, 2W		P, A, T
Adaptor		SMA to BNC		P, A, T
Terminators	HP 11048C HP 10100C	10 W, 50 Ω, ±0.1 % 2 W, 50 Ω		P, A T

* P = Performance Test; A = Adjustments; T = Troubleshooting

Test Record

Equipment Test Records are provided at the end of this chapter. Make a copy in order to record your test results.

Period Performance Test

Specifications

Range

20 ns to 950 ms

Accuracy

±5% of programmed value ±2 ns

Repeatability

Factor 4 better than accuracy

Max Jitter

0.2% of programmed value ±100ps

Equipment

- Counter (HP 5335A)
- Cable Assembly BNC
- 50 Ω Feedthrough Termination
  (Required if counter input impedance ≠ 50 Ω)

Test Setup

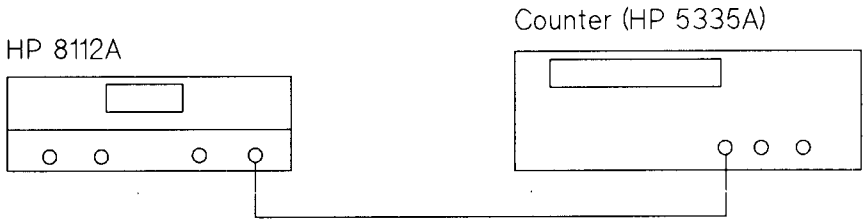


Figure 8-1. Period Performance Test

Procedure

1. Connect the equipment as shown in the setup figure. Use a 50 Ω feedthrough termination if you cannot select 50 Ω input impedance on the counter.
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
Transition	Fixed
DTY	50%
HIL	1.00 V
LOL	−1.00 V

3. Set the counter function control to PER A.
4. Set the HP 8112A Period to the following values and read the actual output from the counter. Record your results on a copy of

the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting	Counter reading	
PER	Low Limit	High Limit
20 ns	17.0 ns	23.0 ns
10 μs	9.5 μs	10.5 μs
10 ms	9.5 ms	10.5 ms
950 ms	902.5 ms	997.5 ms

Delay Performance Test

Specifications

Range

75 ns to 950 ms

Accuracy

$\pm$5% of programmed value $\pm$5 ns

Max Delay

1 period plus (+) 55 ns

Repeatability

Factor 4 better than accuracy

Max Jitter

0.2% of programmed value $\pm$100ps

Equipment

- Counter (HP 5335A)
- Two cable assembly BNC (same length)
- 50 Ω Feedthrough Termination
  (Required if counter input impedance $\neq$ 50 Ω)

Test Setup

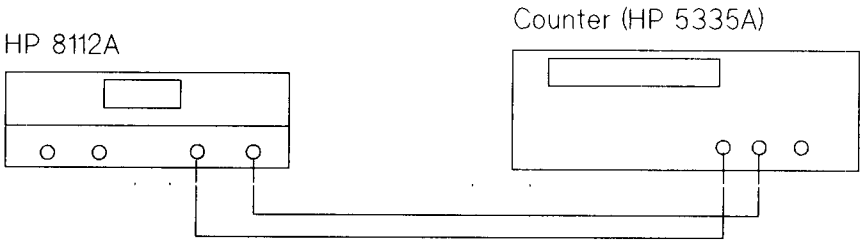


Figure 8-2. Delay Performance Test

Procedure

1. Connect the equipment as shown in the setup figure. Use a 50 Ω feedthrough termination if you cannot select 50 Ω input impedance on the counter.
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
Transition	Fixed
DTY	50%
HIL	2.40 V
LOL	0.00 V

3. Set the counter as follows:

TIME	A → B
Slopes A and B	Positive
Trigger levels	1.2 V
Gate Mode	→ MIN

4. Set the HP 8112A Delay and Period to the following values and read the actual output from the counter. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting		Counter reading	
DEL	**PER**	**Low Limit**	**High Limit**
75 ns	95 ns	-	83.75 ns
50 μs	95 μs	47.50 μs	52.50 μs
10 ms	95 ms	9.50 ms	10.50 ms
900 ms	950 ms	855.0 ms	945.0 ms

Double Pulse Performance Test

Note

The DBL measurement is described as the time interval between the two leading edges of the double pulse, recorded at 50% amplitude.

Specifications

Range

20 ns to 950 ms

Accuracy

±5% of programmed value ±2 ns

Repeatability

Factor 4 better than accuracy

Max Jitter

0.2% of programmed value ±100ps

Equipment

- Digitizing Oscilloscope with Accessory (HP 54121T)
- Counter (HP 5335A)
- Cable, 50 Ω, BNC to BNC, coaxial, 2 each (HP 8120-1839).
- 20 dB attenuators
- 50Ω feedthrough termination
  (Required if counter input impedance ≠ 50 Ω)

Test Setup 1

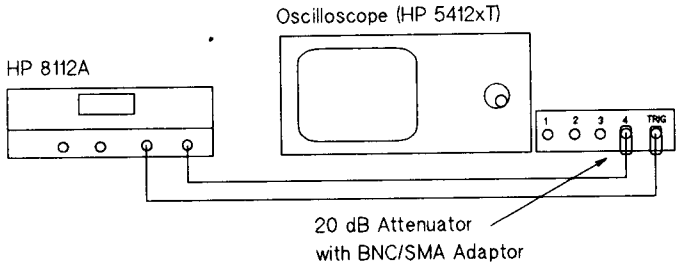


Figure 8-3. Double Pulse Performance Test

Test Setup 2

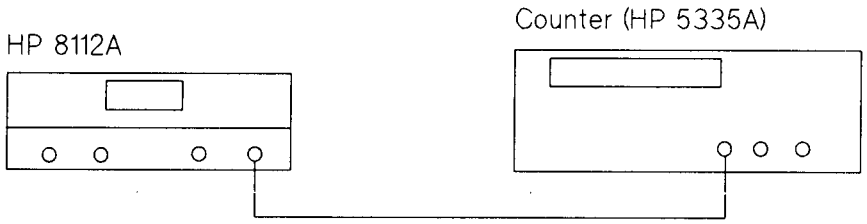


Figure 8-4. Double Pulse Performance Test

Procedure

1. Connect the HP 8112A to the oscilloscope as shown in Test Setup 1
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
Transition	Fixed
DEL	65 ns
HIL	1.00 V
LOL	−1.00 V

3. Connect the HP 8112 TRIG OUTPUT via a BNC to SMA adaptor and a 20 dB attenuator, to the TRIG Input of the HP 54121A.
4. Connect the HP 8112 OUTPUT via a BNC to SMA adaptor and a 20 dB attenuator, to Input 4 of the oscilloscope.
5. Set up the HP 54121T Oscilloscope as follows:
   a. Press AUTOSCALE.
   b. Select the Display menu and set the Number of Averages to 64.
   c. Select the delta V menu and turn the voltage markers On.
   d. Set Preset Levels = 50-50% and press Auto Level Set.
   e. Select the delta t menu and turn the time markers On.
   f. Set START ON EDGE = POS1 and STOP ON EDGE = POS2.
   g. Press the Precise Edge Find key for each new Double setting.
6. Check the HP 8112A double pulse delay.
7. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting			Oscilloscope	
PER	DBL	WID	Low Limit	High Limit
100 ns	20 ns	10 ns	17.0 ns	23.0 ns
100μs	20 μs	10 μs	19.0 μs	21.0 μs

8. Connect the HP 8112A to the counter as shown in Test Setup 2
9. Set the counter as follows:

   Trigger level Preset
   Mode PER A
   Impedance 50Ω
   Gate Mode → MIN
   Slope transition A Positive
10. Set up the HP 8112A as follows:

    Input Mode TRIG
11. Check the HP 8112A double pulse delay for each new DBL setting and at each change press the (MAN) key once.
12. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting			Oscilloscope	
PER	DBL	WID	Low Limit	High Limit
	20 ms	10 ms	19.0 ms	21.0 ms
	800 ms	50 ms	760.0 ms	840.0 ms

Pulse Width Performance Test

Specifications

Range

10 ns to 950 ms

Accuracy

±5% of programmed value ±2 ns

Repeatability

Factor 4 better than accuracy

Max Jitter

0.2% of programmed value ±100ps

Equipment

- Counter (HP 5335A)
- Cable Assembly BNC (2 ×)
- Digitizing Oscilloscope (HP 54121T)
- Attenuator 20 dB, 2 W. (2 ×)
- 50 ΩFeedthrough Termination
  (Required if counter input impedance ≠ 50 Ω).

Test Setup 1

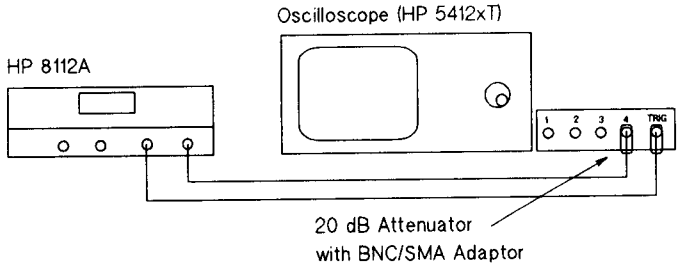


Figure 8-5. Pulse Width Performance Test

Test Setup 2

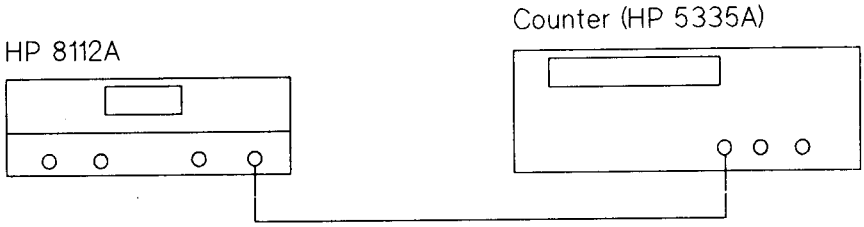


Figure 8-6. Pulse Width Performance Test

Procedure

1. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
Transition	Fixed
DEL	65 ns
HIL	1.00 V
LOL	−1.00 V

2. Connect the HP 8112A and oscilloscope as shown in Figure 8-5.
3. Verify that for the following HP8112A WID settings the scope display indicates that the HP 8112A output is within the specified limits.
4. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

Note Pulse width is measured at 50% of pulse amplitude.

HP 8112A setting		Oscilloscope	
PER	**WID**	**Low Limit**	**High Limit**
100 ns	10 ns	7.5 ns	12.5 ns
200μs	40 μs	38.0 μs	42.0 μs

5. Connect the HP 8112A and counter as shown in Figure 8-6.
6. Set the counter as follows:

Trigger level	Preset
Mode	Time A → B
Impedance	50Ω
Gate Mode	→ MIN
Slope A	Positive
Slope B	Negative

7. Check the HP8112A WID settings against the table below
8. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting		Oscilloscope	
PER	**WID**	**Low Limit**	**High Limit**
5 ms	1 ms	0.95 ms	1.05 ms
999 ms	950 ms	902.5 ms	997.5 ms

Constant Duty Cycle Performance Test

Specifications

Range

1% to 99% of period. 10 ns min, PER−10 ns max.

Accuracy

±10% of programmed value

Repeatability

Factor 4 better than accuracy

Equipment

- Counter (HP 5335A)
- Cable Assembly BNC
- 50 Ω Feedthrough Termination
  (Required if counter input impedance ≠ 50 Ω).

Test Setup

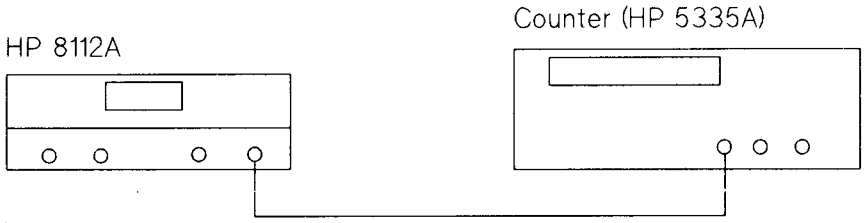


Figure 8-7. Duty Cycle Performance Test

Procedure

1. Connect the equipment as shown in the setup figure. Use a 50 Ω feedthrough termination if you cannot select 50 Ω input impedance on the counter.
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
Transition	Fixed
PER	100μs
DEL	65 ns
HIL	1.00 V
LOL	−1.00 V

3. Set the counter to DTY CY A.
4. Set the HP 8112A DTY to the following values and read the actual output from the counter. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting	Counter reading	
DTY	Low Limit	High Limit
1.0%	0.9%	1.1%
10%	9%	11%
50%	45%	55%
90%	81%	99%
*99%	89.1%	-

Note

* Using the (VERNIER) key adjust the duty cycle in steps until the counter displays 99%.

Output Levels Performance Test

Specifications (values in parenthesis into open circuit)

High Level Range

−7.90 V to 8.00 V (−15.8 V to 16.0 V)

Low Level Range

−8.00 V to 7.90 V (−16.0 V to 15.8 V)

Level Accuracy

±40 mV ±1% of programmed value ±3% of amplitude

Repeatability

Factor 4 better than accuracy

Equipment

- Digital Voltmeter (HP 3458A)
- Two Cable Assemblies BNC (same length)
- 50Ω feedthrough connector (±0.1%)

Test Setup

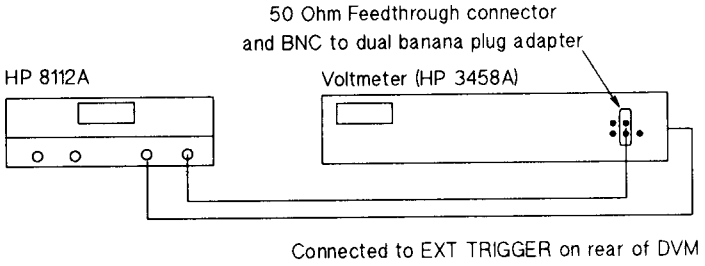


Figure 8-8. Output Levels Performance Test

Procedure

1. Connect the equipment as shown in the setup figure. Use a 50 Ω feedthrough termination 0.1%.
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
Transition	Fixed
PER	100 ms
DEL	6.5 ms
DTY	50%
HIL	+0.10 V
LOL	0.00 V

3. Set up the DVM as follows:

Function	DCV

Trigger EXT

4. For each value of HIL in table, verify that the DVM reading is within the specified limits.
5. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting	HP3458A Reading	
HIL	Low Limit	High Limit
0.1 V	0.056 V	0.144 V
0.5 V	0.44 V	0.56 V
1.0 V	0.92 V	1.08 V
5.0 V	4.76 V	5.24 V
8.0 V	7.64 V	8.36 V

6. Set up the HP 8112A as follows:

DEL	65 ns
HIL	0.0 V
LOL	−0.10 V

7. For each value of LOL in table, verify that the DVM reading is within the specified limits.
8. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting	DVM Reading	
LOL	Low Limit	High Limit
−0.1 V	−0.056 V	−0.144 V
−0.5 V	−0.44 V	−0.56 V
−1.0 V	−0.92 V	−1.08 V
−5.0 V	−4.76 V	−5.24 V
−8.0 V	−7.64 V	−8.36 V

Note

Specification for LOL/HIL = 0 V is ±40 mV, ±3% of amplitude.

Transition Time Performance Test

Specifications

10% - 90% of amplitude

Leading and trailing edge times are independently programmable within a common range (max ratio = 1:20)

Fixed transition (typical)

5ns for leading and trailing edges

Linear transitions

LEE and TRE, 6.5 ns to 95 ms

Accuracy

±5% of programmed value, ±2ns

Linearity (typical)

±3% for transition times greater than 100ns

Equipment

- Oscilloscope HP 54121T
- Two Cable Assemblies BNC

Test Setup

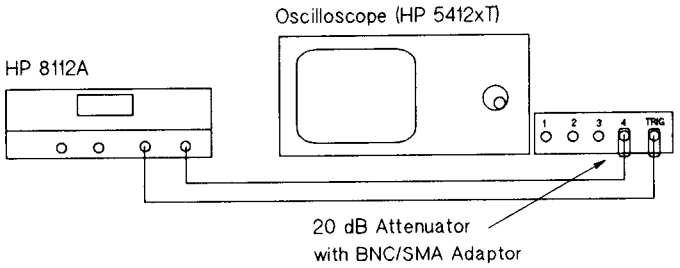


Figure 8-9. Transition Times Performance Test

Procedure

1. Connect the equipment as shown in the setup figure above.
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
PER	100 ns
DEL	65 ns
DTY	50%
HIL	1.00 V
LOL	0.00 V

Fast transitions

- Verify that for the following HP 8112A settings, the sampling scope display indicates, the transition times are within the specified limits.
- Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

HP 8112A setting				Oscilloscope	
Transition	**PER**	**LEE**	**TRE**	**Low Limit**	**High Limit**
Fixed	100 ns	4.5 ns	4.5 ns	-	5.0 ns (typical)
Linear	100 ns	6.5 ns*	6.5 ns	-	8.825 ns

Note

* Under programming to 5.5 ns is permissible to meet this specification.

Slow transitions

- Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
PER	2 μs
DEL	65 ns
DTY	50%
Transition	Linear
HIL	+5.00 V
LOL	0.00 V

- For the HP 8112A to the settings in the table below, measure the displayed leading edges (LEE) and trailing edges (TRE).
- Verify that the transition times do not exceed the specified limits.
- Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

Note

The oscilloscope response is **very slow** for measurements with PER in the **ms** range. The HP 54503A or the HP 54100D oscilloscopes will provide faster response.

HP 8112A setting			Oscilloscope	
PER	**LEE**	**TRE**	**Low Limit**	**High Limit**
2 μs	500 ns	500 ns	473 ns	527 ns
500 μs	100 μs	100 μs	95 μs	105 μs
2 ms	500 μs	500 μs	475 μs	525 μs
5 ms	999 μs	999 μs	949 μs	1.049 ms
5 ms	1 ms	1 ms	0.95 ms	1.05 ms
50 ms	10 ms	10 ms	9.5 ms	10.5 ms

Pulse Performance Test

Specifications

Preshoot, Overshoot, Ringing

5% of amplitude ±10 mV for both Linear and Gauss modes, 10% of amplitude ±10 mV for Fixed transitions

Settling time

100 ns + transition time

Source Impedance

50 Ω

Equipment

- Digital Oscilloscope (HP 54121T)
- Two Cable Assemblies BNC
- Attenuator 20 dB, 2 W (two off)

Test Setup

Procedure

1. Connect the equipment as shown in the setup figure above.
2. Set up the HP 8112A as follows:

Input Mode	NORM
Control Mode	Off
PER	500 ns
DEL	65 ns
DTY	50%
Transition	Fixed
HIL	1.00 V
LOL	0.00 V

3. Adjust the oscilloscope so that one pulse fills the display.
4. Examine the HP 8112A output on the scope display in order to verify that the pulse characteristics do not exceed the specified limits as identified in Figure 8-11.

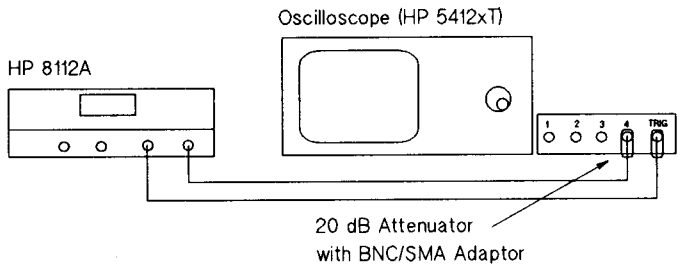


Figure 8-10. Pulse Performance Test

5. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

Note

The oscilloscope trace flatness error may affect the measurement of pre- and overshoot.

Characteristic	Specification
Preshoot	≤±10% of amplitude ±10 mV
Overshoot/Ringing	≤±10% of amplitude ±10 mV
Settling time	≤105 ns

6. Change HP 8112A settings as follows:

Transition	Linear
LEE	6.5 ns
TRE	6.5 ns

7. Examine the HP 8112A output on the scope display in order to verify that the pulse characteristics do not exceed the specified limits as identified in Figure 8-11.
8. Record your results on a copy of the Test Record, specified limits are given here and on the Test Record.

Note

The oscilloscope trace flatness error may affect the measurement of pre- and overshoot.

Characteristic	Specification
Preshoot	≤±5% of amplitude ±10 mV
Overshoot/Ringing	≤±5% of amplitude ±10 mV
Settling time	≤107 ns

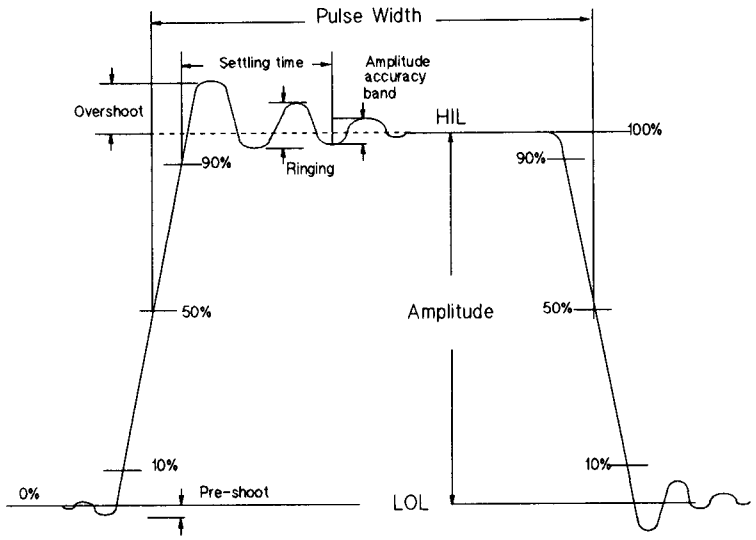


Figure 8-11. Pulse Performance Characteristics

Trigger,Gate,E.Width and E.Burst Verification Test

Characteristics

Trigger

Minimum amplitude 500 mV (p-p)

Minimum pulse width 10 ns

Each active input generates one output pulse.

Gate

- External signal enables Period Generator.
- First output pulse synchronous with external trigger.
- Last output pulse always completed.

External Width

Restoration of external signal with selectable transition times and output levels.

External Burst

Each active input transition generates a preprogrammed number of pulses (1 to 1999). Minimum time between bursts is 100 ns.

Max Input

±20 V

Equipment

- Pulse/function generator (HP 8116A)
- Oscilloscope (HP 54121T)
- Attenuator 20 dB, 2 W (4 ×)
- Cable Assembly BNC (5 ×)
- BNC T-connector

Test Setup

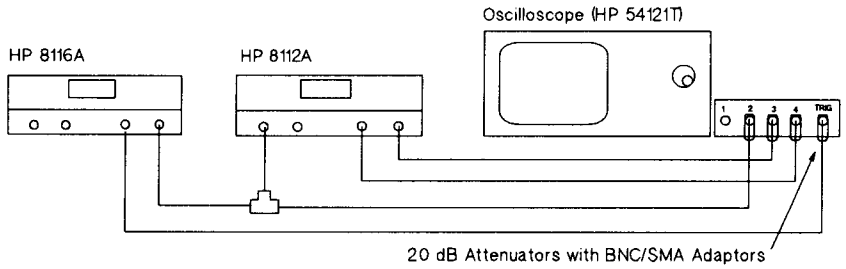


Figure 8-12. Trigger, Gate,E.WID & E.BUR Verification Test

Procedure

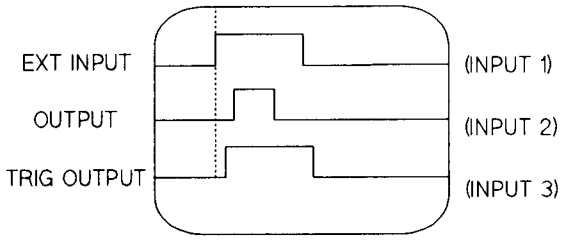
1. Connect the equipment as shown in the setup figure
2. Set up the HP 8112A as follows:

Trigger Mode	TRIG
Trigger Slope	ƒ
Control Mode	Off
Transition	Fixed
PER	2.0 μs
DEL	65 ns
WID	1.0 μs
HIL	1.00 V
LOL	0.00 V

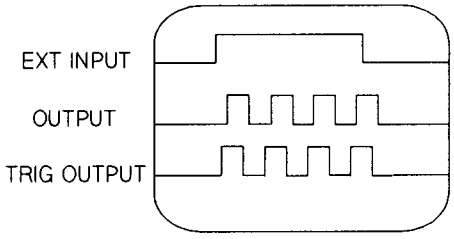
3. Set up the external pulse generator (HP 8116A) as follows:

Frequency	50 kHz
Width	5.0 μs
Amplitude	2.0 V
Offset	0.00 V

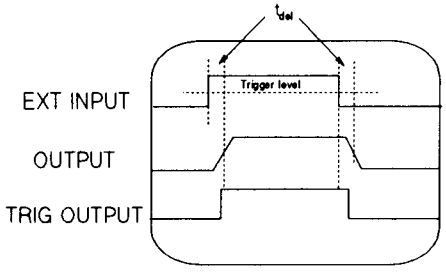
4. Using the oscilloscope, adjust the HP 8112A trigger level to allow triggering from the external pulse generator.
5. Verify that each external trigger pulse generates one complete output cycle as shown shown here.



6. Set the HP 8112A to GATE trigger mode, PER = 900 ns and DTY = 50%. Verify that each gate leading edge releases a train of output pulses and that each cycle is complete. As shown here.



7. Set the HP 8112A to E.WID trigger mode
8. Select Linear transition and LEE, TRE to 1 μs
9. Verify that each external input pulse triggers an output pulse of the same width, as shown here.

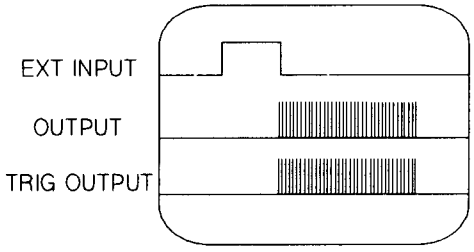


10. Set up the HP 8112A as follows:

Input Mode	E.BUR
Control Mode	Off
Transition	Fixed
BUR	50
PER	300 ns
DEL	65 ns
DTY	50%
HIL	1.00 V
LOL	0.00 V

11. Change the external pulse generator (HP 8116A) width setting to 1.0 μs.

12. Using the oscilloscope, adjust the HP 8112A trigger level to allow triggering from the negative going edge of the external input signal.
13. Set the oscilloscope sweep speed to 2 μs/division.
14. Verify that each external trigger pulse generates a burst of 50 output pulses as shown here.



Output Mode Verification Test

Characteristics

MAN	Simulates an external input
1 Pulse	Provides one output pulse in TRIG, Gate, and E.BUR modes
Limit	Implements the present output levels as output limits to protect the device under test. (when lit).
Complement	Inverts the output signal (when lit).
Disable	Disconnects the output (default at switching on).

Test Setup 1

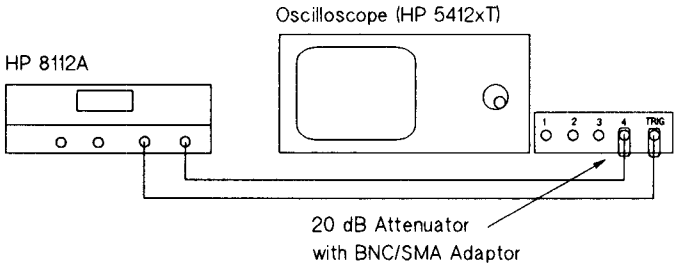


Figure 8-13 Output Mode Verification Test

Test Setup 2

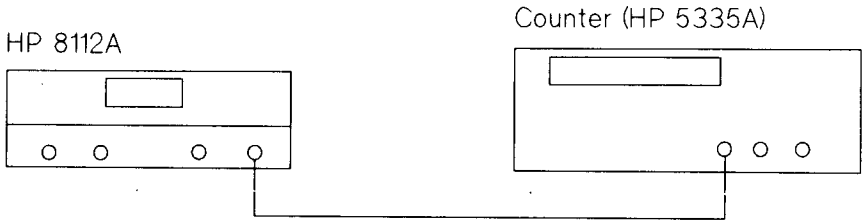


Figure 8-14. Output Mode Verification Test

Equipment

- Oscilloscope (HP 54121T)
- Counter (HP 5335A)
- Cable Assembly BNC (2 ×)
- Attenuator 20 dB, 2 W (2 ×)
- 50Ω Feedthrough Termination
  (required if counter input impedance ≥ 50Ω

Procedure

1. Connect the equipment as shown in the setup 1 figure
2. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
Transition	Fixed
BUR	472
PER	1.0 μs
DEL	65 ns
DTY	25%
Complement Output	Off
HIL	2.0 V
LOL	−2.0 V
Limit Mode	Off

3. Verify that the output signal is inverted by pressing the [COMPL] key.
4. Deselect the [COMPL] key.
5. Verify that the [DISABLE] key disables the output signal.
6. Re-enable the output signal.
7. Change Limit mode to ON
8. Press the [HIL] key and verify that the vernier keys do not increase the HIL beyond the +2.0 V as set previously.
9. Press the [LOL] key and verify that the vernier keys do not decrease the LOL below the -2.0 V as set previously.
10. Reconnect the equipment as setup 2. (use the 50Ω feedthrough if neccessary).

11. Change the HP 8112A settings as follows:

Input Mode	E.BUR
HIL	2.0 V
LOL	−2.0 V

12. Set the counter as follows:

TOT	**A**
GATE	Manual Open
Slope A	Positive
Trigger level	preset

13. Press the [MAN] key on the HP 8112A to simulate an external trigger and verify that the counter counts 472 pulses.
14. Press the [1 PULSE] key and confirm that the counter reading increments to 473.

Period Control Verification Test

Characteristics

Pulse Period ratio	1:10
Control Voltage	1.0 V to 10 V
Period Ranges	20 ns to 1.0 s in eight non-overlapping decade ranges
Bandwidth	1 kHz

Equipment

- Counter (HP 5335A)
- Variable Power Supply (HP 6237B or HP 3324A)
- Cable Assembly BNC (2 off)
- 50 Ω Feedthrough Termination
- BNC to Banana plug adaptor

Test Setup

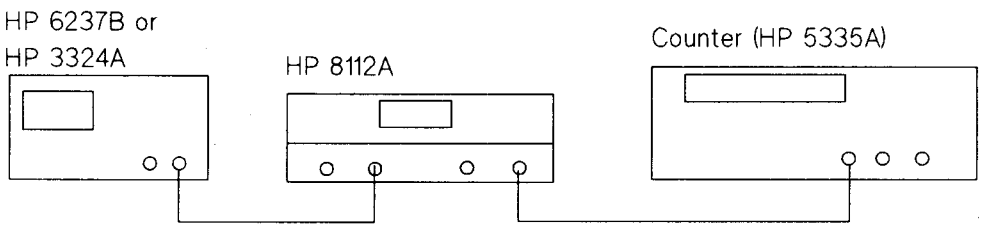


Figure 8-15. Period Control Verification Test

Procedure

1. Connect the equipment as shown in the setup figure
2. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	PERC
Transition	Fixed
DEL	65 ns
HIL	2.00 V
LOL	0.00 V

3. Vary the power supply (or HP 3324 in DC Mode) between approximately 1 volt and 10 volts, and verify that the counter display indicates a range of periodic times which agree with the specified limits for each of the HP 8112A settings below.

HP 8112A setting		Counter reading	
PER	**WID**	**Low**	**High**
100 ns	10 ns	20 ns	100 ns
10 μs	1 μs	1 μs	10 μs
10 ms	1 ms	1 ms	10 ms
1000 ms	100 ms	100 ms	1.0 s

Delay Control Verification Test

Characteristics

Pulse Delay ratio 1:10

Control Voltage 1.0 V to 10 V

Delay Ranges 10 ns to 1.0 s in eight non-overlapping decade ranges. The fixed 55 ns delay of the instrument has to be added to the delay induced by the CTRL voltage

Bandwidth 1 kHz

Equipment

- Oscilloscope (HP 54121T)
- Counter (HP 5335A)
- Variable DC Source (HP 6237B or HP 3324A)
- Cable Assembly BNC (7 off)
- Attenuator 20 dB, 2 W (2 ×)
- BNC to Banana plug adaptor
- BNC TEE piece

Test Setup

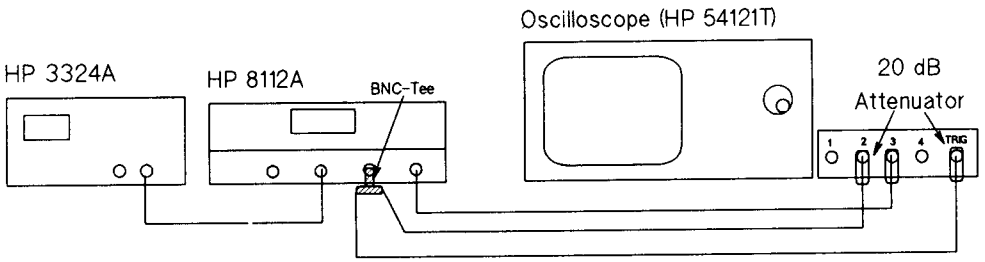


Figure 8-16. Delay Control Verification Test

Procedure

1. Connect the equipment as shown in the setup figure.
2. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	DELC
Transition	Fixed
PER	200 ns
DEL	100 ns
WID	50 ns
HIL	2.00 V
LOL	0.00 V

3. Vary the power supply or HP 3324A between approx 1 volt and 10 volts and verify that oscilloscope display indicates delay time of between 75 ns and 170 ns as shown below.

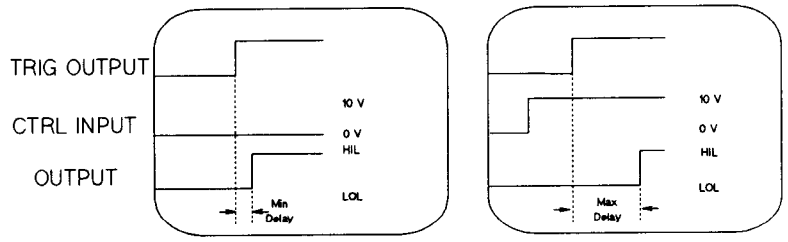


Figure 8-17. Correct Delay Control

4. Connect the HP 8112A output to the counter.
5. Change HP 8112A as follows:

PER	999 ns
WID	300 ms

6. Set the counter as follows:

TIME	A → B
Slopes	A and B
Transition	Positive
Trigger levels	1.0 V
Gate Mode	→ No delay

7. Vary the power supply between approx 1 volt and 10 volts and verify that for the following HP 8112A settings, the range of times displayed agrees with those specified.

HP 8112A setting	Counter reading	
DEL	Low	High
100 ns	75 ns	170 ns
10 μs	1 μs	10 μs
1000 μs	100 μs	1 ms
1000 ms	100 ms	1.0 s

Width Control Verification Test

Characteristics

Pulse Width ratio	1:10
Control Voltage	1.0 V to 10 V
Delay Ranges	10 ns to 1.0 s in eight non-overlapping decade ranges.
Bandwidth	1 kHz

Equipment

- Counter (HP 5335A)
- Variable DC Source (HP 6237B or HP 3324A)
- Cable Assembly BNC (2 off)
- Attenuator 20 dB, 2 W (2 ×)
- BNC to Banana plug adaptor

Test Setup

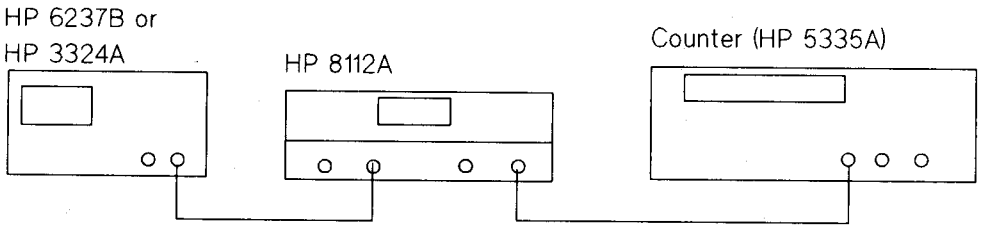


Figure 8-18. Width Control Verification Test

Procedure

1. Connect the equipment as shown in the setup figure
2. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	WIDC
Transition	Fixed
PER	999 ms
DEL	65 ns
HIL	2.00 V
LOL	0.00 V

3. Set the counter to PULSE A
4. Vary the power supply or HP 3324A between approx 1 volt and 10 volts and verify that for the following HP 8112A settings, the pulse width range agrees with those specified.

HP 8112A setting	Counter reading	
WID	Low	High
100 ns	10 ns	100 ns
100 μs	10 μs	100 μs
100 ms	10 ms	100 ms

High-Level Control Verification Test

Characteristics

Control Voltage	−8.0 V to +8.0 V
High-Level Output Window	−8.0 V to +8.0 V into 50Ω, independent of actual low level which is programmable between −8.0 V and +7.95 V in 50 mV steps.
Settling Time	200 μs to settle within 5% of final level.

Equipment

- Oscilloscope (HP 54121T or HP 54503A)
- Pulse/Function Generator (HP 8116A)
- Cable Assembly BNC (5 off)
- Attenuator 20 dB, 2 W (2 ×)

Test Setup

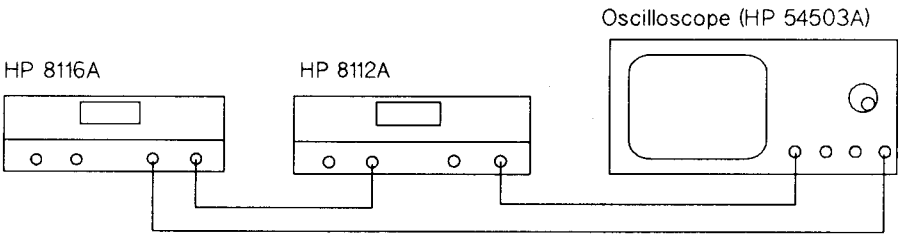


Figure 8-19. High-Level Control Verification Test

Procedure

1. Connect the equipment as shown in the setup figure.
2. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	HILC
Transition	Fixed
PER	200 μs
DEL	65 ns
DTY	50%
LOL	−2.00 V

3. Set up the HP 8116A Pulse/Function Generator as follows:

Output	Sinewave
Frequency	50 Hz
Amplitude	16.0 V
Offset	0.00 V

4. Verify that the High-level output can be varied between +8 V and −8 V while the −2 V level remains unchanged as shown below.

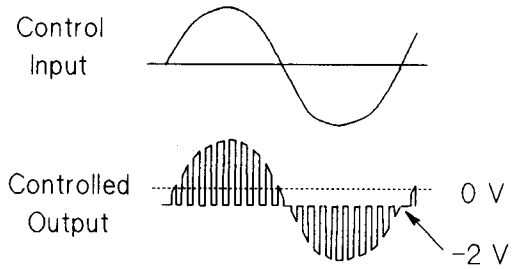


Figure 8-20. Correct High-level Control

5. Set up the HP 8112A as follows:

Trigger Mode	NORM
Transition	Fixed
PER	10.0 ms
DEL	65 ns
WID	10 ns
LOL	−2.00 V
COMPL	On

6. Set up the HP 8116A Pulse/Function Generator as follows:

Output	Squarewave
Frequency	1 kHz
Amplitude	2.0 V
Offset	0.00 V

7. Verify that the scope display indicates a settling time of less than 200 μs as shown below.

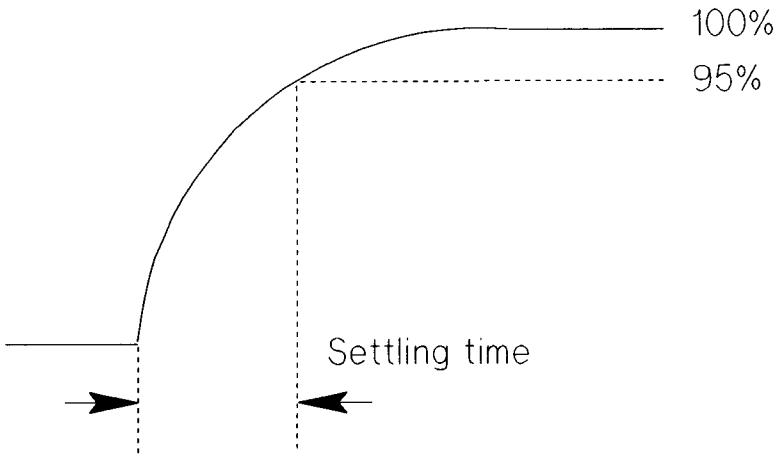


Figure 8-21. Correct Delay Control

Store and Recall Function Test

Characteristics

Nine programmable locations for user preferred mode and parameter settings
One for the standard (switch on) instrument mode and parameter set (RCL 0).
One non accessible location for currently active mode and parameter settings.

Procedure

- Press STO/RCL
- Use right hand **VERNIER** key to obtain display ⊓0
- Press centre **VERNIER** key to recall the standard parameters.
- Alter one of the parameters.
- Press STO/RCL
- Use right hand **VERNIER** key to obtain display ⊔X, where X is any number from 1 to 9.
- Press left hand **VERNIER** key to store the altered parameter.

- Alter one or more other parameters and note the values.
- Select RCL X (the number chosen in step 6).
- Check that the recalled parameter set matches the standard parameter set (RCL0) except for the change made to the standard set in step 4.

HP-IB Verification Test

Test Setup

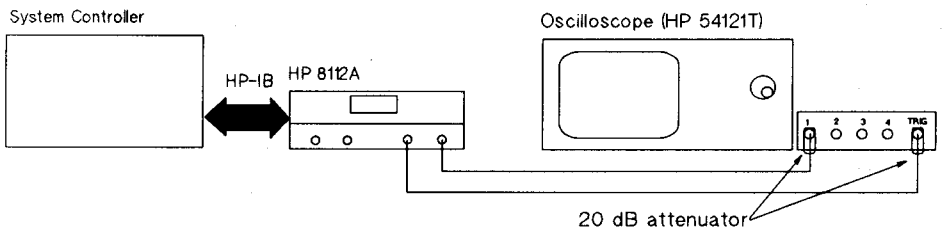


Figure 8-22. HP-IB Verification Test

Equipment

- Controller (HP Series 200/300)
- Oscilloscope (HP 54121T)
- Cable Assembly BNC (2 x)
- HP-IB cable

Procedure

Note

All program statements assume that the HP 8112A is at HP-IB address 12 and that BASIC 5.0/5.1 is being used.

1. Connect the equipment as shown in the setup figure.
2. Use the following program statements to read the HP 8112A Standard Parameter Set:

```
DIM A$[161]          Allocate controller memory to receive HP 8112A status string
REMOTE 712           Set HP 8112A to remote mode
CLEAR 712            Clear HP 8112A status and select standard parameter set
OUTPUT 712;"CST"     Request current settings from HP 8112A
ENTER 712;A$         Read the HP 8112A settings
PRINT A$             Display the HP 8112A settings
```

3. Verify that the result is:

```
W2,D1,PER 1.0 MS,DTY 50 %,HIL 1.0 V,LOL 0.0 V,M1,CT0,T1,L0,C0,BUR 0001 #,
DEL 65 NS,WID 100 US,DBL 200 US,LEE 10 NS,TRE 10 NS
```

4. Use the following program statements to change some instrument settings and then re-read the current settings:

```
DIM B$[161]                    ! Allocate controller memory to
                               ! receive second status string
OUTPUT 712;"W3,PER 10 MS,      ! Change settings
           DTY 10 %,
           W3,HIL 1.5 V,
           D0"
OUTPUT 712;"CST"               ! Request current settings from
                               ! HP 8112A
ENTER 712;B$                   ! Read the HP 8112A settings
PRINT B$                       ! Display the HP 8112A settings
```

5. Verify that the settings are the same as before, except for the following:

```
W3
D0
PER 10.0 MS
DTY 10 %
HIL 1.50 V
```

6. Using the oscilloscope confirm that the HP 8112A output has the following form:

Pulses	Square
Period	10 ms
Duty Cycle	10%
High-Level	+1.5 V
Low-Level	0.0 V

Serial No: _____ Report No: _____ Date: _____

Test Facility :

Test Conditions :

Installed Options : _____

Ambient Temperature : _____ °C

Relative Humidity : _____ %

Line Frequency : _____ Hz

Special Notes :

Serial No: _____ Report No: _____ Date: _____

Test Equipment Used :

Description	Model No.	Serial No.	Trace No.	Cal.Due Date
Counter				
Oscilloscope				
Digital Voltmeter				
Function Generator				
Controller				

Serial No: _____ Report No: _____ Date: _____

Period

Period	Minimum	MEASURED	Maximum	Uncertainty
20 ns	17.0 ns		23.0 ns	
10 μs	9.5 μs		10.5 μs	
10 ms	9.5 ms		10.5 ms	
950 ms	902.5 ms		997.5 ms	

Delay

Delay	Period	Minimum	MEASURED	Maximum	Uncertainty
75 ns	95 ns	-		83.75 ns	
50 μs	95 μs	47.50 μs		52.50 μs	
10 ms	95 ms	9.50 ms		10.50 ms	
900 ms	950 ms	855.0 ms		945.0 ms	

Double Pulse

Period	Double	Width	Minimum	MEASURED	Maximum	Uncertainty
100 ns	20 ns	10 ns	17.0 ns		23 ns	
100μs	20 μs	10 μs	19.0 μs		21.0 μs	
100 ms	20 ms	10 ms	19.0 ms		21.0 ms	
999 ms	800 ms	50 ms	760.0 ms		840.0 ms	

Serial No: _____ Report No: _____ Date: _____

Pulse Width

Pulse

Period	Width	Minimum	MEASURED	Maximum	Uncertainty
100 ns	10 ns	7.5 ns		12.5 ns	

Settings

Period	Width	Minimum	MEASURED	Maximum	Uncertainty
200μs	40 μs	38.0 μs		42.0 μs	
5 ms	1 ms	0.95 ms		1.05 ms	
999 ms	950 ms	902.5 ms		997.5 ms	

Duty Cycle

Duty	Minimum	MEASURED	Maximum	Uncertainty
1.0%	0.9%		1.1%	
10%	9%		11%	
50%	45%		55%	
90%	81%		99%	
99%	89.1%		-	

Output Levels

High

High-Level	Minimum	MEASURED	Maximum	Uncertainty
0.1 V	0.056 V		0.144 V	
0.5 V	0.44 V		0.56 V	
1.0 V	0.92 V		1.08 V	
5.0 V	4.76 V		5.24 V	
8.0 V	7.64 V		8.36 V	

Serial No: _____ Report No: _____ Date: _____

Low

Low-Level	Minimum	MEASURED	Maximum	Uncertainty
−0.1 V	−0.056 V		−0.144 V	
−0.5 V	−0.44 V		−0.56 V	
−1.0 V	−0.92 V		−1.08 V	
−5.0 V	−4.76 V		−5.24 V	
−8.0 V	−7.64 V		−8.36 V	

Transition Times

Fast

Transition	Period	Leading Edge	Trailing Edge	Minimum	MEASURED	Maximum	Uncertainty

Serial No: _____ Report No: _____ Date: _____

Pulse Performance

Fixed Transition

Characteristic	Specification	MEASURED	Uncertainty
Preshoot	≤±10% of amplitude ±10 mV		
Overshoot/Ringing	≤±10% of amplitude ±10 mV		
Settling time	≤105 ns		

Linear Transition

Characteristic	Specification	MEASURED	Uncertainty
Preshoot	≤±5% of amplitude ±10 mV		
Overshoot/Ringing	≤±5% of amplitude ±10 mV		
Settling time	≤107 ns		

Serial No: _____ Report No: _____ Date: _____

Trigger, Gate, External Width and Burst Modes

Trigger	Positive trigger initiates one complete output cycle:	YES/NO
Gate	Each gate leading edge releases train of output pulses, last cycle completed:	YES/NO
External Width	Each ext input pulse enables output pulse of same width:	YES/NO
External Burst	Number of output cycles = set burst number:	YES/NO

Output modes

(MAN) key functioning:	YES/NO
(1 PULSE) key functioning:	YES/NO
Limited output mode functioning:	YES/NO
(COMPL) key functioning:	YES/NO
(DISABLE) key functioning:	YES/NO

Period Control

PER	WID	Minimum and Maximum achieved
100 ns	10 ns	YES/NO
10 μs	1 μs	YES/NO
10 ms	1 ms	YES/NO
1000 ms	100 ms	YES/NO

Serial No: _____ Report No: _____ Date: _____

Delay Control

DEL	Minimum and Maximum achieved
100 ns	YES/NO
10 μs	YES/NO
1000 μs	YES/NO
1000 ms	YES/NO

Width Control

WID	Minimum and Maximum achieved
100 ns	YES/NO
100 μs	YES/NO
100 ms	YES/NO

High-Level Control

−2 V level remains unchanged: **YES/NO**

Settling time correct: **YES/NO**

Store and Recall

STO/RCL key functions correctly: **YES/NO**

HP-IB programming

HP-IB functioning: **YES/NO**

9

Adjustment Procedures

Safety Considerations

Warning

Dangerous voltages, capable of causing serious personal injury, are present in this instrument. Use extreme caution when handling, testing and adjusting.

The adjustments described in this chapter are performed with the instrument switched on and its protective covers removed. Therefore, the adjustments *must* only be carried out by a skilled person, who is aware of the hazards involved, and in the presence of another person who is capable of rendering first aid and resuscitation.

Capacitors inside the instrument may still be charged after the instrument has been disconnected from its external power supply.

Any disconnection of the protective ground connection, inside or outside the instrument, is prohibited, as this is likely to make the instrument dangerous.

Introduction

This chapter describes the adjustment procedures which return the HP 8112A to peak operating condition after repairs are completed. The procedures cover:

- Power Supplies
- Preliminary Adjustments
- Overshoot & Transition Time Adjustment
- Timing
- Shaper and Offset Adjustment
- Slope

Note

Always allow the HP 8112A to warm up for at least 1 hour before starting any adjustment procedures.

The Power Supply and Preliminary adjustment procedure must *always* be carried out after any repairs. If any re-adjustment is required during this procedure then all the remaining procedures must be carried out. If no re-adjustment is required during the Power Supply and Preliminary adjustment procedure then only those procedures which the repair could affect need to be carried out.

Always carry out an adjustment procedure completely and in the order in which it is presented.

If the HP 8112A is very badly out of adjustment, turn A1R413 fully clockwise and all other adjustment potentiometers to their mid position. Then carry out *all* the adjustment procedures.

Some of the adjustment procedures may require components to be changed. These components are summarised in Table 9-1.

Warning  **Do not change a component while power is connected to the instrument.**

Figure 9-8 and Figure 9-9 at the end of the chapter show the locations of all the adjustment points in the instrument.

Table 9-1. Adjustment Procedures - Changeable Components

Procedure	Reference	Range	Description
Overshoot/ Transition Times	A1C409	0 pF (open) – 3.3 pF	Increasing the value decreases transition times and increases overshoot in Fixed mode
	A1C414	as used	Increasing C414 decreases overshoot at amplitudes ≥14 V
	A1C501	27 pF	Pulse performance at ampl. 0.1 V – 0.99 V
	A1C502	120 pF	Pulse performance at ampl. 1 V – 9.99 V
	A1C528	1.5 pF	Pulse shape
	A1C532	0 pF (open) – 33 pF	Increasing C352 decreases transition times and decreases overshoot in Fixed and Linear mode
	A1C535	47 pF	Pulse shape
	A1C541	0.01 pF	Pulse shape
Timing			
Period	A1C200	22 pF	Range capacitor
	A1R211	215Ω	Bias adjustment
	A2VR2	open or 4.3 V	Both influence linearity of
	and		
	A2R62	open or 51.1 kΩ	Period Generator
	A2R2	3.83 kΩ	used to get A2R4 (PER 1 ms Adj.) to it's mid range
	A2R53	3.83 kΩ	used to get A2R3 (PER 20 ms Adj.) to it's mid range

Table 9-1. Adjustment Procedures - Changeable Components (continued)

Procedure	Reference	Range	Description
Delay	A1C220	22 pF	Range capacitor
	A1R225	215Ω	Bias adjustment
	A2VR4	open or 4.3 V	Both influence linearity of
	and		
	A2R64	open or 51.1 kΩ	Delay Generator
	A2R12	3.83 kΩ	used to get A2R14 (DEL 1 ms Adj.) to it's mid range
	A2R55	3.83 kΩ	used to get A2R13 (DEL 20 ms Adj.) to it's mid range
Width	A1C240	22 pF	Range capacitor
	A1R244	215Ω	Bias adjustment
	A2VR3	open or 4.3 V	Both influence linearity of
	and		
	A2R63	open or 51.1 kΩ	Width Generator
	A2R7	4.42	used to get A2R9 (WID 1 ms Adj.) to it's mid range
	A2R54	4.87	used to get A2R8 (WID 20 ms Adj.) to it's mid range
	A2R243	46.4 kΩ endash; 51.1 kΩ	Influences minimum width
	A2R248	1.96 kΩ	Influences minimum width
Shaper and Offset			
Linear	A1R317	1.78 kΩ	Amplitude in linear mode
Fixed	A1R422	5.11 kΩ	Amplitude vernier, 1 V, in fixed mode
	A1R423	1.1 kΩ	A1 TP 10, 2.1 V to 2.6 V
	A1R427	1.1 kΩ	A1 TP 11, 2.1 V to 2.6 V
	A1R437	9.53 – 16.2 kΩ	Increasing the value of R437 Normal/Complement differential offset

Test Equipment

Refer to Chapter 1 *Introduction* for the recommended test equipment and accessories.

Test Preparation

Refer to Chapter 10.1 *Troubleshooting* for instructions on how to open up the HP 8112A instrument and prepare for servicing>

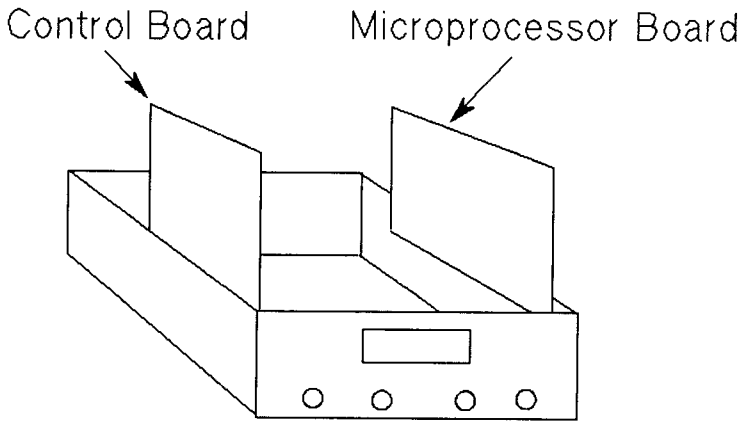


Figure 9-1. Access to the HP 8112A for Adjustments

Power Supplies

Equipment

Digital Voltmeter (HP 3456A)

Procedure

1. Connect the DVM low terminal to the ground testpoint on board A1.
2. Test the supply voltages and, if necessary, make adjustments to achieve the levels given here:

Testpoint	Adjust	Result
A1+15 V	A1R24	+15.000 V ±15 mV
A1−5.4 V	A1R12	−5.40 V ±10 mV
A1+5.0 V	-	+5.050 V ±50 mV
A3+5.0 V	-	+5.150 V ±50 mV
A1+23 V	A1R18	+23.000 V ±50 mV
A1−23 V	A1R19	−23.000 V ±50 mV
A1−15 V	A1R25	−15.000 V ±15 mV

3. Disconnect the DVM.

Pre Adjustments

Equipment

- Oscilloscope (HP 54121T).
- Attenuator 20 dB (3 ×).

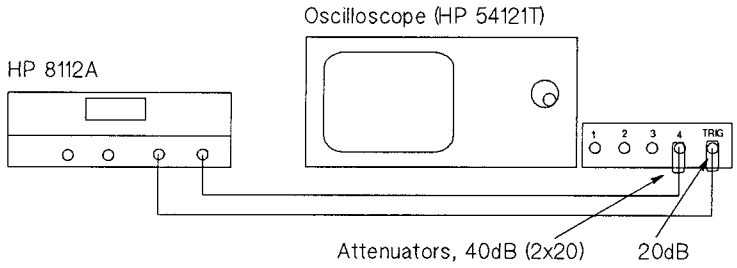


Figure 9-2. Pre adjustments setup

Procedure

Minimum Pulse Droop

1. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	1 ms
DEL	65 ns
DTY	50%
Transition	Linear, Fixed, Gaussian as reqd.
LEE	10 ns
TRE	10 ns
HIL	+4.99 V
LOL	−4.99 V
COMPL	Off
DISABLE	Off (= Enable)
LIMIT	Off

2. Connect the HP 8112A main output to the oscilloscope input 4 via 40 dB (2 × 20 dB) attenuation.
3. Connect TRIGGER OUT of the HP 8112A to the TRIG IN of the oscilloscope, via a 20 dB Attenuator.
4. On the oscilloscope:
   a. Press (Autoscale) and set for 2 V/division.
   b. Set the attenuation factor to 100 and its offset to 0 V.
5. Adjust A1R515 for best pulse droop in all three transition modes.

Normal/Complement

6. Set the HP 8112A Transition to FIXED.
7. Switch the HP 8112A COMPL on and off .
8. Adjust A1R403 for same HIL and LOL on the screen in both modes.

Amplitude/Offset

9. Set the HP 8112A Transition to FIXED.
10. Set the HP 8112A output to COMPL off.
11. Connect the HP 8112A trigger output to the oscilloscope trigger input via 20 dB attenuation.
12. On the oscilloscope press (Autoscale) and set for 2 V/div vertically and 200 μs/div.
13. Adjust A1R410 (amplitude)/R425 (bal.) to achieve an output amplitude of 10 V symmetrical about 0 V.
14. Set the HP 8112A as follows:

Transition	Linear
LEE	5.5 ns
TRE	5.5 ns
LIMIT	Off

15. Adjust A1R318 (amplitude)/R407 (bal.) to achieve an output amplitude of 10 V symmetrical about 0 V.
16. Alter HP 8112A Transition to Gaussian.
17. Adjust A1R418 (amplitude)/R402 (bal.) to achieve an output amplitude of 10 V symmetrical about 0 V.
18. Set up the HP 8112A as follows:

DTY	75%
Transition	Fixed
HIL	0.5 V
LOL	−0.5 V
LIMIT	Off

19. On the oscilloscope, remove one of the 20 dB attenuators from input 4 and set the attenuation factor to 10.
20. Press (Autoscale) and set to 200 mV/division, Ext. trigger, pos.
21. Turn A2R46 fully clockwise.
22. Adjust A2R46 (amplitude) / A1R416 (bal.) for a symetrical 1 V signal.

Overshoot & Transition Time Adjustment

Equipment

- Oscilloscope (HP 54121T).
- Attenuator 20 dB (3 ×).

Procedure

1. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	200 ns
DEL	65 ns
DTY	50%
Transition	Linear
LEE	15.5 ns
TRE	15.5 ns
HIL	8 V
LOL	−8 V
COMPL	Off
DISABLE	Off (=Enable)
LIMIT	Off

2. Connect the HP 8112A main output to the oscilloscope input 4, via two 20 dB attenuators (40 dB).
3. Connect the HP 8112A trigger output to the oscilloscope trigger input via 20 dB attenuation.
4. Press (Autoscale).
5. Adjust A1R535 to give best slope linearity in both COMPL off (=Norm) and COMPL on modes.
6. Set the HP 8112A as follows:

LEE	5.5 ns
TRE	5.5 ns

7. Set the oscilloscope as follows:
   a. Full screen display (center one pulse horizontally and vertically on the screen).
   b. Number of averages to 64.
   c. Attenuation factor to 100.
   d. Select the `Delta V` and turn the voltage markers on.
   e. Set VARIABLE LEVELS = 95 - 105% and press the Auto Level Set.
   f. Center the pulse top vertically (offset = 8 V).
   g. Set V/div to 500 mV.
8. Adjust A1C530 for overshoot < 5% in normal and complement modes.

9. Centre the pulse base line vertically (offset = 8 V) and set
10. Set the VARIABLE LEVELS = −5 to +5%
11. Check overshoot < 5% in normal and complement modes. Re-adjust A1C530 if necessary.
12. Set the HP 8112A as follows:

    Transition Fixed

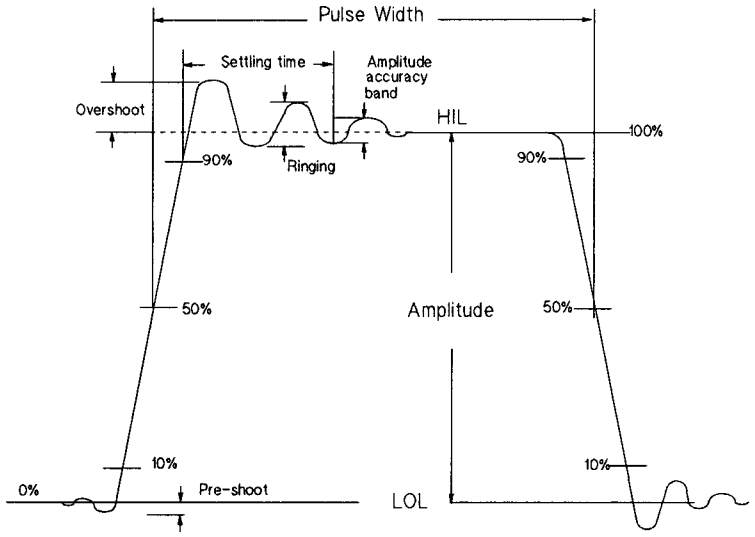


Figure 9-3. Typical Pulse Display

13. Repeat steps 7 to 11 using 90 - 110% / −10 - 10% and adjust A1C410 for overshoot < 10% in both normal and complement modes.
14. Set the HP 8112A as follows:

    LOL −2.0 V
    LIMIT Off

15. Check the overshoot at both HIL and LOL for both Fixed and Linear modes. If necessary, re-adjust A1C530 or A1C410 to achieve the above limits. Repeat steps 1 to 12 if necessary.

Note

The oscilloscope trace flatness error (GaAs input circuit) may affect measurement of pre- and over-shoot

16. Set the HP 8112A as follows:

    Transition Fixed
    HIL +0.5 V
    LOL −0.5 V
    LIMIT Off

17. Remove one of the two 20 dB attenuators and set attenuation factor to 10.

18. Take full screen display on the scope. Check that the transition times <4.8 ns in both normal and complement modes.
19. Set the HP 8112A to Linear transition.
20. Measure the transition times are <6.2 ns.

Note

Transition times can be increased by increasing the overshoot. If Overshoot/Transition times adjustment cannot be achieved within specification, change values of A1C532/C409 (See table 9-1) and repeat steps 1 to 15.

Timing

Equipment

- Counter (HP 5335A)
- Oscilloscope (HP 52141T)

Procedure

Period

1. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	1 ms
DEL	65 ns
DTY	50%
Transition	Fixed
HIL	+3.0 V
LOL	0.0 V
COMPL	Off
DISABLE	Off
LIMIT	Off

2. Set the counter for Period measurement.
3. Connect HP 8112A output via a 50Ω feedthrough to the counter.
4. The typical period accuracy of the period decades is as shown in Figure 9-4.

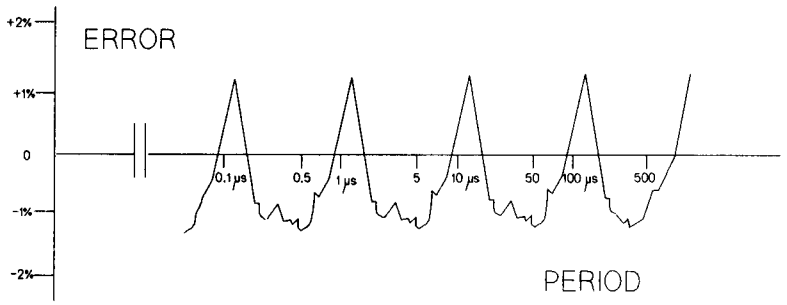


Figure 9-4. Decade Accuracy

5. Adjust the range **high** end with A2R4 for approx 1% above the programmed value (i.e. 1.01ms).
6. Alter HP 8112A PER to 9.99 ms.
7. Adjust the range **low** end with A2R6 for approx 1% above the programmed value (i.e. 10.1ms).
8. Alter HP 8112A PER to 5.0 ms.
9. Check that the **mid-range** deviation is about the same as the low/high range BUT negative. See Figure 9-4.

10. If necessary, repeat steps 1 to 9 to achieve an equal and opposite percentage deviation (up to ±1.5%).

Note

If the adjustment is not possible alter the value of A2VR2/R62 (See table 9-1) and repeat steps 1 to 9.

11. Alter HP 8112A PER to 20 ns.
12. Adjust the range **high** end with A2R3 for 19.5 ns ±0.2 ns.
13. Alter HP 8112A PER to 99.9 ns.
14. Adjust the range **low** end with A2R57 for 102.5 ns ±0.2 ns.
15. Alter HP 8112A PER to 50 ns.
16. Check that the **mid-range** reading for 50 ns ± 2ns.
17. If necessary, repeat steps 1 to 17 and adjust if necessary.

Delay (Double Pulse)

18. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	50 ms
DEL	1 ms
DTY	20%
Transition	Fixed
HIL	+3.0 V
LOL	0.0 V
COMPL	Off
DISABLE	Off
LIMIT	Off

19. Set the counter as follows:

Time interval	A → B
Trigger (both chan)	$\int$, DC, Z = 50 Ω

20. Connect HP 8112A Trigger Output to channel A of the counter.
21. Connect HP 8112A Output to channel B of the counter.

22. Set trigger levels to trigger at about 50% of amplitudes.
23. The typical DELAY (DBL) range characteristic is similar to that shown in Figure 9-5.
24. Adjust the range **high** end with A2R14 for approx 1% above the programmed value (i.e. 1.01ms).
25. Alter HP 8112A DEL to 9.99 ms.
26. Adjust the range **low** end with A2R15 for approx 1% above the programmed value (i.e. 10.1ms).

28. Check that the **mid-range** for 3.5 ms is ± 50 ms.
29. Repeat steps 18 to 28 and re-adjust if necessary.

Note

If the adjustment is not possible add the value of A2VR4/R64 (See table 9-1) and repeat steps 18 to 28.

30. Set the HP 8112A as follows:

PER	200 ns
DBL	20 ns
WID	10 ns
LIMIT	Off

31. Connect HP 8112A Trigger Output via a 20 dB attenuator, to Ext. trigger of the HP 54121A.
32. Connect HP 8112A Output via a 20 dB attenuator to input 4 of the HP 54121A.
33. Press [Autoscale] and adjust A2R13 for 18 ns ± 0.3 ns at 50% of amplitude. See Figure 9-5.

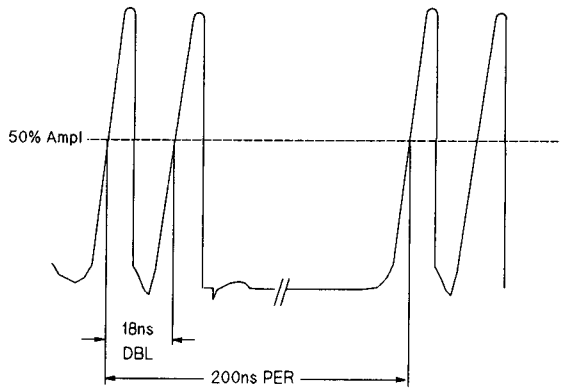


Figure 9-5. Double Pulse Adjustment

34. Alter HP 8112A DBL to 99.9 ns.
35. Adjust A2R61 for 100 ns ±1 ns at 50 % of amplitude.
36. Alter HP 8112A DBL to 50 ns.
37. Check that the **mid-range** reading for 50 ns ± 2ns at 50% of amplitude.
38. If necessary, repeat steps 30 to 37 and adjust if necessary.

Width Adjustment

Equipment

- Counter (HP5335A)
- Oscilloscope (HP 54121T)

Procedure

1. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	20 ms
DEL	65 ns
WID	1 ms
Transition	Fixed
HIL	+3.0 V
LOL	0.0 V
COMPL	Off
DISABLE	Off
LIMIT	Off

2. Set the counter to TIME Interval A→B, COM, A ⨍, B ⨍, Trig level 1.50 V, Z = 50Ω
3. The typical Width range characteristic is shown in Figure 9-4.
4. Connect the HP 8112A main output to channel A of the counter.
5. Adjust the range **high end** with A2R9 for about 1% above programmed value (1.01 ms).
6. Set the HP 8112A WID parameter to 9.99 ms.
7. Adjust the range **low end** with A1R11 for about 1% above programmed value (10.1 ms).
8. Set the HP 8112A WID parameter to 3.5 ms.
9. Check the **mid range** for 3.5 ms ±50 μs.
10. Repeat steps 5 to 9, adjusting again if necessary for the best compromise.

Note

If the adjustment is not possible, alter the value of A2VR3/R63 (see table 9-1). Repeat steps 5 to 9 if neccessary.

11. Set the HP 8112A as follows:

PER	200 ns
WID	10 ns

12. Connect HP 8112A Trigger Output via a 20 dB attenuator, to trigger input of the HP 54121A.
13. Connect HP 8112A Output via a 20 dB attenuator to input 4 of the HP 54121A.

14. On the oscilloscope press (Autoscale) and adjust A2R8 for 10 ns ± 0.2 ns at 50% of amplitude. See Figure 9-5.
15. Alter HP 8112A WID to 99.9 ns.
16. Adjust the **low** range end with A2R59 for 101 ns ±0.2 ns.
17. Repeat previous six steps and re-adjust if necessary.
18. Alter HP 8112A WID to 50 ns.
19. Check that Min. width is 50 ns ± 2ns.

Shaper and Offset Adjustments

Equipment

- Oscilloscope (HP 54503A)
- Digital Voltmeter (HP 3458A)
- Counter HP 5335A
- Pulse/Function Generator (HP 8116A)
- Low pass filter (Refer to Figure 9-6)
  (Only required if DVM does not have built-in 5 Hz low-pass input filter.)

Procedure

Fixed amplitude

1. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	1 ms
DEL	65 ns
WID	500 μs
Transition	Fixed
HIL	+0.99 V
LOL	−0.99 V
COMPL	Off
DISABLE	Off
LIMIT	Off

2. Set the counter to TIME Interval A→B, COM, A $\_\!\!/$, B $\backslash\!\!\_$, Trig level 0 V, Z = 50Ω
3. Connect the HP 8112A main output to channel A of the counter.
4. Observe the counter whilst switching the HP 8112A output from COMPL on and COMPL off.
5. Step the HP 8112A WID with the vernier until the counter reads exactly the same (Exactly 50% Duty Cycle).
6. Set the HP 8112A for STO 9.
7. Disconnect HP 8112A from the counter.
8. Set the HP 8112A as follows:

HIL	+4.99 V
LOL	−4.99 V
LIMIT	Off

9. Set up the DVM to read AC voltages up to 10 V.
10. Connect the HP 8112A main output to the DVM via an exact 50Ω feedthrough (0.1%).
11. Adjust A1R410 until the measured voltage is 5.045 V +20 mV − 0 mV RMS.

12. Make a note of the adjusted voltage.
13. Set the DVM to read DC voltages. If the DVM does not have a built-in filter, use an external low pass filter, as shown in Figure 9-6.

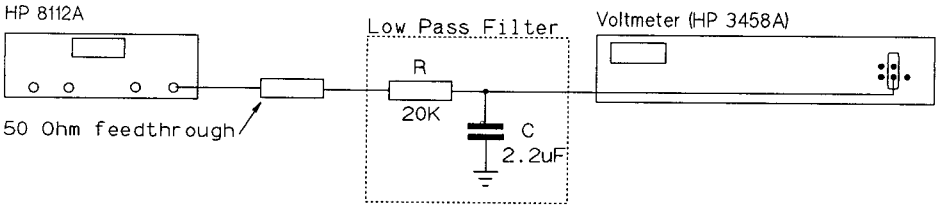


Figure 9-6. Low Pass Filter

14. Switch COMPL on and off, and adjust A1R403 to obtain the minimum amplitude difference between the two modes (Same DVM reading as step 11).
15. Adjust A1R425 for 0 V ±10 mV.

Note

If the adjustments are not possible, change value of A1R437 (see table 9-1) and repeat steps 1 to 15.

16. Set the HP 8112A as follows:

HIL	+0.5 V
LOL	−0.5 V

17. Set up the DVM to read AC voltages up to 10 V. Switch filter OFF or remove external filter.
18. Adjust A2R46 for 0.506 V ±5 mV RMS.
19. Use the DVM built-in filter and set the DVM to read DC voltages. If the DVM does not have a built-in filter, use an external low pass filter, as shown in Figure 9-6.
20. Adjust A1R416 for 0 V ±5 mV.

Linear Amplitude

21. Set up the HP 8112A as follows:

Transition	Linear
HIL	+4.99 V
LOL	−4.99 V

22. Switch COMPL on and off, and adjust A1R407 to obtain the minimum amplitude difference between the two modes 0 V ± 10 mV (Same DVM reading).
23. Set up the DVM to read AC voltages up to 10 V. Switch filter OFF or remove external filter.

24. Adjust A1R318 for 5.045 V −0/+20 mV RMS. Same DVM reading as in FIXED transition mode.

Gauss Amplitude

25. Set the HP 8112A transition to GAUSS.
26. Adjust A1R418 for 5.045 V −0/+20 mV RMS. Same DVM reading as in FIXED and LINEAR transition modes.
27. Use the DVM built-in filter and set the DVM to read DC voltages. If the DVM does not have a built-in filter, use an external low pass filter, as shown in Figure 9-6.
28. Switch COMPL on and off, and adjust A1R402 to obtain the minimum amplitude difference between the two modes 0 V ± 10 mV (Same DVM reading).
29. Set up the HP 8112A as follows:

Transition	Fixed
HIL	+8.0 V
LOL	−8.0 V
LIMIT	Off

30. Set up the DVM to read AC voltages up to 20 V. Switch filter OFF or remove external filter.
31. Check that the amplitude for FIXED, LINEAR and GAUSS transition mode is 8.080 V −0/+40 mV RMS.
32. If re-adjustment is necessary, repeat Fixed, Linear and Gauss adjustments as required.

Offset

33. Set up the HP 8112A as follows:

HIL	+8.00 V
LOL	+7.90 V

34. Set up the DVM to read DC voltages up to 10 V.
35. Connect the HP 8112A main output via an exact 50 Ω 0.1% feedthrough terminator to the DVM, and enable the DVM built-in filter. If the DVM does not have a built in filter, use a low-pass filter as shown in Figure 9-6.
36. Adjust A2R42 for 7.95 V ± 10 mV.
37. Set up the HP 8112A as follows:

HIL	−7.90 V
LOL	−8.00 V

38. Check accuracy of negative offset. DVM reading −7.95 V ± 30 mV.
39. Re-adjust A2R42 if necessary.

HIL C

40. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	HILC
PER	1 ms
DEL	65 ns
WID	500 μs
Transition	Fixed
HIL	+8.00 V
LOL	0.0 V
COMPL	Off
DISABLE	Off
LIMIT	Off

41. Connect the HP 8112A output via an exact 50 Ω 0.1% feedthrough, to the oscilloscope (HP 54503A).
42. Adjust A2R50 for 0 V amplitude (no signal).
43. Set the HP 8116A Signal Generator as follows:

Trigger Mode	NORM
FREQ	2 Hz
AMPL	8 V, symetrical
DISABLE	Off

44. Connect the signal to the HP 8112A CTRL INPUT.
45. Adjust A1R506 for minimum change in the waveform baseline.

Slope

Equipment

- Oscilloscopes (HP 54121T/HP 54503A)
- 20 dB attenuators (3 ×)

Procedure

1. Set up the HP 8112A as follows:

Trigger Mode	NORM
Control Mode	Off
PER	5 ms
DEL	65 ns
DTY	50%
Transition	Linear
LEE	100 μs
TRE	500 μs
HIL	+4.00 V
[illegible]	[illegible]
COMPL	Off
DISABLE	Off
LIMIT	Off
STO	1

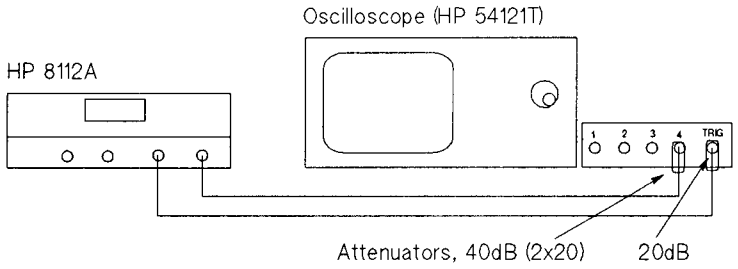


Figure 9-7. Slope test setup

2. Set the HP 8112A as follows:

LEE	999 μs
STO	2

3. Set the HP 8112A as follows:

LEE	500 μs
STO	5

4. Set the HP 8112A as follows:

TRE	100 μs
STO	3

5. Set the HP 8112A as follows:

TRE 999 μs
STO 4

6. Set the HP 8112A as follows:

   RCL 1

7. Connect the HP 8112A Trigger Output to the oscilloscope Trigger Input.
8. Connect the HP 8112A output to input 4 of the oscilloscope.
9. Set the oscilloscope to display one pulse using the `Delta t` mode.
10. Observe LEE on the oscilloscope (10% - 90% of amplitude). Adjust A2R37 for about 0.5% below programmed value (i.e. 99.5 μs).
11. Set the HP 8112A as follows:

    RCL 2

12. Observe LEE on the oscilloscope and adjust A2R32 for about 0.5% below programmed value (i.e. 995 μs).
13. Repeat last two steps and re-adjust if necessary.
14. Set the HP 8112A as follows:

    RCL 5

15. Check LEE on the oscilloscope for < 510 μs and > 480 μs.
16. Step LEE up and down using the vernier keys and observe the oscilloscope for $< 2\%$ deviation.
17. Set the HP 8112A as follows:

    RCL 3

18. Observe TRE on the oscilloscope (90% - 10% of amplitude) and adjust A2R38 for about 0.5% below programmed value (i.e. 99.5 μs).
19. Set the HP 8112A as follows:

    RCL 4

20. Observe TRE on the oscilloscope and adjust A2R35 for about 0.5% below programmed value (i.e. 995 μs).
21. Repeat last two steps and re-adjust if necessary.
22. Set the HP 8112A as follows:

    RCL 5

23. Check TRE on the oscilloscope for < 510 μs and > 480 μs.
24. Step TRE up and down using the vernier keys and observe the oscilloscope for $< 2\%$ deviation.
25. Set the HP 8112A as follows:

LEE	1 ms
TRE	1 ms

26. Observe TRE on the oscilloscope and adjust A2R27 for 1.000 ms ±5 μs.
27. Switch COMPL on and off and adjust A2R27 for best compromise 1.000 ms ±5μs.
28. Set the HP 8112A as follows:

PER	50 ms
LEE	10 ms
TRE	10 ms

29. Observe LEE and TRE on the oscilloscope and adjust A2R28 whilst switching COMPL on and off, and adjust for best compromise 10.00 ms ±50 μs.
30. If the last two steps cannot be achieved, repeat steps 11 to 26 for the minimum difference between LEE and TRE.
31. Set the HP 8112A as follows:

PER	500 ns
LEE	100 ns
TRE	100 ns

32. Connect the HP 8112A to the HP 54121A oscilloscope using two 20 dB attenuators.
33. Set the oscilloscope to display one pulse and set it to measure Rise/Fall time.
34. Observe the oscilloscope and adjust A1C304 for best compromise of LEE and TRE (100 ns ±2 ns).
35. Set the HP 8112A as follows:

LEE	49.9 ns
TRE	49.9 ns

36. Observe the oscilloscope and adjust A2R26 for best compromise of LEE and TRE (50 ns ±1 ns).

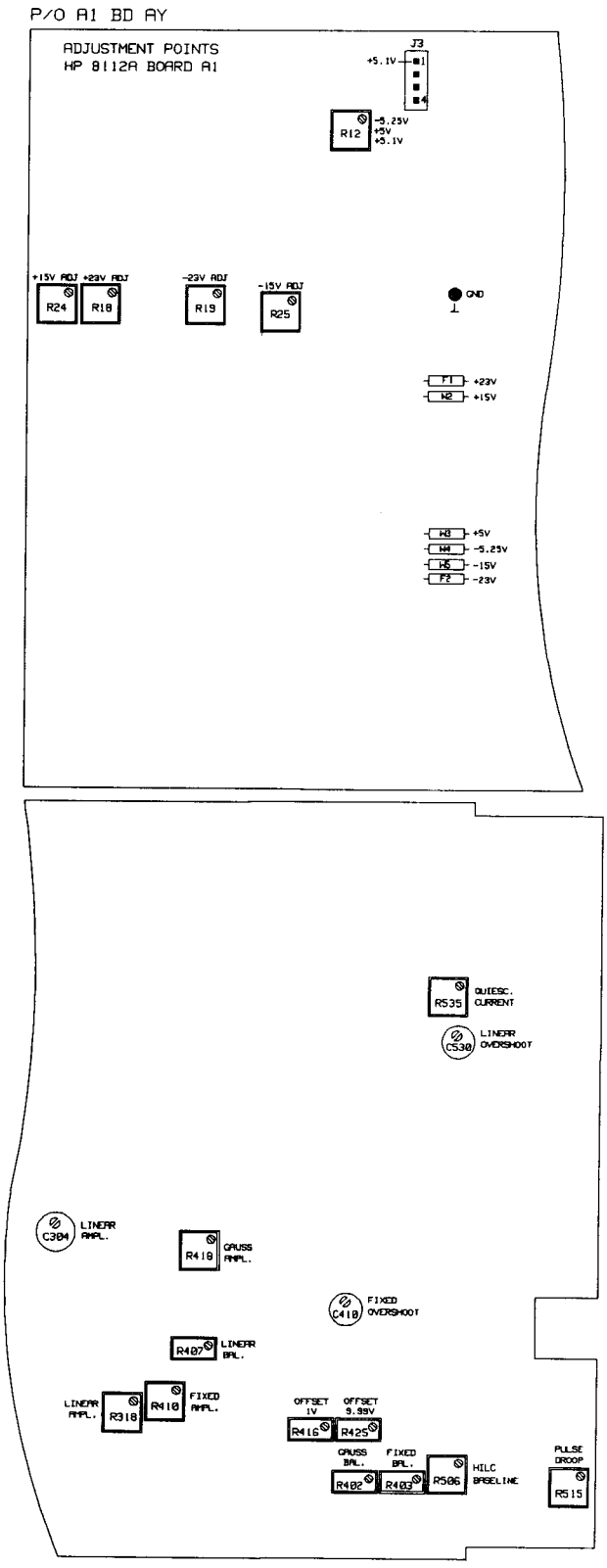


Figure 9-8. Adjustment Points on the Main Board A1

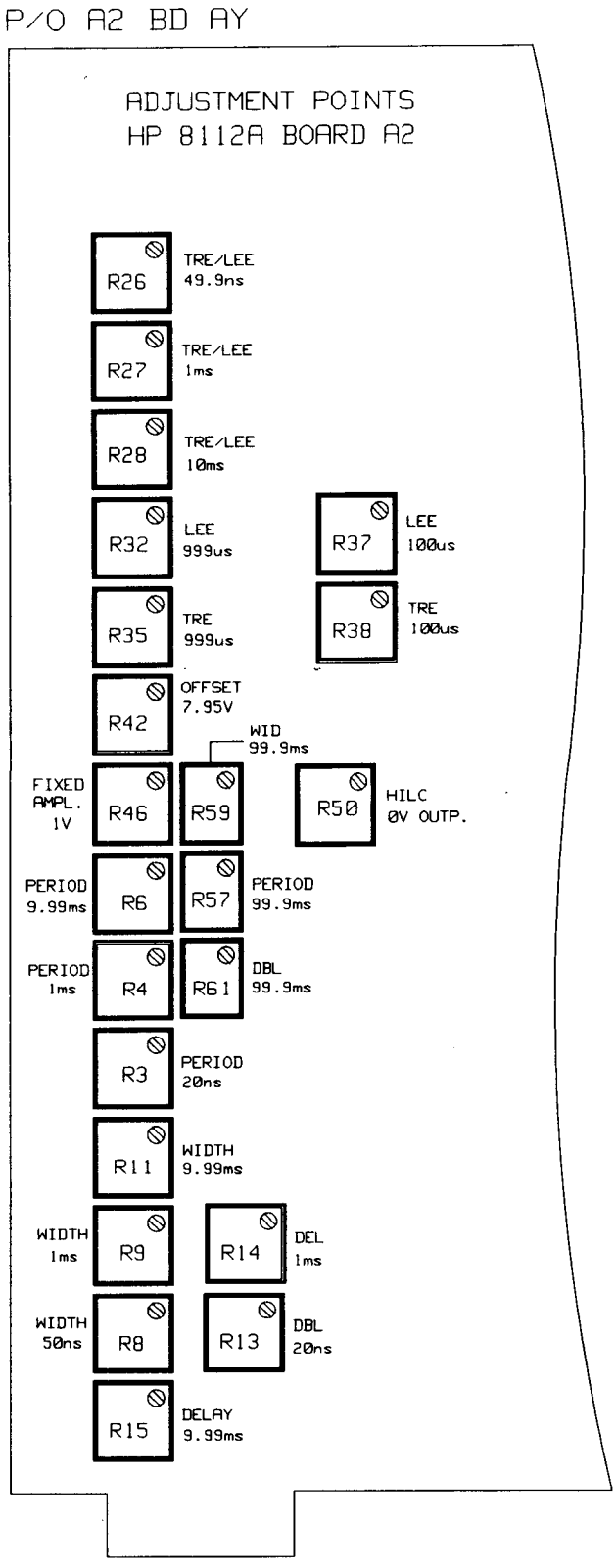


Figure 9-9. Adjustment Points on the Control Board A2

10

Introduction to Servicing

Safety Considerations

Warning

Dangerous voltages, capable of causing serious personal injury, are present in this instrument. Use extreme caution when handling, testing and adjusting.

The servicing described in the following chapters is performed with the instrument switched on and its protective covers removed. Therefore, servicing *must* only be carried out by a skilled person, who is aware of the hazards involved, and in the presence of another person who is capable of rendering first aid and resuscitation.

Capacitors inside the instrument may still be charged after the instrument has been disconnected from its external power supply.

The HP 8112A contains static-sensitive devices. Ensure that "static-safe" precautions are taken to prevent electro-static discharge when the instrument covers are removed.

Safety Check

The following safety checks must be carried out after any servicing is completed:

1. Disconnect the power cord from the external voltage supply.
2. Inspect the interior of the instrument for any signs of abnormal overheating or arcing, such as:
   - Discolored circuit board
   - Discolored components
   - Damaged insulation

   If a problem exists, it *must* be investigated and fixed before proceeding.
3. Check the case to power-cord ground-pin continuity in accordance with IEC & VDE. Flex the power cord during the measurement to check for any intermittent discontinuity. If a problem exists, it must be investigated and fixed before proceeding.
4. Check the internal ground connections between circuit boards and the instrument frame. If a problem exists, it must be investigated and fixed before proceeding.

5. Check that the case is isolated from the power-cord power-pins in accordance with IEC & VDE. If a problem exists, it must be investigated and fixed before proceeding.
6. Check that the correct line fuse is fitted.
7. Check that all safety covers are fitted.
8. Check that all inter-connecting co-axial and flat cables are properly connected.

10. Check that the heatsink connections between the main board and the front frame member are secure.
11. Inform Hewlett-Packard of any repeated failures of any of the checks, or any other safety features.

General

The servicing information is divided into chapters as summarised here:

Instrument Overview	This chapter deals with the overall instrument and is intended to help you to isolate a fault at a functional level. You can then proceed to the appropriate chapter which covers that function in more detail.
Servicing the Power Supply	This chapter deals with the power supply, including rectification, regulation, voltage and current sensing and power-down detection.
Servicing the Time and Slope Generator	This chapter covers the trigger-input circuits, slope generator IC, timing IC, error feedback circuit and the vernier feedback circuit.
Servicing the Shaper and Output Amplifier	This chapter covers the shaper IC, amplitude modulator, current mirror, pre-attenuator, signal output amplifier, output attenuator and the trigger-output amplifier.
Servicing the Standard Control Board	This chapter covers the byte-offset latches, Digital to Analog Converters, timer, reference circuits, and the width-vernier current source.
Servicing the Microprocessor and Frontpanel	This chapter covers the microprocessor board including ROM, RAM, HP-IB interfacing, address decoding and the RAM battery supply. It also covers the keyboard and display board which make up the frontpanel.

Each of these chapters contains an explanation of the theory of operation, a troubleshooting guide and circuit schematics. Component layouts for each board assembly are also provided. The five board assemblies contained in the HP 8112A are listed in Table 10-1 which lists the servicing chapters applicable to each board.

Table 10-1.
HP 8112A Board Assemblies & Servicing Chapters

Assembly	Reference	Chapter(s)
Main Board	A1	10.2, 10.3, 10.4
Control Board	A2	10.5, 10.6
Microprocessor Board	A3	10.7
Keyboard	A4	10.7
Display Board	A5	10.7

10.1

Instrument Overview and Troubleshooting Guide

Theory of Operation

The block diagram in Figure 10.1-1 shows the HP 8112A at a functional level.

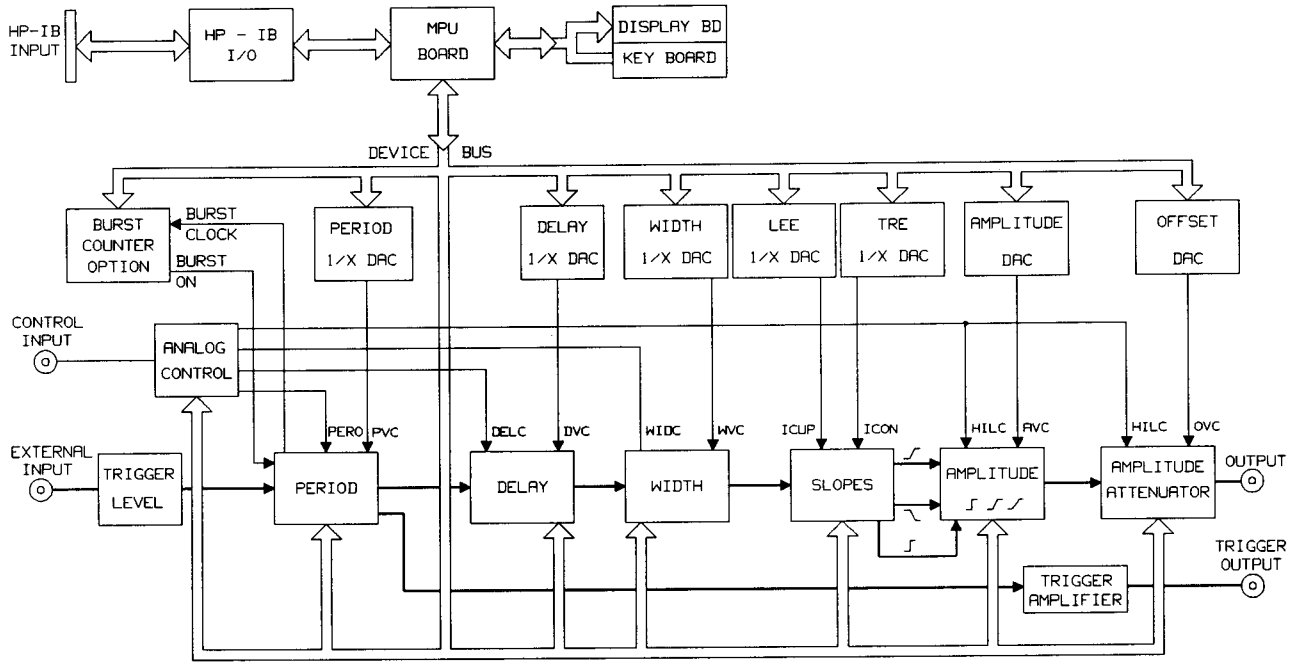


Figure 10.1-1. HP 8112A Functional block diagram

The microprocessor controls the operation of the instrument by reading inputs from the front panel keyboard or the HP-IB, and sending the appropriate data to the Digital-to-Analog Converters (DACs) which control the generator hardware. It also updates the front panel LEDs and display in response to the keyboard and HP-IB inputs.

The generator hardware contains three specially developed HP ICs:

Timing IC — This is used as triggerable pulse generators. Three ICs are used, taking the external signal applied to the Control Input and applying Period, Delay and Width control in successive stages to provide pulses for the Slope IC.

Slope IC	This is used as a pulse generator up to 50 MHz, with the output either continuous, gated or triggered. It is also used as a burst generator.
Shaper IC	This is used as a linear preamplifier and final output pulse shaper.

The ICs and their supporting circuits are covered in more detail in the relevant parts of the later chapters, however, the IC pin identities are given in Figure 10.1-2.

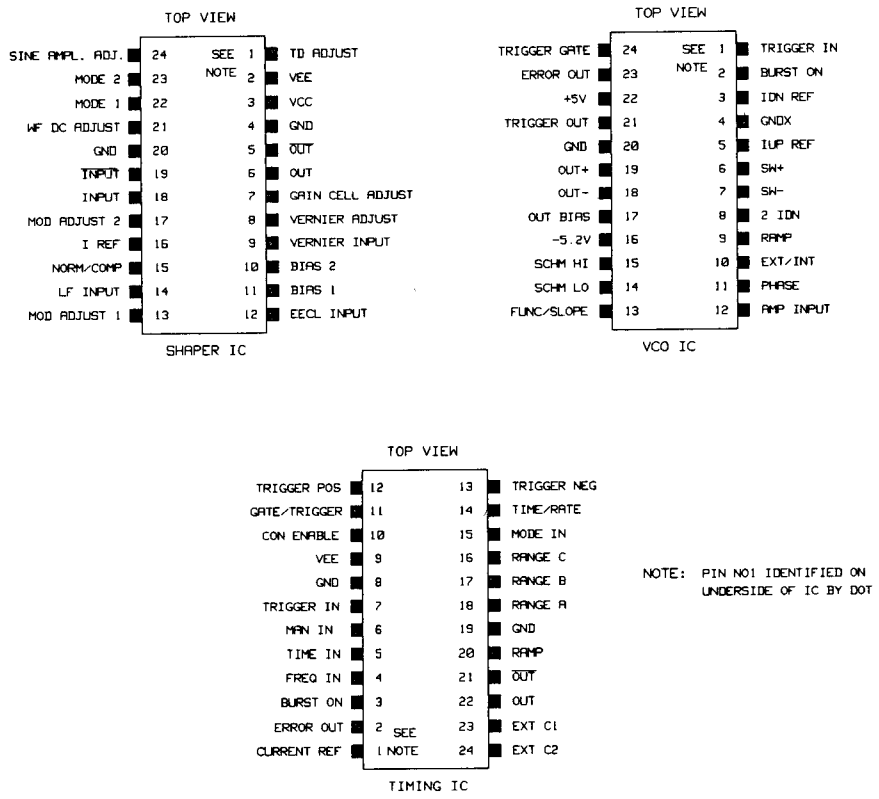


Figure 10.1-2. Custom ICs used in the HP 8112A

Trouble shooting

Every time the instrument is switched on, or when an EST command is received on the HP-IB, the HP 8112A executes a self-test. If a fault is detected an error code is displayed, otherwise the instrument is ready for operation. The error code can be used to locate the fault by referring to the following flowchart. If more than one fault exists, only the first one is detected and displayed. After this is successfully repaired, the self-test will be able to proceed further and detect other remaining faults.

Preparing the HP 8112A for servicing

The HP 8112A contains static-sensitive devices. Ensure that "static-safe" precautions are taken to prevent electro-static discharge when the instrument covers are removed.

1. Remove the rear of the instrument by unscrewing the two TORX fastening screws.
2. Remove the single screw securing the instrument's case underneath the instrument.
3. Remove the case by sliding it backwards. You may need to use a screwdriver in one of the case ventilation holes to gently lever the case back. It is held tightly by the RFI seals at the front of the frame.
4. Remove the four screws securing the microprocessor board.
5. Lift the microprocessor board and stand it vertically by placing the cut-outs on the edge of the board over the locating lugs on the inside of the right-hand side-panel (as seen from the front of the instrument).
6. Remove the screen covering the control board.
7. Lift the control board and stand it vertically on the inside of the left-hand side-panel.

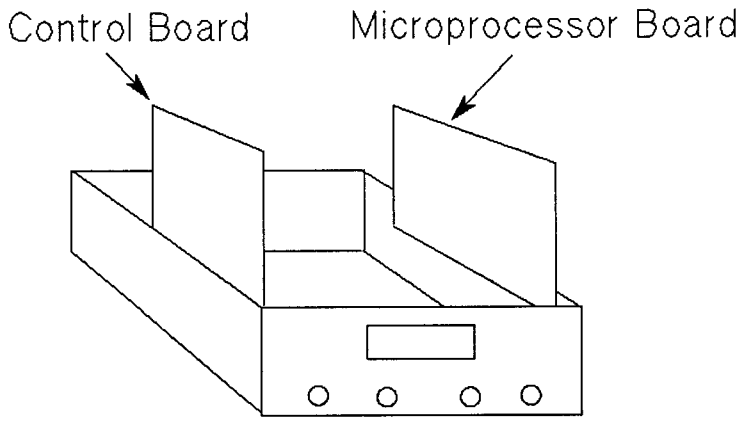
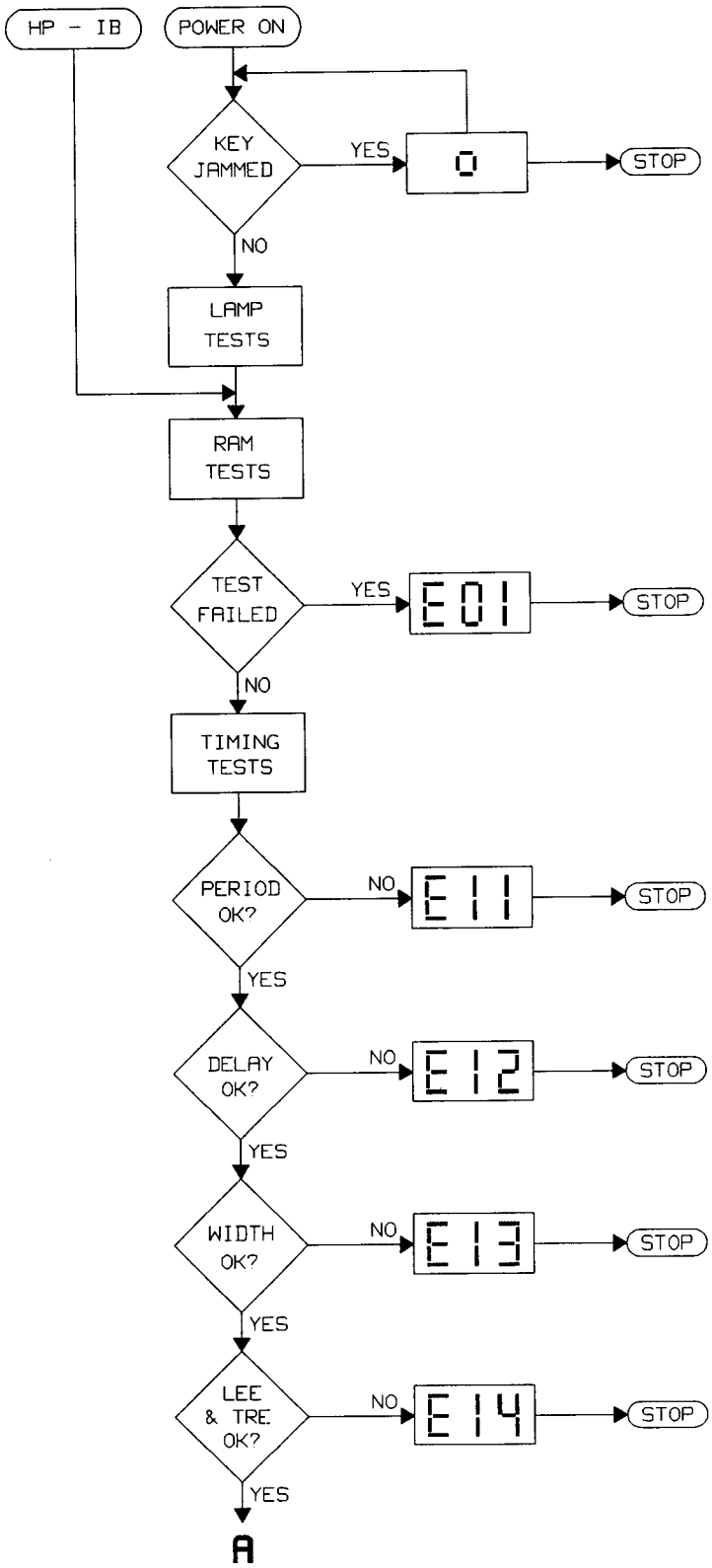


Figure 10.1-3. HP 8112A in its servicing position


HP - IB
POWER ON
KEY JAMMED
YES
0
STOP
NO
LAMP TESTS
RAM TESTS
TEST FAILED
YES
E01
STOP
NO
TIMING TESTS
PERIOD OK?
NO
E11
STOP
YES
DELAY OK?
NO
E12
STOP
YES
WIDTH OK?
NO
E13
STOP
YES
LEE & TRE OK?
NO
E14
STOP
YES
A

Key Jammed

0

Possible faulty A3 Processor Board (ROM reset circuit) or power supply fault (restart signal)

A front panel key is stuck. The instrument cannot be used until it is freed.

RAM Test

E01

The microprocessor is unable to load a test pattern into the RAMs U10/U11 and verify it. In order to avoid influence from the control or main board, remove the device-bus cable from the main board A1 at connector J2 (See Chapter 10.2. mainlayout\) and from the control board A2 at connector J5 (See Chapter 10.5.

Timing Tests

E11

Period generator U200 is not able to supply a period of 1 ms in MAN mode with a software trigger. Possible failure of Period control circuit U4, U7, Error feedback U141 or trigger input stage U101, LD0 and Q100. See Chapter 10.3.

E12

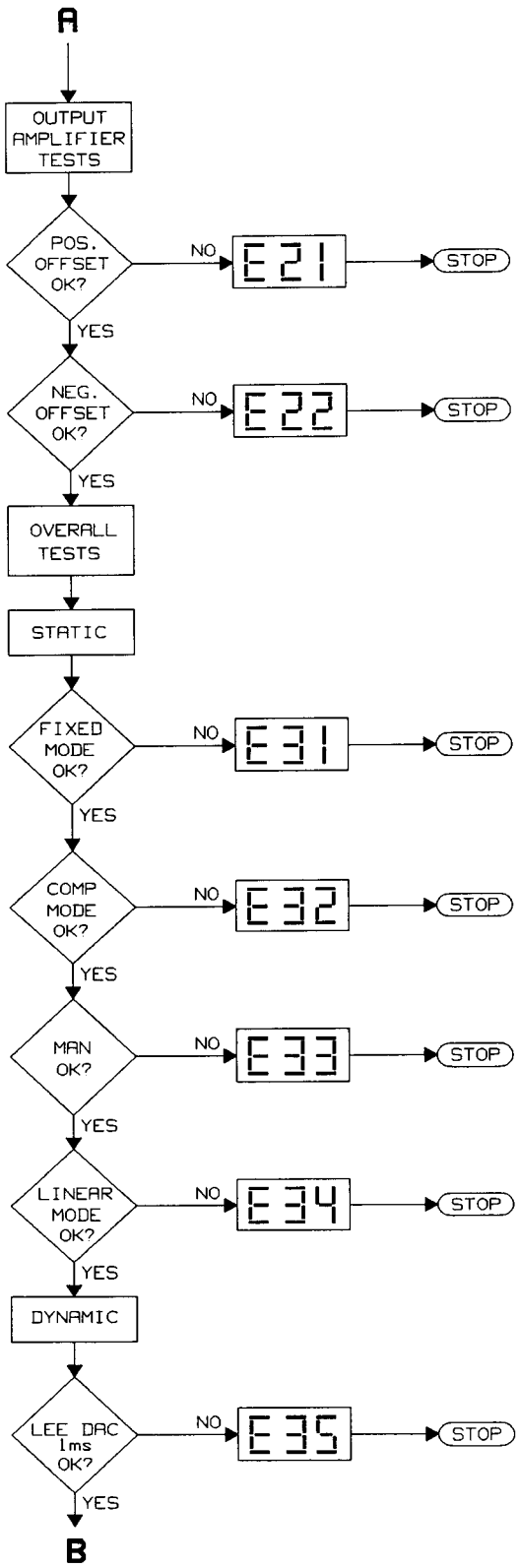
Delay generator U220 is not able to supply a pulse of 3 ms when in positive trigger mode and triggered via the Period generator. Possible failure of Delay control circuit U5, U7, Error feedback U140 or level shifter Q200. See Chapter 10.3.

E13

Width generator U240 is not able to supply a pulse of 9 ms when in positive trigger mode and triggered via the Delay generator. Possible failure of Width control circuit U6, U8, Error feedback U141 or level shifter Q220. See Chapter 10.3.

E14

The Slope IC U301 in function mode, is unable to produce pulses with a period of 2.5 ms and rise/fall times of 1 ms. Possible failure of Slope control circuit U12, U13, U14 or U302, Slope range switching circuit Q305 to Q309, U300, or reference circuit U320. See Chapter 10.3.


A
OUTPUT AMPLIFIER TESTS
POS. OFFSET OK?
NO
E 21
STOP
YES
NEG. OFFSET OK?
NO
E 22
STOP
YES
OVERALL TESTS
STATIC
FIXED MODE OK?
NO
E 31
STOP
YES
COMP MODE OK?
NO
E 32
STOP
YES
MAN OK?
NO
E 33
STOP
YES
LINEAR MODE OK?
NO
E 34
STOP
YES
DYNAMIC
LEE DAC lms OK?
NO
E 35
STOP
YES
B

Output Amplifier Tests

E21

Offset generator is unable to produce positive offset. Possible failure in Output amplifier or offset control circuit U17 to U19, U20 to U22, or U27. See Chapter 10.4.

E22

Offset generator is unable to produce negative offset. Possible failures as E21.

Overall Tests, Static

These tests check pulse generation using the level check circuits.

E31

When software triggered (low), a fixed mode negative pulse is not detected. Possible failure in signal transfer between:

- Period generator U200
- Delay generator U220
- Width generator U240
- Slope generator U301
- Shaper IC U401

and output pre-attenuator and amplifier. Refer to Chapters 10.5, 10.3 and 10.4.

E32

When software triggered (low), a fixed mode positive pulse is not detected. Possible failures as in E31.

E33

When software triggered (high), a fixed mode negative pulse is not detected. Possible failures as in E31.

E34

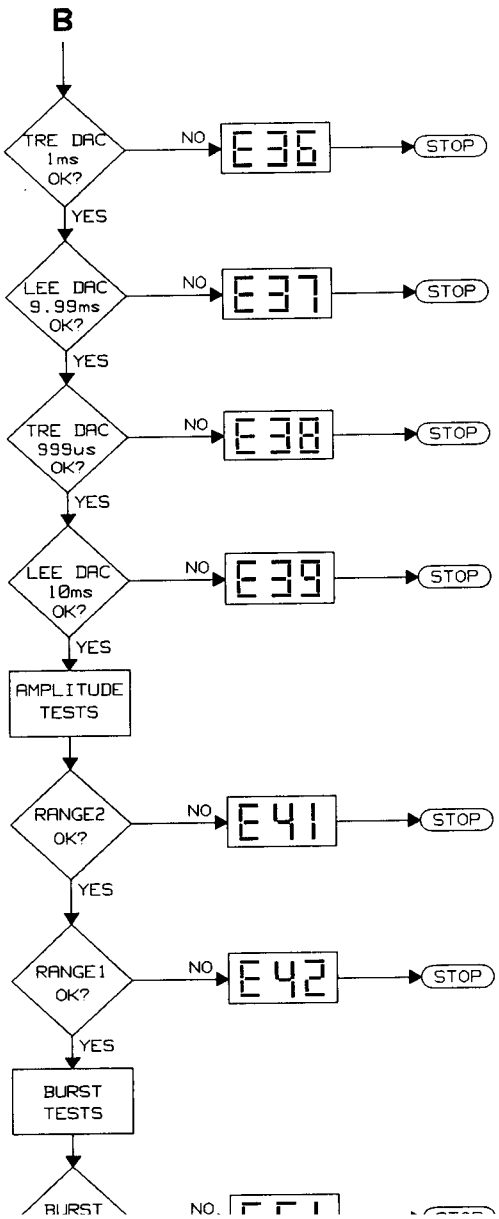
When software triggered (low), a linear mode negative pulse is not detected. Possible failures as in E31.

Overall Tests, Dynamic

These tests check the accuracy of the output pulse rise and fall times in normal output mode.

E35

When software triggered (high), rise time of 1 ms (Range 6) out of limits. Possible faults in leading edge slope control circuit U12, U14 or U302. See Chapter 10.5.


B
TRE DAC 1ms OK?
NO
E36
STOP
YES
LEE DAC 9.99ms OK?
NO
E37
STOP
YES
TRE DAC 999us OK?
NO
E38
STOP
YES
LEE DAC 10ms OK?
NO
E39
STOP
YES
AMPLITUDE TESTS
RANGE2 OK?
NO
E41
STOP
YES
RANGE1 OK?
NO
E42
STOP
YES
BURST TESTS
BURST
NO.

E36

When software triggered (low), fall time of 1 ms (Range 6) out of limits. Possible faults in trailing edge slope control circuit U13, U14 or U302. See Chapter 10.5.

E37

When software triggered (high), rise time of 9.99 ms (Range 6) out of limits. Possible faults as in E35.

E38

When software triggered (low), fall time of 9.99 ms (Range 6) out of limits. Possible faults as in E35.

E39

When software triggered (high), rise time of 10 ms (Range 7) out of limits. Possible faults as in E35.

Amplitude Tests

E41

Amplitude range 2 (9.99 V) not possible. Possible faults:

- Pre-attenuator circuit
- Amplitude control circuit U23 to U25
- Offset control circuit U20 to U22

See Chapters 10.5 and 10.4.

Shaper Output State Test

E42

Amplitude range 1 (1 V) not possible. Possible faults as in E41.

Burst Tests

HP 8112A set to produce a burst of 10 pulses of period 250 μs.

E51

Burst counter supplies less than 10 pulses. Possible fault in Burst flip-flop U201 or Burst control circuit U102 to U112. Refer to Chapter 10.6.

E52

Burst counter produces more than 10 pulses. Possible faults as in E51.

10.2

Servicing the Power Supply

Theory of Operation

Introduction

The HP 8112A power supply unit occupies part of the main board A1 and consists of the following four parts, as shown in Figure 10.2-1:

- Line voltage selector and transformer
- Voltage rectifiers and regulators
- Voltage and current sensing circuits
- Power-down detection circuit

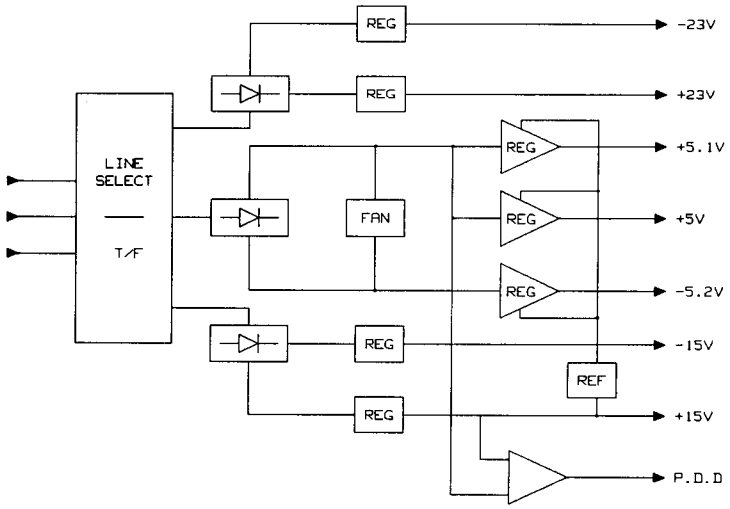


Figure 10.2-1. Power Supply block diagram

Line Voltage Selector and Transformer

Refer to Figure 10.2-2. The line-voltage selector-switches, S2 and S3, connect the incoming line-voltage lines to an appropriate pair of transformer inputs. The transformer provides six ac outputs and an earth line to the bridge rectifiers.

Bridge Rectifiers and Regulators

There are three bridge rectifiers, all modular and therefore replaceable:

Table 10.2-1. Power supply rectifiers

Rectifier	Output
CR1	±5 V DC
CR2	±23 V DC
CR3	±15 V DC

The raw voltage outputs are all smoothed by capacitors, as shown in Figure 10.2-3. The following supplies are then fed to voltage regulators, with potentiometers to adjust the final voltage level:

Table 10.2-2. Regulated voltage supplies

Supply	Regulator	Adjustor
+23 V	U3	R18
-23 V	U4	R19
+15 V	U5	R24
-15 V	U6	R25

Voltage and Current Sensing Circuits

The smoothed ±5 V DC outputs of CR1, which drive the fan, also provide the basis for the voltage and current sensing circuits which control the +5.1 V, +5 V and -5.4 V supplies.

+5.1 V supply

A reference voltage of 5.1 V is obtained from the +15 V regulated supply, using zener diode VR1 (6.2 V),R11 and R12. U1C compares the +5.1 V supply with this reference voltage and drives the regulator transistor Q1, via driver transistor Q2, until there is zero difference.

If the current drawn from the +5.1 V supply is excessive, a distinct voltage drop develops across R2. U1D detects this and its output switches toward the negative supply. This forward-biases diode CR8, switches off Q2 and Q1, and hence the +5.1 V supply is withdrawn.

+5 V supply

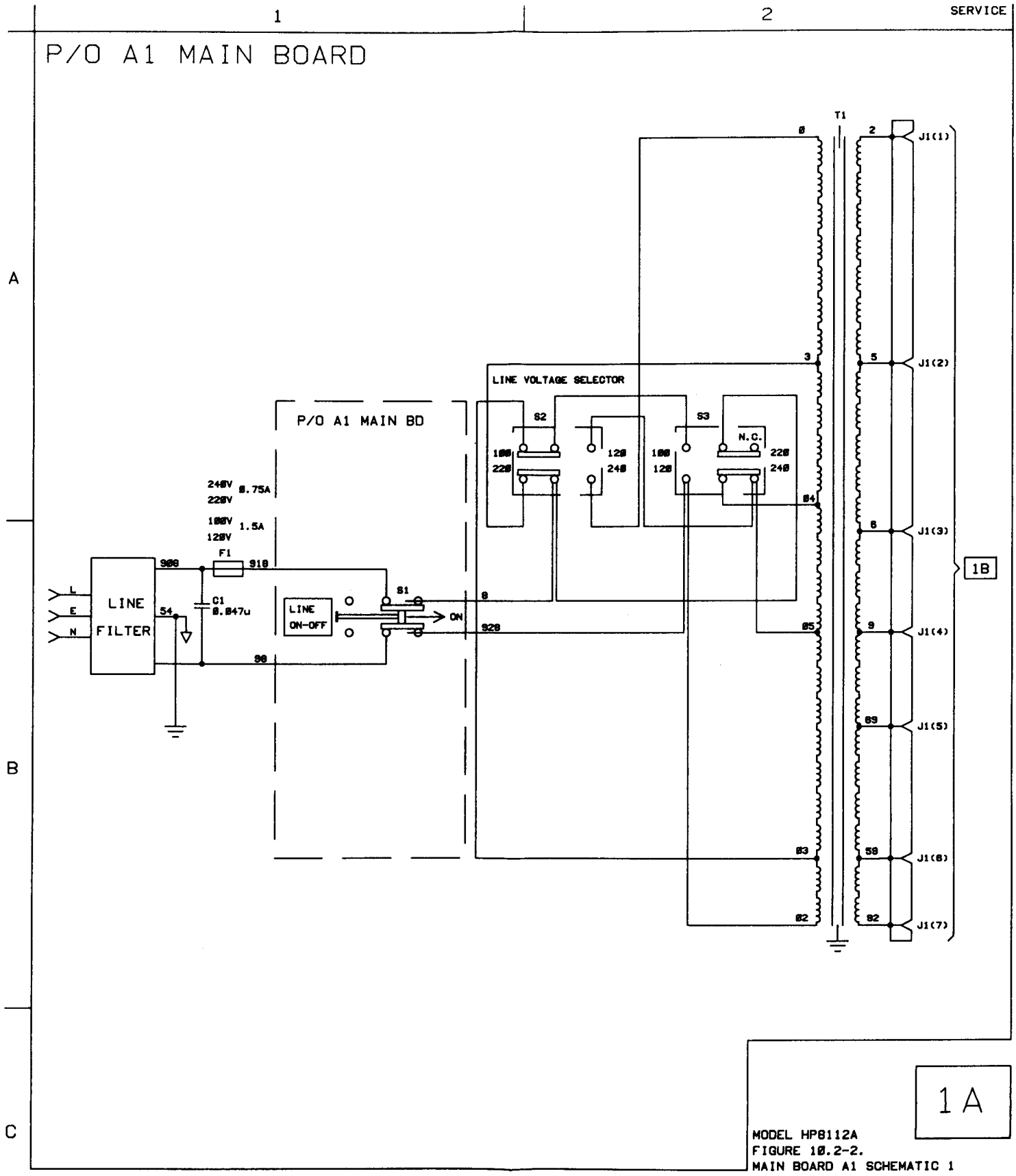
The same principles of operation apply to the +5 V voltage regulator, U2C, and current sensor, U2B. The 5 V reference is obtained from the 5.1 V reference via R13.

-5.4 V supply

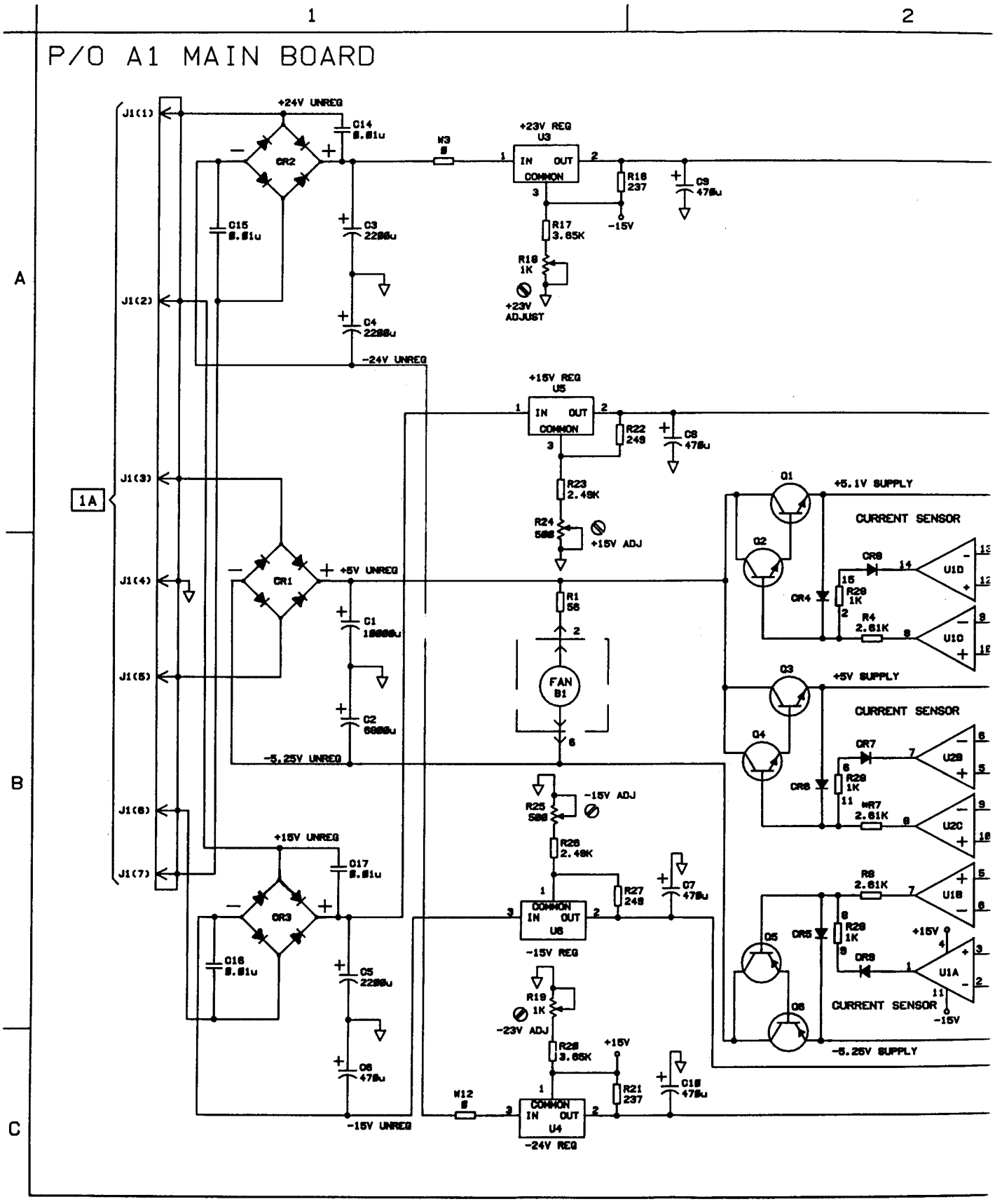
The -5.4 V reference is obtained from the 5 V reference using U2D as an inverter with a gain of 1.08. The voltage regulator U1B and the current sensor U1A operate as above except that the comparator output is normally negative and switches positive to withdraw the supply.

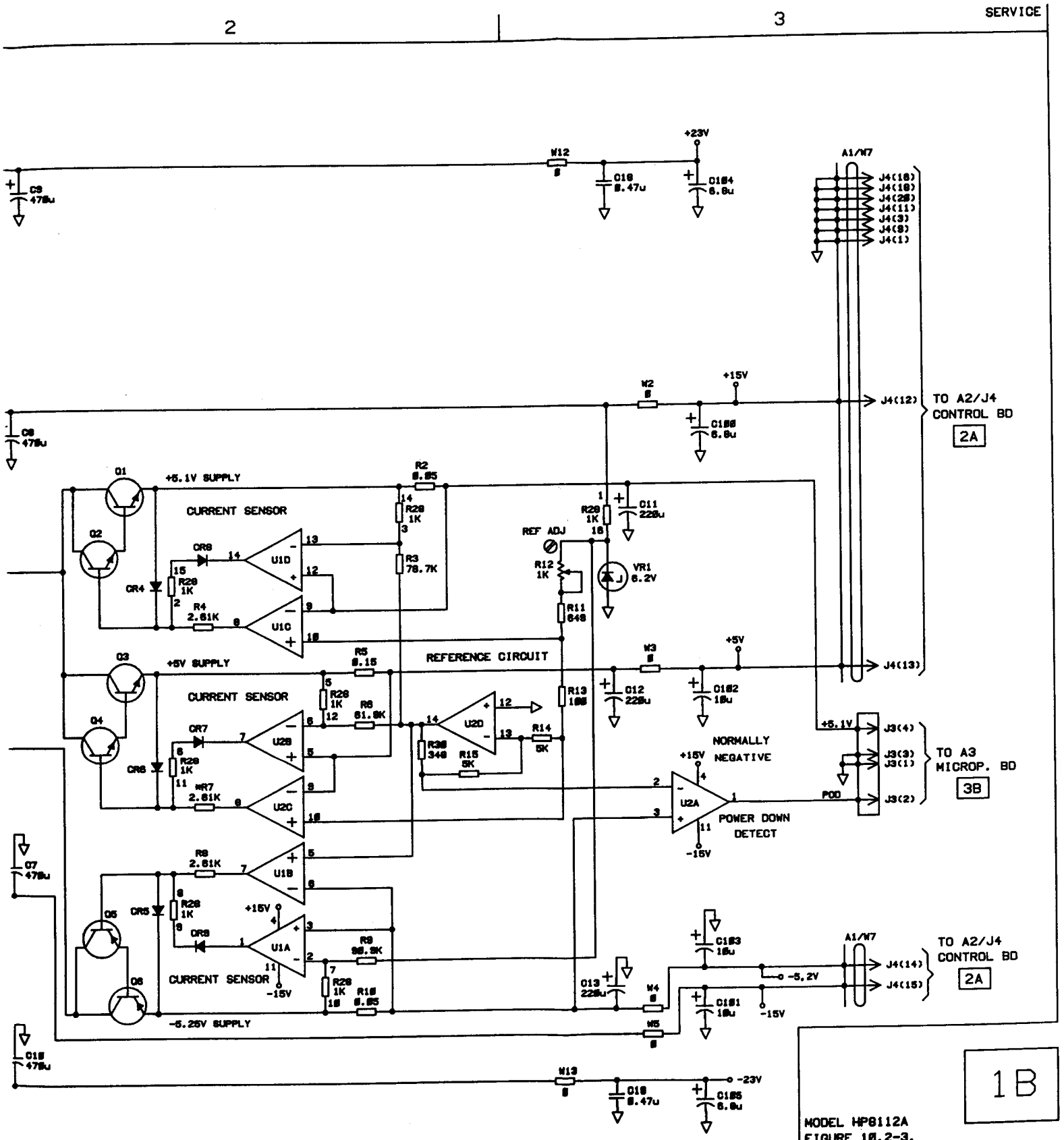
Power-down Detection

U2A is used to detect the power being switched off. Normally its output is negative because its inverting input is at a higher potential (5.1 V) than its non-inverting input (5 V). When the HP 8112A is switched off, the 5.1 V supply breaks down faster than the 5 V reference because it is loaded by the microprocessor board. This is detected by U2A which switches its output towards its positive supply. This "Power Down Detected" signal is used on the microprocessor board to ensure that the microprocessor and HP-IB switch off cleanly. Refer to Chapter 10.7 *Servicing the Microprocessor*.



MODEL HP8112A
FIGURE 10.2-2.
MAIN BOARD A1 SCHEMATIC 1


1
2
A
B
C
P/O A1 MAIN BOARD
J1(1)
J1(2)
J1(3)
J1(4)
J1(5)
J1(6)
J1(7)
1A
+24V UNREG
C14
8.81u
CR2
C15
8.81u
C3
2200u
C4
2200u
-24V UNREG
W3
+23V REG
U3
IN
OUT
COMMON
R16
237
C9
470u
-15V
R17
3.65K
R18
1K
+23V
ADJUST
+15V REG
U5
R22
249
C8
470u
R23
2.49K
R24
500
+15V ADJ
+5V UNREG
CR1
C1
C2
-5.25V UNREG
R1
56
FAN
B1
-15V ADJ
R25
500
R26
2.49K
R27
249
C7
470u
-15V REG
U6
R19
1K
-23V ADJ
R28
3.65K
+15V
R21
237
C18
470u
W12
-24V REG
U4
+15V UNREG
C17
8.81u
CR3
C16
8.81u
C5
2200u
C6
470u
-15V UNREG
Q1
+5.1V SUPPLY
CURRENT SENSOR
Q2
CR8
CR4
R29
1K
R4
2.61K
U1D
U1C
Q3
+5V SUPPLY
CURRENT SENSOR
Q4
CR7
CR6
R29
1K
MR7
2.61K
U2B
U2C
R8
2.61K
U1B
Q5
CR5
R29
1K
+15V
CR9
U1A
Q6
CURRENT SENSOR
-15V
-5.25V SUPPLY



1B

MODEL HP8112A
FIGURE 10.2-3.
MAIN BOARD A1 SCHEMATIC 2

Troubleshooting the Power Supply

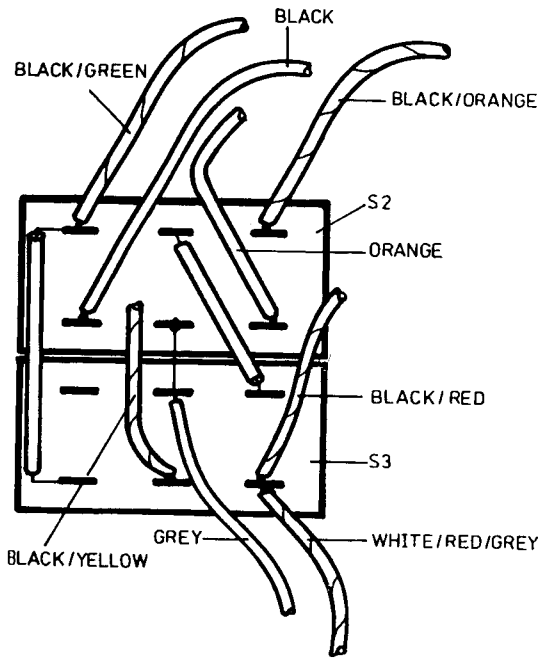


Figure 10.2-4. Detail of wiring to Line Voltage Selector switches

Removing the fan

Starting with the instrument in its Servicing position:

1. Unplug the red and blue wires connecting the fan to the main board.
2. Remove the four screws securing the fan to the rear of the frame.
3. Take out the fan assembly.

Re-fitting the fan

1. Orient the fan so that the arrow on its case (indicating the direction of air-flow):
   - points to the rear of the instrument
   - and is on the bottom.
2. Secure the fan to the rear of the frame using the four screws, keeping the arrow at the bottom and pointing outwards.
3. Plug the red cable onto the pin marked 2, on the main board, routing the cable between the side of the frame and the heatsink.
4. Plug the blue cable onto the pin marked 6.

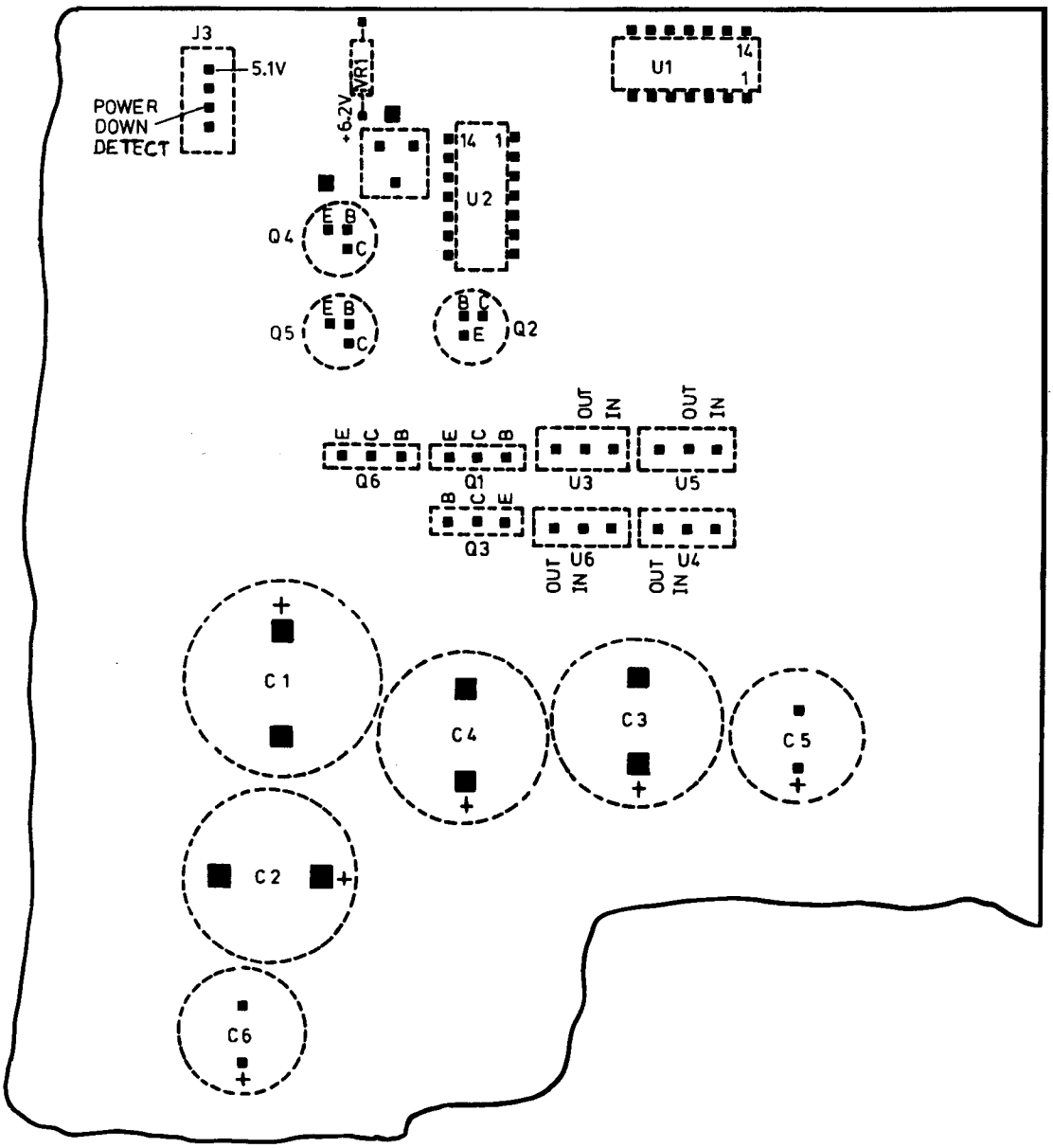


Figure 10.2-5. Power supply components - Underside of main board A1

Note

The main component layout and locator for the main board A1 are in Chapter 10.4.

10.3

Servicing the Timing and Slope Generators

Theory of Operation

Introduction

The majority of the timing and slope generation circuit components are on the main board A1. A small part of the associated circuitry, concerned with burst control, is on the control board A2. Operation of the timing and slope circuits is explained under the following functions:

- Trigger input
- Address decoder
- Control input
- Timing IC (General)
- Period, Width and Delay generation
- Slope generation
- Error feedback

Trigger Input

The trigger input level circuit provides the required trigger-level to the period generator without affecting the external trigger source.

When enabled by $\overline{\text{TON}}$, the External Input signal from the front panel is buffered by Op-amp U110B and shifted to produce an input in the range −4.3 V to +0.4 V for the TRIG IN input for the period generator U200. The actual triggering level is controlled by the front panel level control R119, via Op-amp U110A. When the external trigger signal matches the selected level, U110B applies an input voltage of approximately −1.3 V to pin 7 of the period generator U200.

Trigger mode

Trigger mode selection (positive, negative, gate etc.) is performed by the timing IC U200, in conjunction with the mode decoder circuit U101 and U102 (see "Mode and Range Decoders" and Figure 10.3-1) to provide the type of trigger selected.

Address Decoder

An eight line decoder U100 is controlled by address lines LA3 to LA5 with $\overline{WS1}$. The decoder output lines determine which timing, mode or range circuit latches data from the data bus (LD0 to LD7) as shown in Table 10.3-1. The address decoder also controls the output of the contents of the error latches onto the data bus.

Table 10.3-1. Address decoder enable outputs

U100 pin	Mnemonic	IC	Circuit Action
7	$\overline{SRC}$	U300	Load Range Decoder
10	$\overline{PIC}$	U200	Load Period Generator
11	$\overline{CLR}$	U142	Output Error Latches
12	$\overline{MAMO}$	U101	Load Mode Decoder
13	$\overline{WIC}$	U240	Load Width Generator
14	$\overline{DIC}$	U220	Load Delay Generator

Mode and Range Decoders

Under the control of the Address Decoder, these decoders latch data from the data bus and input it to the various switches that select control and trigger modes and the switching transistors which select the range capacitor to be used by the slope IC.

Control Input Circuits

Refer to Figure 10.3-4. The control input signal is clamped within ±5 V by the protection diodes CR130 to CR132. For Period, Delay, and Width control the input voltage is rectified by precision rectifier U132B and associated components. The signal then passes to the control mode selector switch U130 where microprocessor control signals AC0 and AC1 from the mode decoder U101 select its route to the appropriate timing IC.

When the High Level Control (HILC) is selected, the control input signal is routed through the switch (U131) and low pass filter (U132a with associated components), to the output stages. See chapter 10.5. The low pass filter is needed because of the 20 μs settling time inherant in HILC mode operation.

Timing IC

The timing ICs used in the HP 8112A are programmable timers which can be used to produce repetition rates, pulse widths and delay times by utilizing a variety of trigger and gate mode inputs.

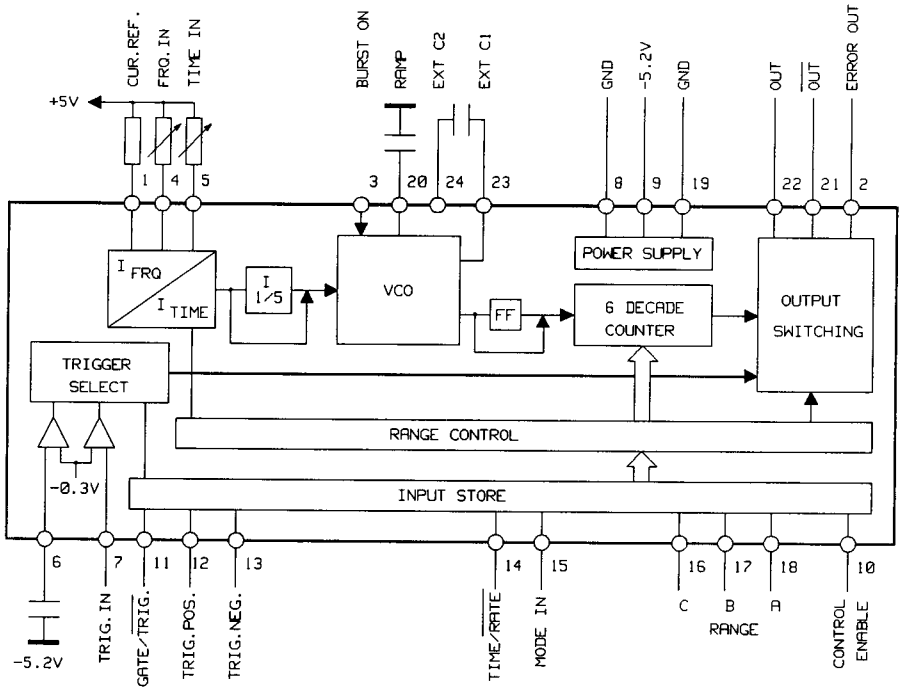


Figure 10.3-1. Timing IC block diagram

Refer to Figure 10.3-1 and Figure 10.3-6. The timing IC has an input store containing 8 control bits which control the mode of the IC:

Table 10.3-2. IC Digital Control Signals

Pin	Name	Signal	Function
10	CONTROL ENABLE	$\overline{WS3}$	A positive TTL edge on this pin latches all the digital control signals into the input store.
11	GATE/$\overline{TRIG}$	LD7	Selects trigger or gate
12	TRIG POS	LD6	Positive trigger
13	TRIG NEG	LD5	Negative trigger
14	TIME/$\overline{RATE}$	LD4	Selects TIME or $\overline{RATE}$ mode
15	MODE	LD3	Always 0 in this application
16	RANGE C	LD2	Range selection, refer to Table 10.3-3
17	RANGE B	LD1	
18	RANGE A	LD0	

Timing Generation

The main timing element of the IC is a voltage controlled oscillator (VCO) which has two ranges of operation in each of the two operating modes (see TIME and $\overline{RATE}$ below). These two basic ranges, time and frequency, are further divided if necessary by switching divider circuits (6 × decade counters) into operation under control of the range setting.

In TIME mode the ranges are from 10 ns to 99.9 ms and 50 ns to 500ns. In $\overline{\text{RATE}}$ mode, ranges are from 100 MHz to 10 MHz and 20 MHz to 2 MHz. Ranges are selectable as shown in Table 10.3-3.

Table 10.3-3. Timing IC Time/frequency Range Selection

Range Number	Range			FREQ OUT in $\overline{\text{RATE}}$ Mode	Out WID or DEL in TIME Mode
	C	B	A		
0	0	0	0	10 MHz – 100 MHz	10 ns – 100 ns
1	0	0	1	1 MHz – 10 MHz	100 ns – 1 μs
2	0	1	0	100 kHz – 10 MHz	1 μs – 10 μs
3	0	1	1	10 kHz – 100 kHz	10 μs – 100 μs
4	1	0	0	1 kHz –10 kHz	100 μs – 1ms
5	1	0	1	100 Hz – 1 kHz	1 ms – 10 ms
6	1	1	0	10 Hz – 100 Hz	10 ms – 100 ms
7	1	1	1	1 Hz – 10 Hz	100 ms – 1 s

Analog control within each range is controlled by the FRQ IN (Pin 4) current, derived from the appropriate DAC on the control board A2, and the TIME IN (Pin 5) current, derived from the control input via the control mode switch U130. The signal passes through a divider circuits before being applied to the VCO.

$\overline{\text{RATE}}$ Mode

In the $\overline{\text{RATE}}$ mode, the timing IC output is a 50% duty cycle square wave whose repetition rate is directly related to the internal range data and the IFRQ input current

TIME Mode

In the TIME mode, the output signal repetition is identical to the input trigger frequency but the output pulse width or delay, depending on trigger mode selection, is directly related to the internal store range data and the FRQ IN current from the relavent DAC.

Selection of the above modes is made by using the MODE IN and $\overline{\text{RATE}}$ inputs as shown below.

Table 10.3-4. Timing IC mode selection

TIME	MODE IN	MODE/OUTPUT
0	0	$\overline{\text{RATE}}$ RATE
0	1	Not used
1	0	TIME TIME
1	1	Not used

Because CUR REF, FRQ IN and TIME IN are virtual earth inputs, the external input currents can be produced by a voltage source and series resistance. The control mode functions (PERC, DELC, WIDC) are produced by feeding the conditioned control input voltage to the TIME IN input of the relevant timing IC. The approximate value of current drawn by the input current pins is shown below.

Table 10.3-5. Reference current input levels

Reference Current	FRQ IN	TIME IN
$\overline{\text{RATE}}$ mode approx 80 μA	2 mA - 0.2 mA	0.2 mA const
TIME mode approx 80 μA	2 mA - 0.2 mA	0.2 mA const
CTRL mode approx 80 μA	2 mA - 0.2 mA	2 mA - 0.2 mA

Outputs

The three outputs of the Timing ICs (OUT, $\overline{\text{OUT}}$, ERROR OUT) are all open-collector with a fixed current (HI = 0 mA, LO = 12 mA) and a fixed transition time of 2.5 ns.

Error Output. The error output from the timing IC indicates that a trigger signal has been received before the completion of the previously triggered event.

Period, Delay and Width Generation

Period, Delay and Width signals are generated by Timing ICs U200, U240 and U220 respectively.

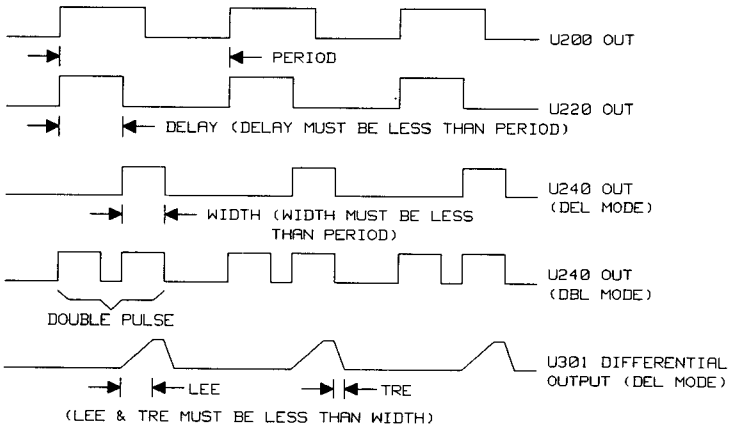


Figure 10.3-2. Example of signal generation

Period Generator

The period generator operating in the $\overline{\text{RATE}}$ mode produces 50% duty cycle square wave output pulses at a repetition rate governed by the analog current input (from the Period DAC or Control Input) and the internal range data.

The IC is either free running or triggered by the EXT INPUT, depending on the state of the internal trigger mode latches (data from LD5 to LD7). The inverse output $\overline{OUT}$ is passed to the trigger amplifier (Chapter 10.7) for subsequent output as TRIG OUT. Normal output OUT, is passed via level shifter Q200 to the delay generator trigger input.

Connections are also made from the period generator to the Burst Clock described in chapter 10.6.

Delay Generator

The delay generator, working in TIME mode produces a time-shifted output identical in rate to its trigger input. The delay time is dependant on the analog inputs, internal range data, and triggering mode. See Figure 10.3-2 for an example of signal generation. A delay time greater than the periodic time will cause ERROR OUT to become active. Normal output OUT, is passed via level shifter Q220 to the width generator trigger input.

Width Generator

The width generator, working in TIME mode produces an output of equal repetition rate to its trigger input, but whose width is dependant on the analog inputs, internal range data. In DBL mode the width generator is configured to produce an output pulse at both leading and trailing edges of the trigger pulse from the delay generator. See Figure 10.3-2 for an example of signal generation. An output pulse width which is greater than the periodic time will cause ERROR OUT to become active. Normal output OUT, is passed directly to the Slope Generator IC.

Slope Generation

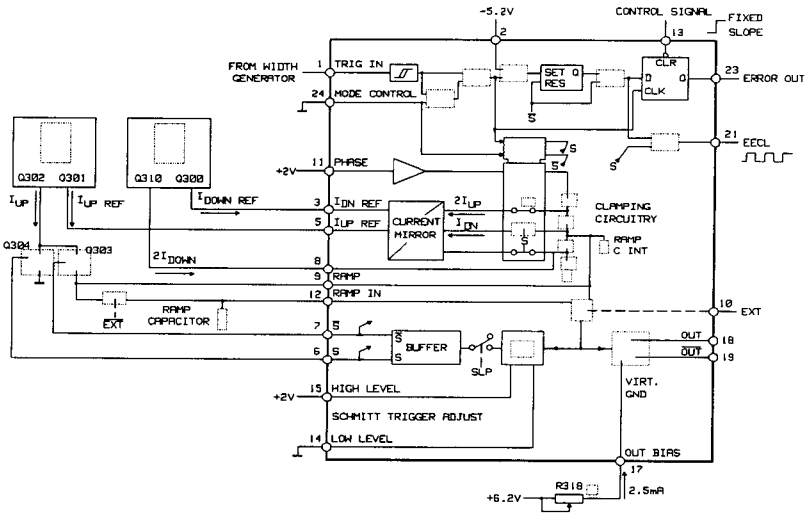


Figure 10.3-3. Slope IC block diagram

Refer to Figure 10.3-5 and Figure 10.3-3. When triggered by the output of the width generator, the Slope IC U301 operates in one of two transition modes.

Fixed Transition

In fixed mode (fixed 4.5 ns transitions), an ECL trigger output is

time output pulses.

With fixed mode selected, the input trigger signal on pin 1 is passed via ECL circuitry to the EECL output, pin 21. See Figure Figure 10.3-3. An error output is available at pin 23, this goes active

Current Sources

External constant current sources on the control board A2 provide $I_{up\ ref}$ and $I_{down\ ref}$. When a rising edge is detected at TRIG IN, Q303 is switched on via the internal buffer to enable one of the internal or external ramp capacitors to charge up linearly by I_{up} (derived from $I_{up\ ref}$) at a rate set by the LEE DAC on the control board. Once the charge threshold of 2 V has been reached, charging current is diverted via internal diodes into the current mirror circuit, and the capacitor voltage remains constant.

When a falling edge is detected at pin 1, Q303 is switched off and Q304 is switched on, dumping I_{up} to ground. The capacitor now discharges via the current mirror at a rate set by $I_{down\ ref}$, to 0 V. At this point I_{down} is diverted via the internal diodes and the current mirror circuit, and the capacitor voltage remains at 0 V until the next trigger is detected.

Range Switches

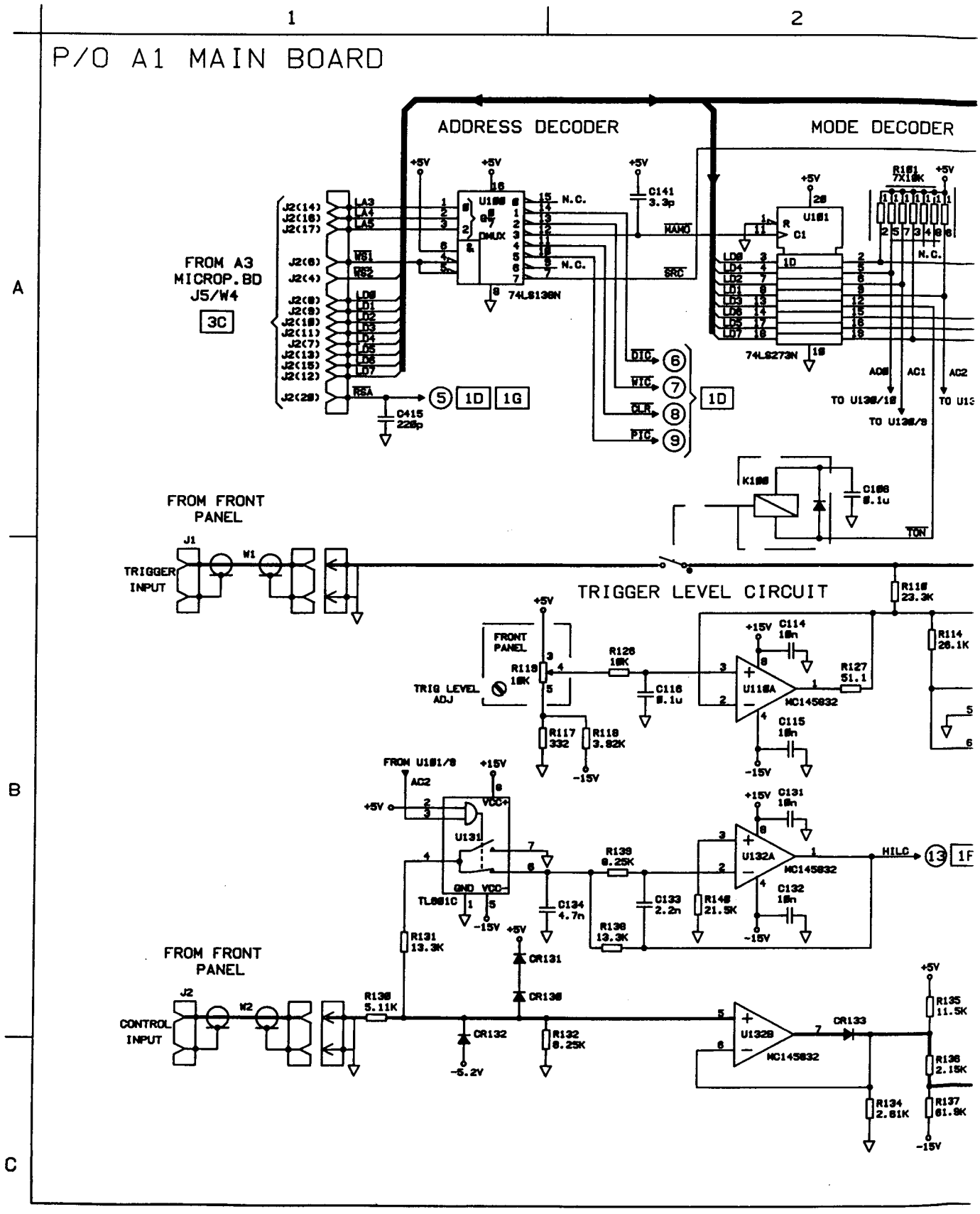
The ramp timing capacitance is selected from range latch U300. Slopes from 100 μs to 95 ms are possible with the external capacitors, slopes less than 100 μs use the internal capacitor in U301.

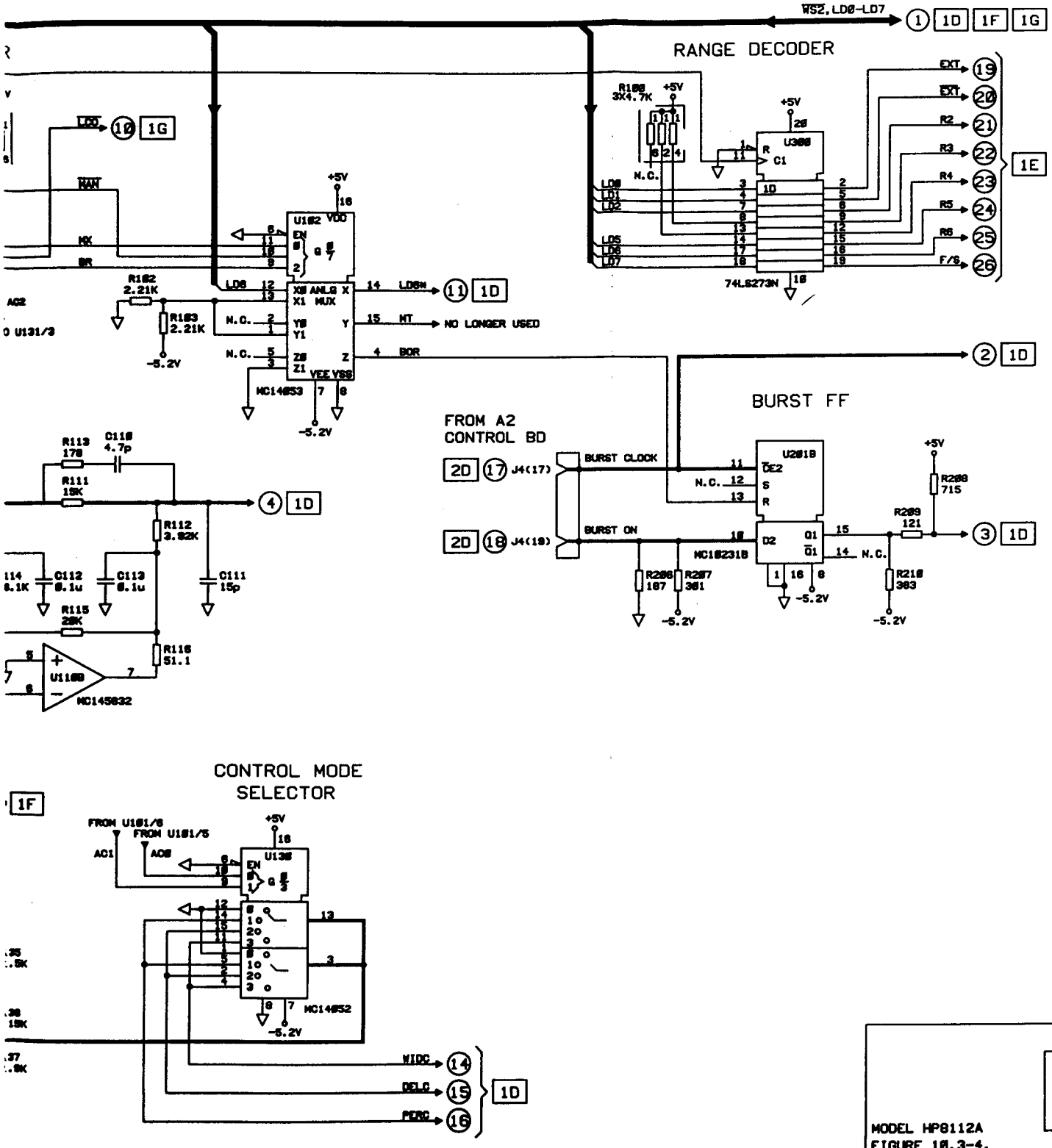
Reference Circuit

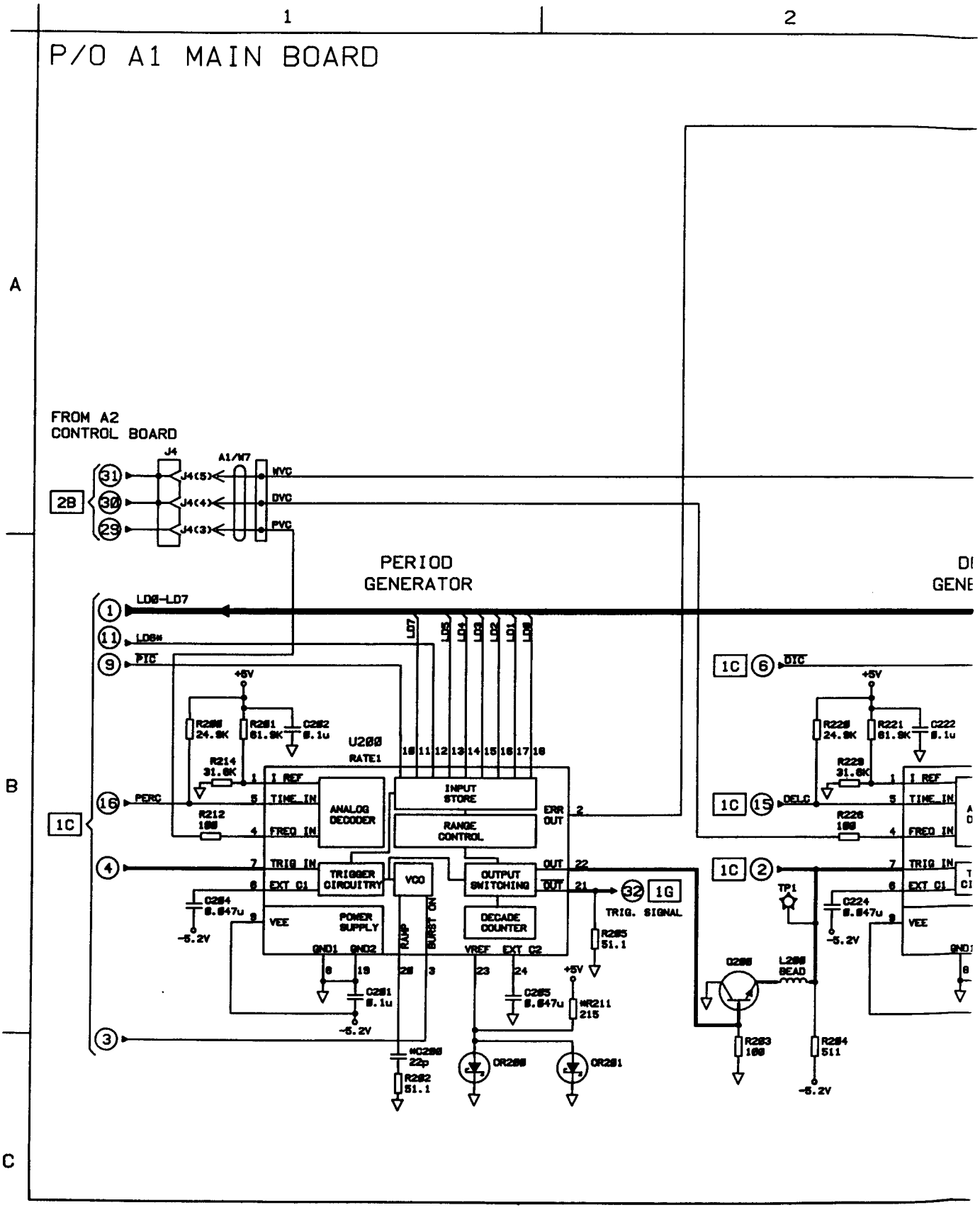
An external reference source U320 and associated components, provides the reference voltage (via the Schmidt trigger) required by the internal switching diodes which clamp the ramp voltage and the output current sources.

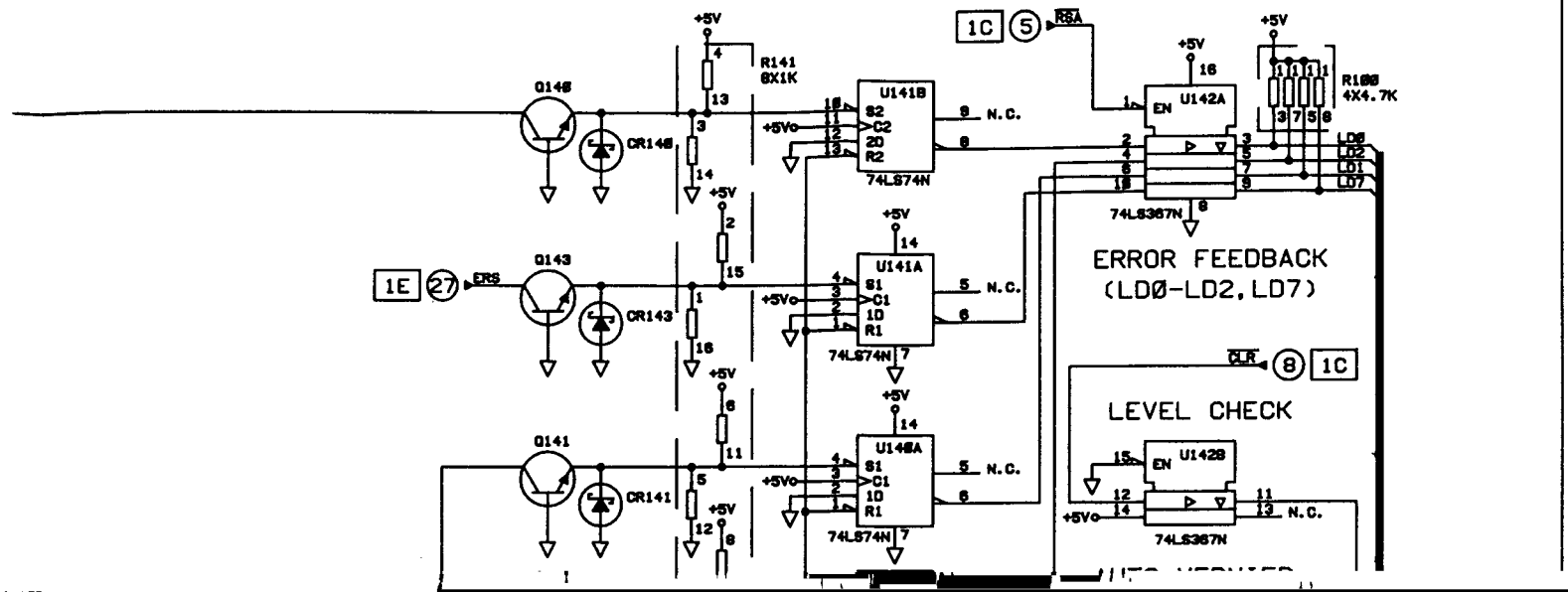
Error Feedback

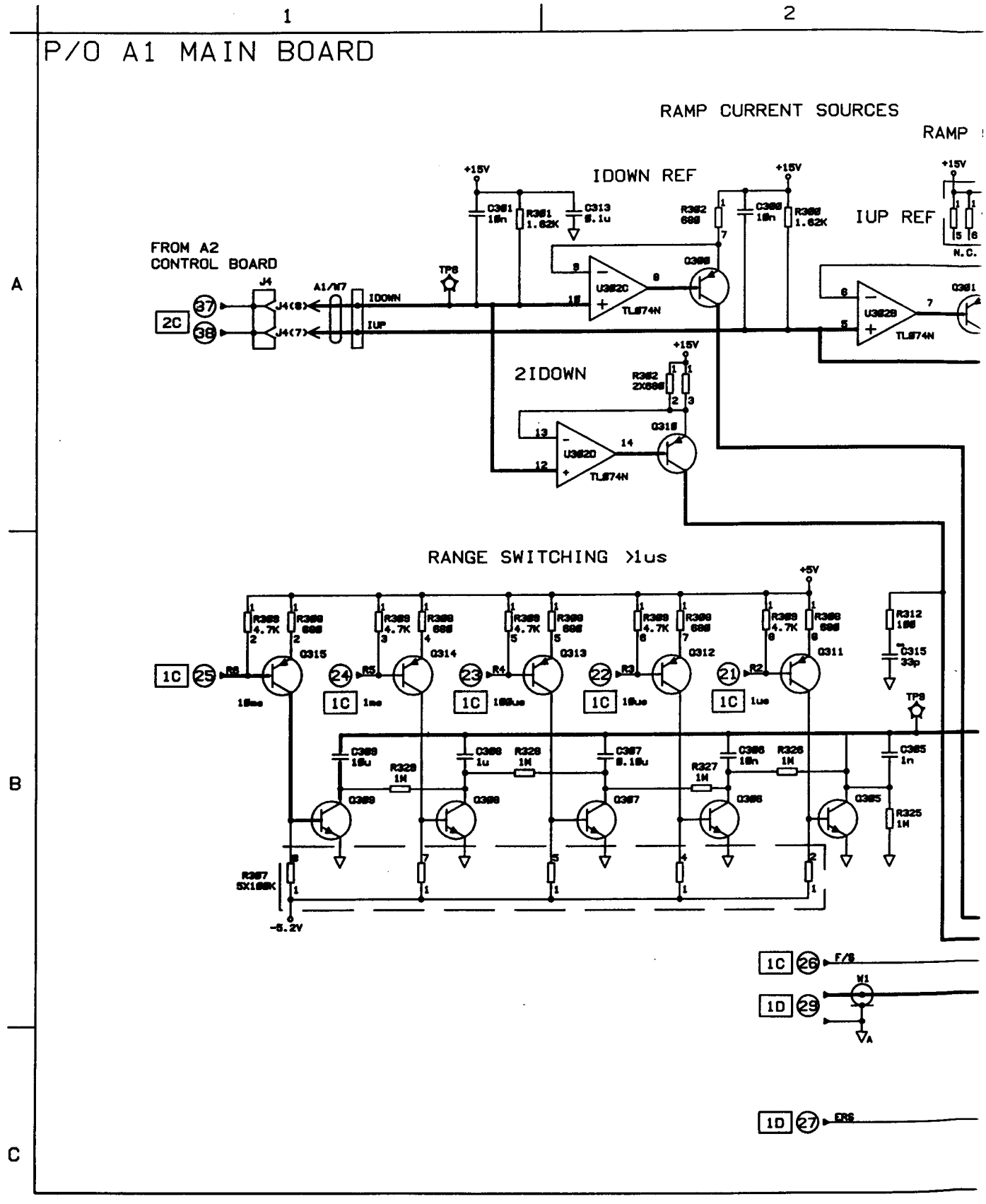
The four ECL error feedback outputs from the Timing and Slope ICs are converted to TTL levels by transistors Q140 to Q143 and their associated components. The error outputs are fed via latches and drivers to the Data Bus when $\overline{\text{RSA}}$ is active.


1
2
A
B
C
P/O A1 MAIN BOARD
ADDRESS DECODER
MODE DECODER
FROM A3
MICROP.BD
J5/W4
3C
74LS138N
74LS273N
C415
220p
C141
3.3p
C106
0.1u
TO U13B/1B
TO U13B/8
FROM FRONT
PANEL
J1
W1
TRIGGER
INPUT
TRIGGER LEVEL CIRCUIT
FRONT
PANEL
TRIG LEVEL
ADJ
R119
15K
R126
15K
R118
23.3K
R114
26.1K
R127
51.1
C116
0.1u
R117
332
R118
3.92K
C114
15n
C115
15n
U116A
MC145032
FROM U1B1/8
AC2
U131
TL081C
R139
8.25K
R138
13.3K
C134
4.7n
C133
2.2n
R140
21.5K
C131
15n
C132
15n
U132A
HILC
FROM FRONT
PANEL
J2
W2
CONTROL
INPUT
R130
5.11K
R131
13.3K
CR131
CR130
CR132
-5.2V
R132
8.25K
U132B
CR133
R135
11.5K
R136
2.15K
R134
2.61K
R137
61.9K

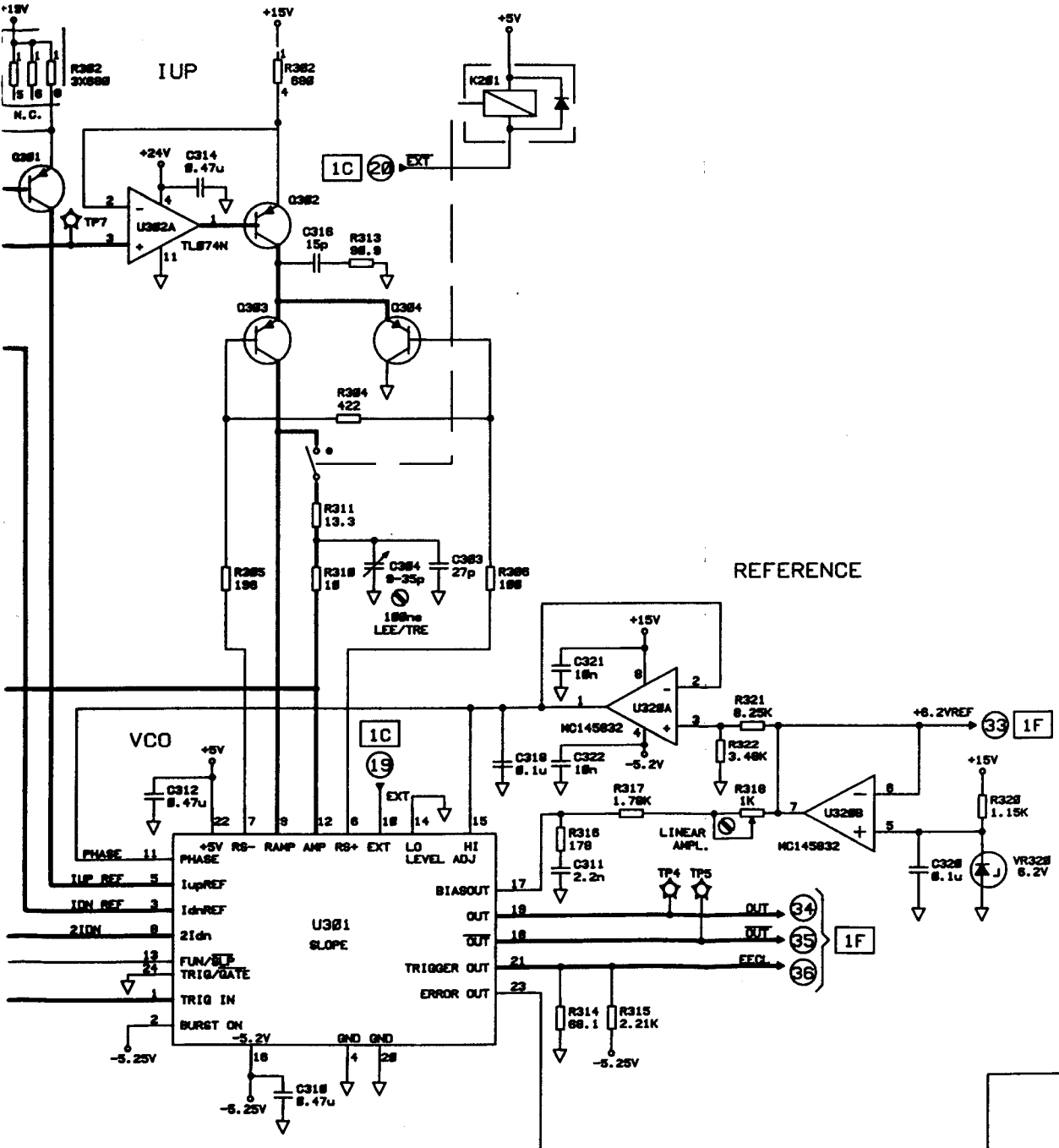

WS2, LD0-LD7
RANGE DECODER
EXT
EXT
R2
R3
R4
R5
R6
F/S
74LS273N
LDD
MAN
MX
MR
LD8
R162 2.21K
R163 2.21K
-5.2V
MC14053
LDSN
NO LONGER USED
BOR
BURST FF
FROM A2 CONTROL BD
BURST CLOCK
BURST ON
MC10231B
R288 715
R289 121
R286 187
R287 301
R218 383
R113 178
C118 4.7p
R111 15K
R112 3.92K
C112 0.1u
C113 0.1u
C111 15p
R115 20K
R116 51.1
MC145032
CONTROL MODE SELECTOR
FROM U101/6
FROM U101/5
MC14052
MIDC
DCLC
PERC


1
2
A
B
C
P/O A1 MAIN BOARD
FROM A2
CONTROL BOARD
J4
A1/W7
2B
WVC
DVC
PVC
PERIOD
GENERATOR
LD0-LD7
LD8H
PTC
PERC
1C
+5V
R208
24.9K
R201
61.9K
C202
0.1u
R214
31.6K
R212
100
U200
RATE1
I REF
TIME IN
FREQ IN
ANALOG
DECODER
INPUT
STORE
RANGE
CONTROL
ERR
OUT
TRIG IN
EXT C1
TRIGGER
CIRCUITRY
VCO
OUTPUT
SWITCHING
OUT
32
1G
TRIG. SIGNAL
C204
0.047u
-5.2V
VEE
POWER
SUPPLY
DECADE
COUNTER
R205
51.1
GND1
GND2
RAMP
BURST GN
VREF
EXT C2
C201
0.1u
C205
0.047u
+5V
WR211
215
C206
22p
R202
51.1
CR206
CR201
DTC
DELC
R220
24.9K
R221
61.9K
C222
0.1u
R223
31.6K
R226
100
C224
0.047u
TP1
Q206
L206
BEAD
R203
100
R204
511


+5V
R141
8X1K
Q148
CR148
U141B
74LS74N
N.C.
1C
5
R5A
U142A
74LS367N
R186
4X4.7K
LD0
LD2
LD1
LD7
ERROR FEEDBACK
(LD0-LD2, LD7)
1E
27
ER5
Q143
CR143
U141A
74LS74N
CLR
8
1C
LEVEL CHECK
Q141
CR141
U148A
U142B
+5Vo


1
2
P/O A1 MAIN BOARD
RAMP CURRENT SOURCES
RAMP
IDOWN REF
IUP REF
FROM A2
CONTROL BOARD
J4
A1/W7
IDOWN
IUP
TP8
+15V
2IDOWN
TL074N
RANGE SWITCHING >1us
+5V
-5.2V
F/S
ERS
A
B
C

MP CURRENT SOURCES



1E

MODEL HP8112A
FIGURE 10.3-6.
MAIN BOARD A1 SCHEMATIC 5

Troubleshooting

Note

- If an error code is being displayed by the HP 8112A you must press a key, (LCL) for example, to return the microprocessor to normal operation before troubleshooting.
- The component layout and locator for the main board A1 is at the end of this chapter.

Address Decoder

The address decoder U100 can be checked with signature analysis. Set the microprocessor to free run mode as follows:

1. Set the P1 wire on board A3 (See Chapter 10.7) to position **P1**.
2. Disconnect Jumper A2W1.
3. Connect RES on A3 to ground for a short time to ensure the microprocessor is reset.
4. Connect the signature analyser ground to the microprocessor board ground, then set the signal analyser as follows:

Signal Analyzer	**A3 μP Board Connections**
Start ƒ	TP "SA"
Stop ƒ	TP "SP"
Clock ↿	TP "E"
Ground	Ground

5. Verify that the reading at the microprocessor board +5 V is 0003.
6. Check the signature of board inputs against those given in Table 10.3-6

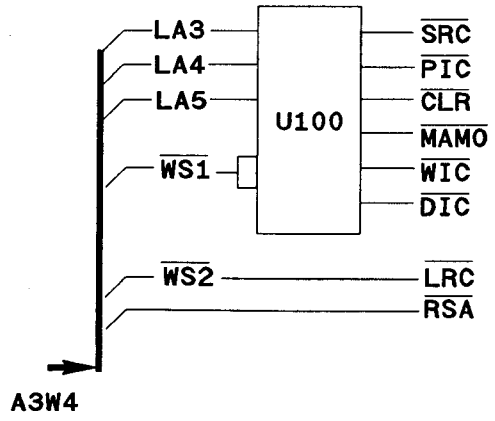


Table 10.3-6. Address Decoder Signatures

Connector A3W4	Mnemonic	Description	Free run S.A.	Area
LA3		Sub coded address	P50H	U100/1
LA4		Sub coded address	CH9U	U100/2
LA5		Sub coded address	8759	U100/3
$\overline{WS1}$		Enable address decoder	1P50	U100/4
$\overline{WS2}$	$\overline{LRC}$	Data load signal for U500 see chapter 10-4	PU99	U500/11
$\overline{RSA}$		Error feedback gate signal	9H1P	U142/1

7. Check the signature of address decoder outputs against those given in Table 10.3-7

Table 10.3-7. Address Decoder Signatures

U100 Pin	Mnemonic	Description	Free run S.A.	Area
7	$\overline{SRC}$	Slope range decoder load signal	273U	U300/11
10	$\overline{PIC}$	Period input store select	U859	U200/10
11	$\overline{CLR}$	Error feedback reset	P54U	U142/12
12	$\overline{MAMO}$	Mode decoder data load signal	8PHH	U101/11
13	$\overline{WIC}$	Width input store select	C10F	U240/10
14	$\overline{DIC}$	Delay input store select	3813	U220/10

Control Mode Selection

Check the control-mode selection signals from control-latch U101 against Table 10.3-8 and Table 10.3-9:

Table 10.3-8. Mode Decoder check table

Mode	Ext. Input Slope Switch	U101 pin 12 $\overline{TON}$	Relay K100
TRIG	+ ƒ and,or ↘	Low	On
GATE	+ ƒ or ↘	Low	On
E.WID	+ ƒ or ↘	Low	On
E.BUR	+ ƒ and,or ↘	Low	On

Table 10.3-9. U101 Mode Decoder truth table

CTRL Mode Mnemonic	U101/9 (AC2)	U101/6 (AC1)	U101/5 (AC0)	U101/16
Off	L	L	L	
PERC	L	L	H	
DELC	L	H	L	
WIDC	L	H	H	
HILC	H	L	L	
Area	U131/2	U130/10	U130/9	U503/1

The level check output ($\overline{LCO}$) on pin U101/16 is LOW in normal mode and HIGH during self test.

Period Generator

To check operation of the Ext. Input Circuit:

1. Set up the HP 8112A as follows:

Mode	Trig
Trig Slope	f
Trig Level Pot	Mid-range

2. Apply a symetrical signal to the Ext. Input.
3. Check the input signal from the trigger input circuit at pin 7 of U200 against Figure 10.3-8.

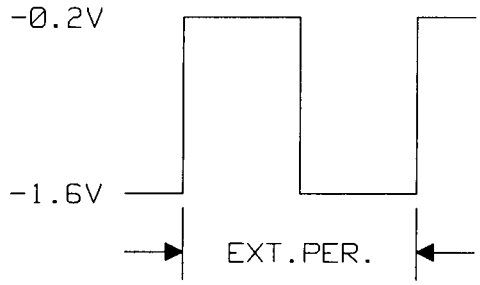


Figure 10.3-8. Period Generator Input pin 7

To check the operation of the Period Generator:

1. Set the HP 8112A to RCL 0
2. Check the ramp signal at pin 20 of U200 against Figure 10.3-9.

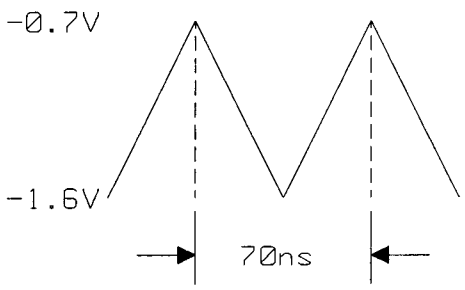


Figure 10.3-9. Period Generator ramp signal pin 20

3. Check the trigger output signal at pin 21 of U200 against Figure 10.3-10.
4. Check the signal being sent to the delay generator IC220 at TP1 against Figure 10.3-10.

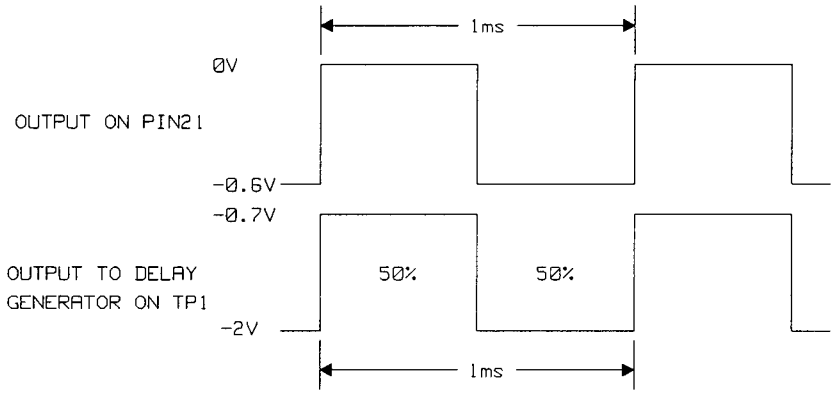


Figure 10.3-10. Period Generator output signals

5. Check the period generator operation against Table 10.3-10 and Table 10.3-11:

Table 10.3-10. Period Generator Operation

U200 Pin	Mnemonic	Description	State
5	PERC	Period control voltage input	L
2	ERP	Period error output signal	L
10	$\overline{\text{PIC}}$	Period input store select	See Table 10.3-1
11 to 18	LD7 - LD0	Data to be latched into the input store of U200	See Table 10.3-2
R212	PVC	Period vernier current	See Table 10.3-11

6. Verify that voltage at U200 pins 1, 4 and 5 are at virtual ground (min. −40 mV max. 0 V)

Note

Period Vernier Current can be checked by measuring the voltage across R212.

Table 10.3-11. Period Generator Signal Levels

PER Setting	Voltage across R212
1 ms	+0.16 V
5 ms	+0.003 V
9.99 ms	−0.016 V

Delay Generator

1. Set up the HP 8112A as follows:

   RCL 0
   DEL 650 μs or
   DBL 200 μs

2. Check the input signal from the period generator pin 7 of U220 against Figure 10.3-11.

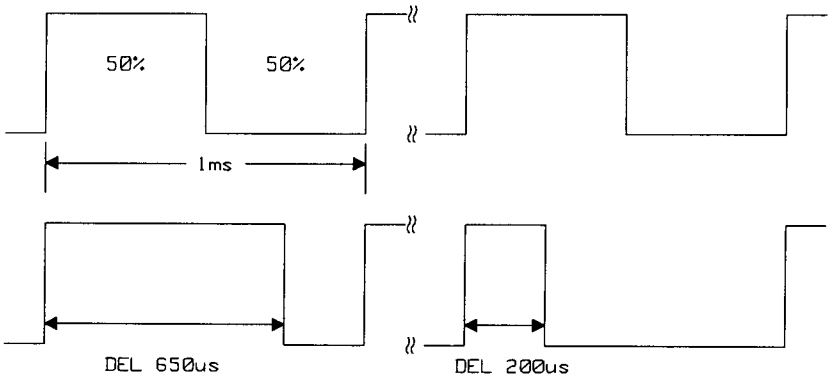


Figure 10.3-11. Delay Generator I/P O/P waveforms

3. Check the ramp signal at pin 20 of U220 against Figure 10.3-12.
4. Check the signal being sent to the width generator IC240 at TP2 against Figure 10.3-11.

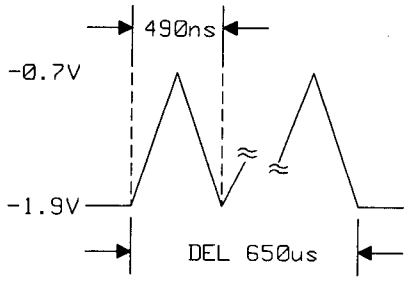


Figure 10.3-12. Delay Generator ramp signal pin 20

5. Check the Delay Generator operation against Table 10.3-12

Table 10.3-12. Delay Generator Operation

U220 Pin	Mnemonic	Description	State

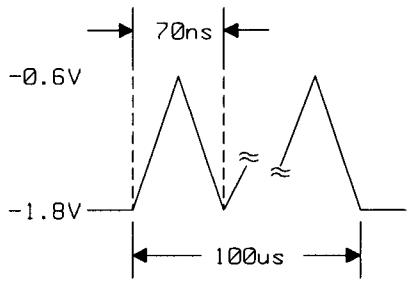


Figure 10.3-14. Width Generator ramp signal

4. Check the signal being sent to the slope generator IC at TP3 against Figure 10.3-15.

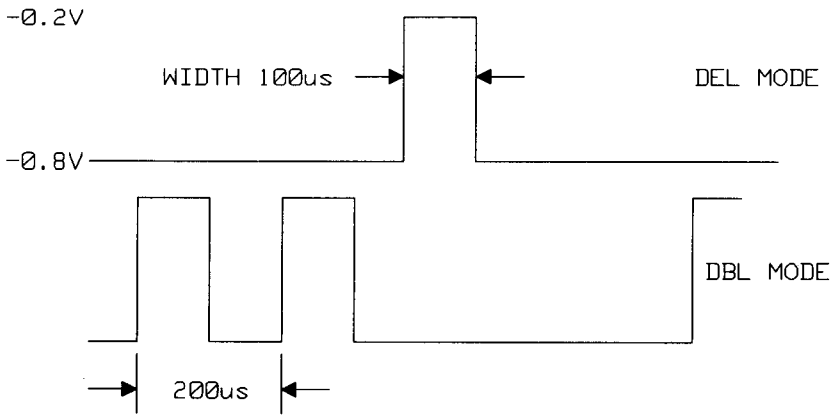


Figure 10.3-15. Width Generator output

5. Check the Width Generator operation against Table 10.3-14 and Table 10.3-15

Table 10.3-14. Width Generator Operation

U240 Pin	Mnemonic	Description	State
5	WIDC	Width control voltage input	L
2	ERW	Width error output signal	L
10	$\overline{\text{WIC}}$	Width input store select	See Table 10.3-1
11 to 18	LD7 - LD0	Data to be latched into the input store of U240	See Table 10.3-2
R245	WVC	Width Vernier Current	See Table 10.3-15

6. Verify that voltage at U240 pins 1, 4 and 5 are at virtual ground (min. −40 mV max. 0 V)

Note

Width vernier current can be checked by measuring the voltage across R245.

7. Set HP 8112A PER to 20 ms
8. Check signal levels against Table 10.3-15

Table 10.3-15. Width Generator Signal Levels

WID Setting	Voltage across R245
1 ms	+0.125 V
5 ms	+0.004 V
9.99 ms	−0.02 V

Slope Generator

1. Set the HP 8112A to RCL 0 and press the (Set) key:
2. Check the input signal from the width generator at pin 1 of U301 against Figure 10.3-16
3. Check the ramp current input at pins 9 and 12 of U301 against Figure 10.3-16
4. Check the signals being sent to the shaper IC (waveforms at TP1, TP4 and pin 21 of U301) against Figure 10.3-16.

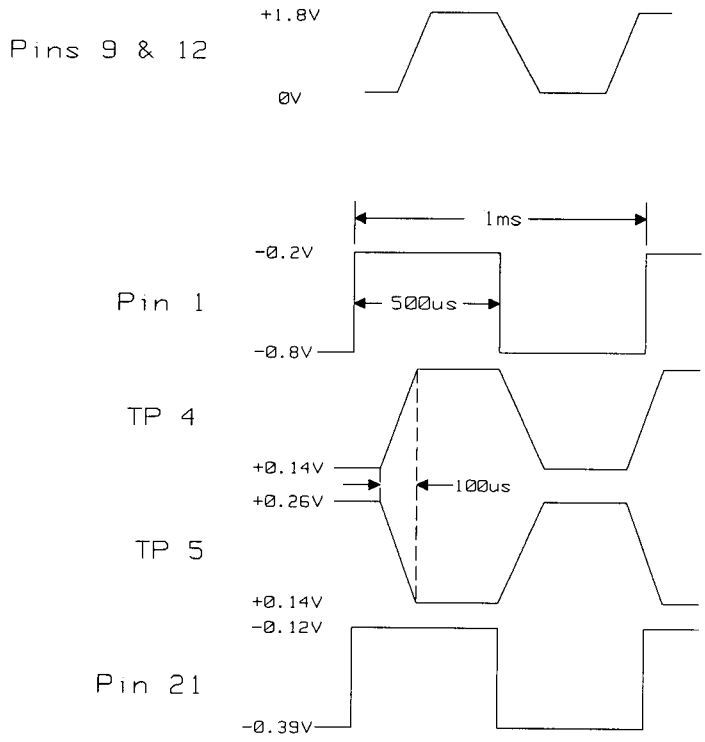


Figure 10.3-16. Slope Generator Input and Output signals

5. Verify that the voltages at U301 pins 11/15 are at REF voltage (typ. +1.85 V)
6. Verify that the voltage at U301 pin 13 is at TTL LOW level (typ. +90 mV)

Range Decoder

1. Check the range decoder against Table 10.3-16.

Table 10.3-16. Range Decoder Truth Table

U300 Pin		2	5	6	9	12	15	16	19
Slope Range	Transition Time	Ext	$\overline{\text{Ext}}$	R2	R3	R4	R5	R6	F/S
1	5.5 ns - 99.9 ns	L	H	H	H	H	H	H	L
2	50 ns - 999 ns	H	L	H	H	H	H	H	L
3	0.5μs - 9.9 μs	H	L	L	H	H	H	H	L
4	5μs - 99.9 μs	H	L	L	L	H	H	H	L
5	50 μs - 999 μs	H	L	L	L	L	H	H	L
6	0.5 ms - 9.99 ms	H	L	L	L	L	L	H	L
7	50 ms - 99.9 ms	H	L	L	L	L	L	L	L
Area		U301/ 10	K300	Q311	Q312	Q313	Q314	Q315	U301/ 13
Only in Self-Test									H

Note

LEE and TRE must be in the same range. See transition modes operating section)

2. Should values of LEE and TRE be selected that overlay in an overlap region, the microprocessor selects the nearer range.

Example. If LEE and TRE are changed from 100 ns to 750ns, Range 2 will be selected and if they are changed from 100 μs to 750 ns, Range 3 will be selected.

10.4

Servicing the Shaper and Output Amplifier

Theory of Operation

Introduction

The shaper and output amplifier circuits are located on the main board A1 and are divided into the following parts:

- Bus Latch
- Shaper IC
- Current Mirror
- Pre-Attenuator
- Signal Output Amplifier
- Output Attenuator
- Trigger Output Amplifier
- Level Check Circuit

These circuits are the last in the signal path.

Bus Latch

An eight line decoder U500 latches data from the data bus when enabled by $\overline{WS2}/\overline{LRC}$ (sent by the microprocessor) and outputs the data to the shaper IC where it is used to control pulse shaping/correction and to select output mode and complement. The data is also applied to the pre-attenuator where it controls the attenuation and output disable functions via relays K500 to K504.

Shaper IC

The shaper IC U401, shown in Figure 10.4-1,is a high-performance signal-control circuit which, depending on the state of its mode inputs (pins 22 and 23), produces outputs as shown in Table 10.4-1.

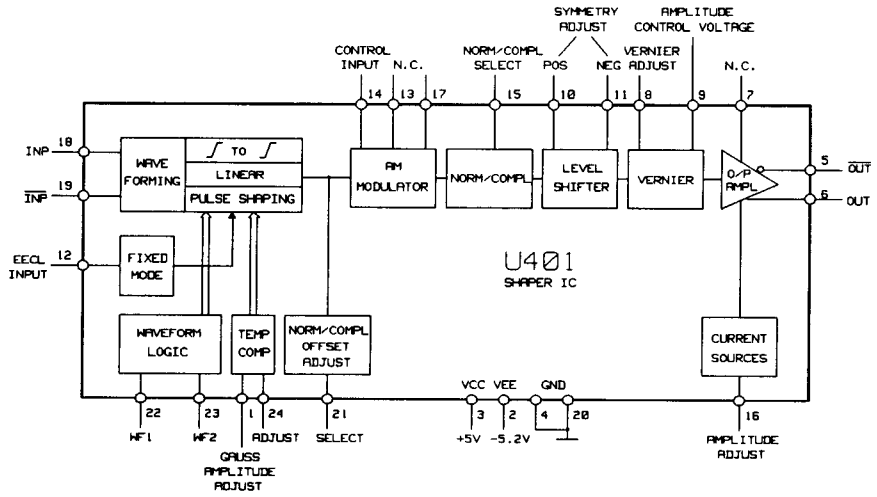


Figure 10.4-1. Shaper IC Block Diagram

Table 10.4-1. Shaper IC Output Modes

Inputs		Input	Output
WF1	WF2	Selected	Signal
LO	LO	Differential	Linear
LO	HI	Differential	Shaped
HI	LO	Not used	———
HI	HI	EECL (0 V, −0.6 V)	Fast Pulse

The main inputs are differential current inputs INP or $\overline{\text{INP}}$. The single-ended EECL voltage input (0 V to -0.6 V) generates an output pulse with fast, but fixed, transition times.

Wave Forming

In Linear transition mode, the waveform block within the shaper IC acts as a linear amplifier upon the input from the slope generator (See Chapter 10.3).

In shaped (Gaussian) mode, the linear slopes of the input pulses are given gaussian characteristics controlled by the inputs on pins 1 and 24 of the shaper IC.

For fixed transitions, the single ended EECL input is used to provide fast, fixed mode output pulses having a fixed transition of 4.5 ns.

Output Mode

For all waveforms, normal or complement output is selected by a digital input from the bus latch to pin 15 of the shaper IC. This input works in conjunction with a bias adjusting network and the internal level shift, to provide normal and complement output modes.

Shaper Output

A portion of the amplitude vernier control (See Chapter 10.5) and HILC input (See Chapter 10.3) are used by the vernier block in the shaper IC to attenuate the output signal. The IC output amplifier block is a differential output circuit, whose reference currents are derived from the 6.2 V reference on the timing generator.

Current Mirror

The differential output of the shaper IC requires a "current mirror" output stage which eliminates the effect of quiescent currents and doubles the available output signal. The operating principle is illustrated in Figure 10.4-2, and depends on Q1A and Q1B being a matched pair so that $I_a = I_b$.

In the HP 8112A Q1A = Q400A, Q1B = Q400B and Q2 = Q402. In fixed mode, Q403 is turned on, switching the R430/C409 combination into the current mirror in order to improve its performance.

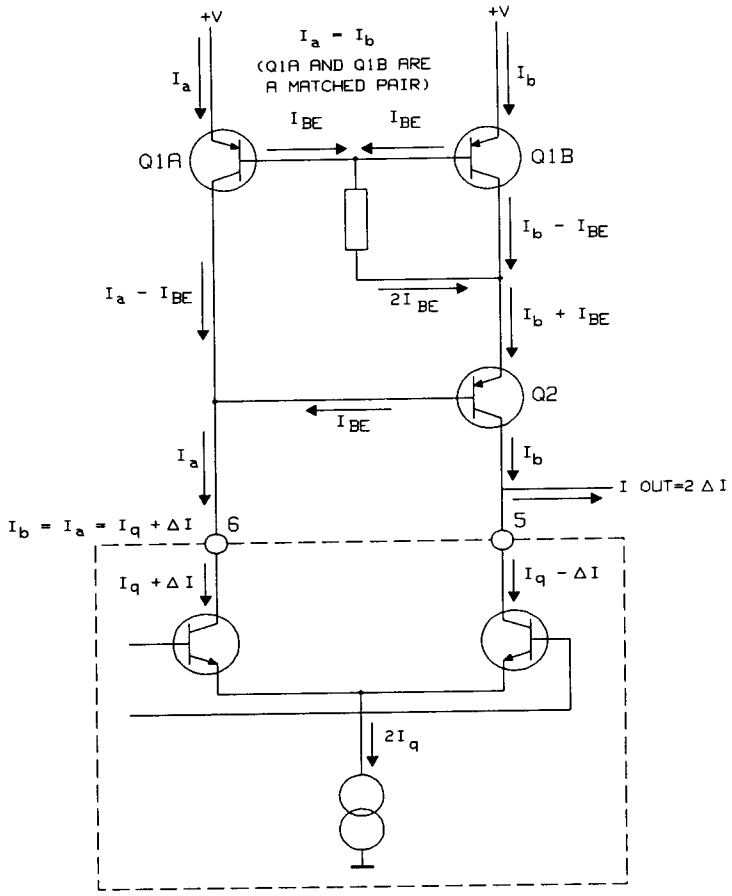


Figure 10.4-2. Current Mirror

Pre-Attenuator

The pre-attenuator circuit is controlled by the microprocessor via latch U500. Logic signals K1 – K4 control relays K500 – K503 to provide three levels of attenuation according to the range of output voltage required.

Table 10.4-2. Pre-attenuator ranges

Attenuation	Active Relay(s)	Final Output Range
0 dB	K503	10 to 16 V
−4 dB	K502	1 to 9.99 V
−24 dB	K500 & K501	0.1 to 0.99 V

Signal Output Amplifier

The output amplifier amplifies the signal received from the shaper IC via the pre-attenuator and adds the required offset voltage as dictated by the HIL and LOL settings. A simplified version of the circuit is given in Figure 10.4-3

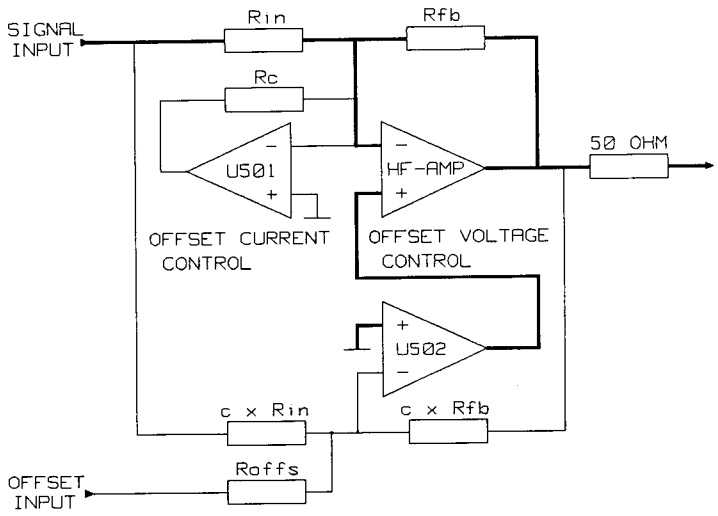


Figure 10.4-3. Simplified Output Amplifier circuit

The circuit is effectively an inverting amplifier with a voltage gain given by

$$Gain = \frac{R_{fb}}{R_{in}}$$

The main HF amplifier consists of the discrete transistors Q501 – Q513 and their related components on Figure 10.4-5.

The offset current error of the amplifier is compensated for by the offset-current control amplifier U501. This amplifier compares the virtual ground at the inverting-input of the main-amplifier with actual ground, and supplies a compensating current via R_c in order to maintain zero difference.

[redacted]

voltage at the main amplifier output, via the feedback network c x R_{in} / c x R_{fb}, and compensates for it via the main-amplifier's non-inverting input.

The required output-offset is created by injecting the offset-input signal from, the offset vernier DAC and the HILC from the timing

Voltage gain

The signals from the input stage, generated across R524 and R527, are applied to the bases of Q503 and Q504. These transistors operate as emitter followers for Q505 and Q506 which provide the actual voltage gain.

Output

The output stage consists of the emitter-follower pairs Q510, Q512 and Q511, Q513. These decouple the voltage gain stage from the low output-impedance.

Trigger Output Amplifier

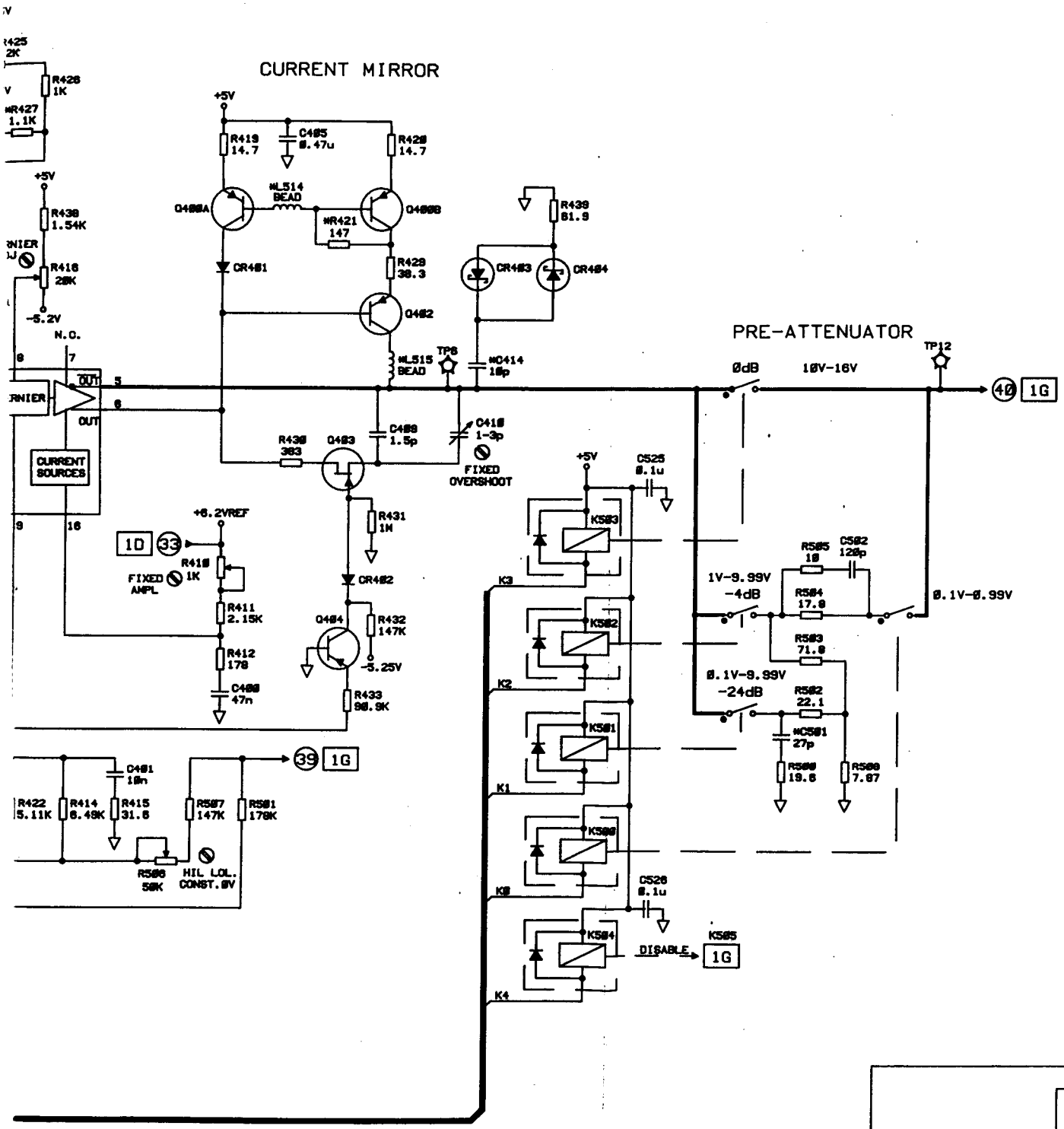
The input to the trigger amplifier, derived from the period generator (See Chapter 10.3), is passed via a schmidt trigger input Q280 and Q281, to the output stage. With a logic high on the input, Q282 is switched on and in turn switches Q283 off, to produce a low (0 V) output.

When the circuit input goes low, Q282 is switched off allowing Q283 to switch on and provide an output voltage of 2.4 V into 50 Ω or 4.8 V into a high impedance.

Due to the inverting action of the trigger amplifier, the inverted trigger input pulse is output as a positive going pulse, synchronized to the output of the period generator. In normal mode the TRIG OUT signal is a 50% duty cycle square wave at the same frequency as the main HP 8112A output. In TRIG and GATE modes, the TRIG OUT signal is a pulse-shaped equivalent of the trigger input. The rising and falling edges correspond to the trigger level voltage passing through the threshold level set by the TRIG LEVEL control.

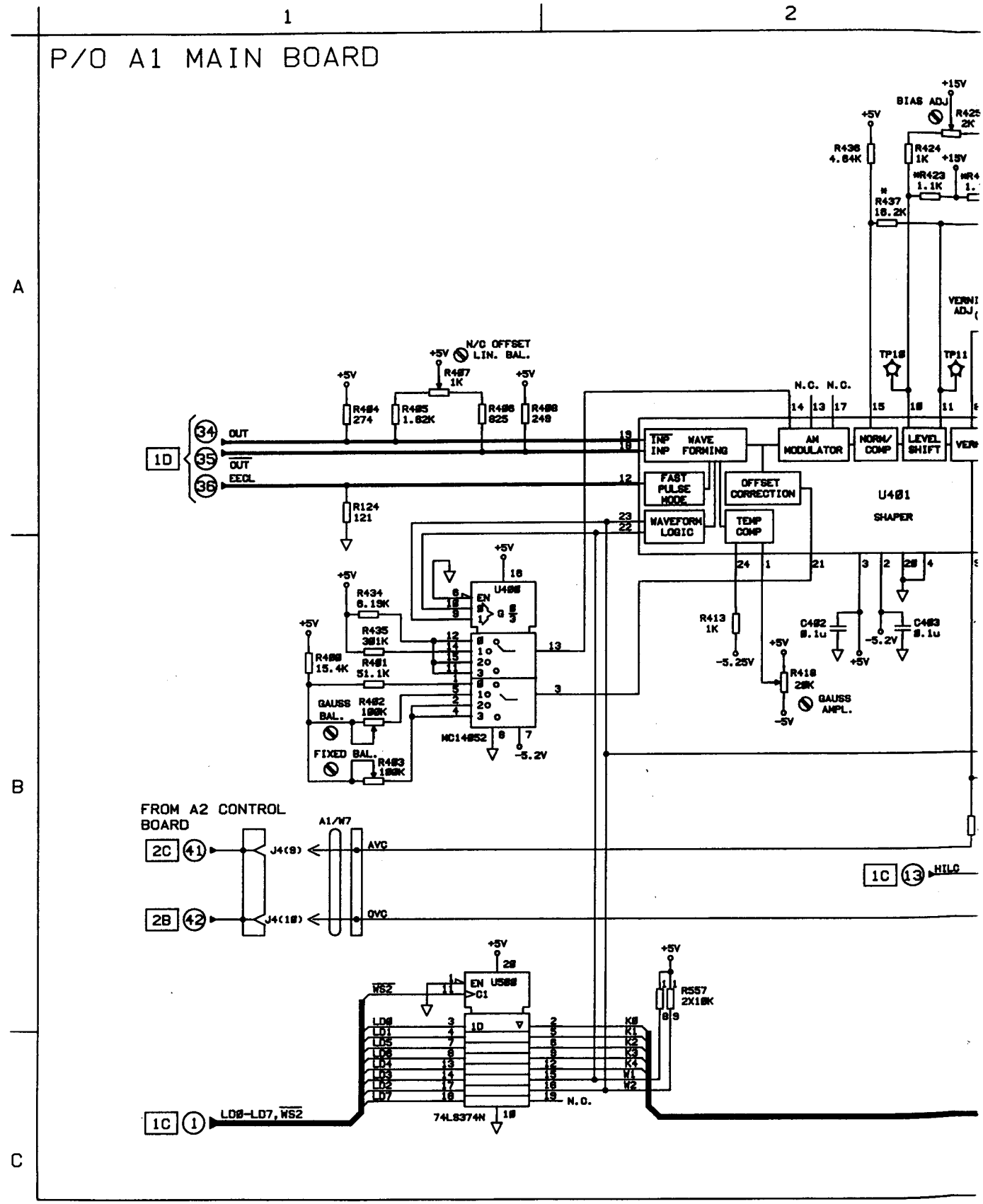
Level Check Circuit

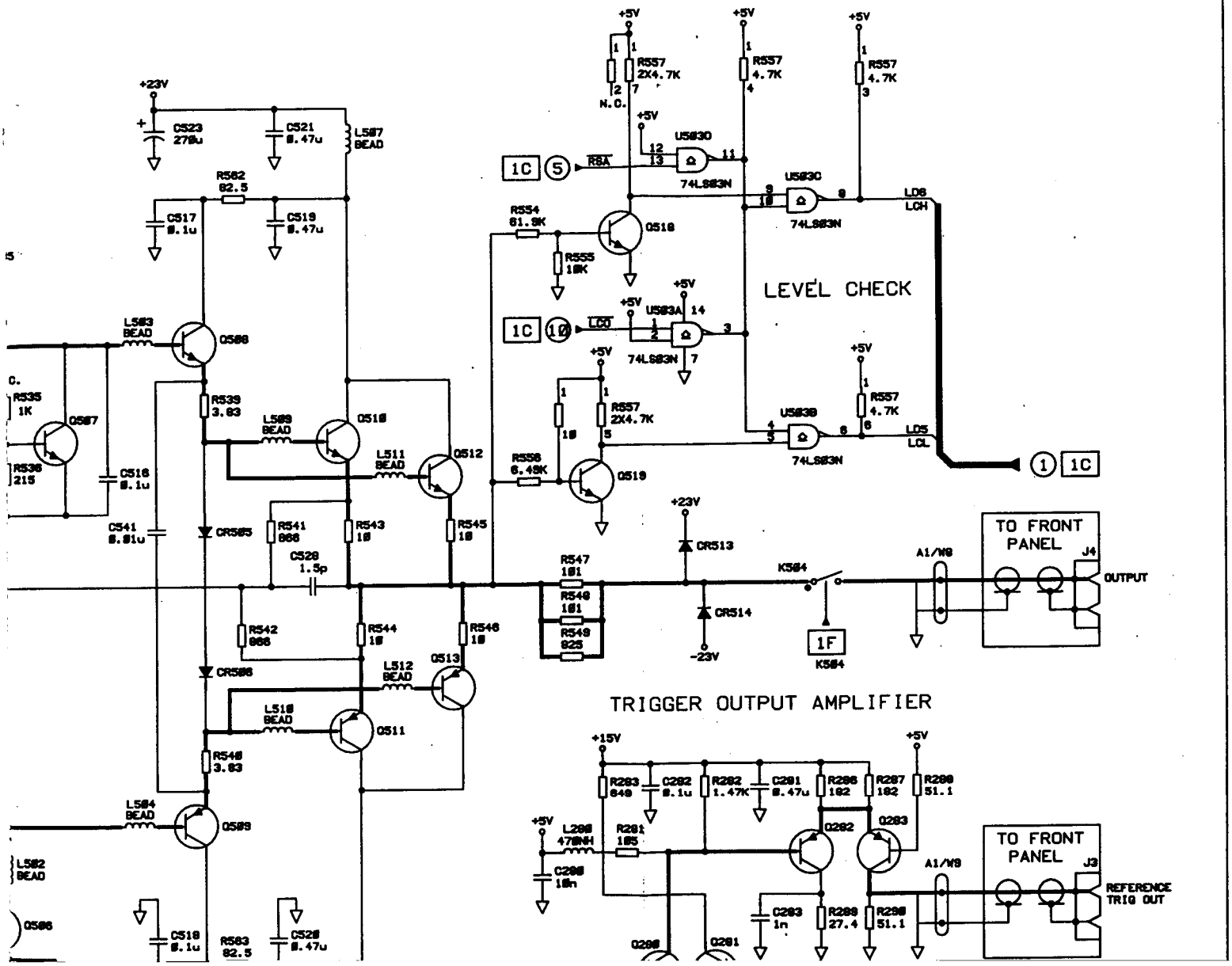
This circuit is used during instrument self-test which is performed at switch on, to verify the operation of the output amplifier and

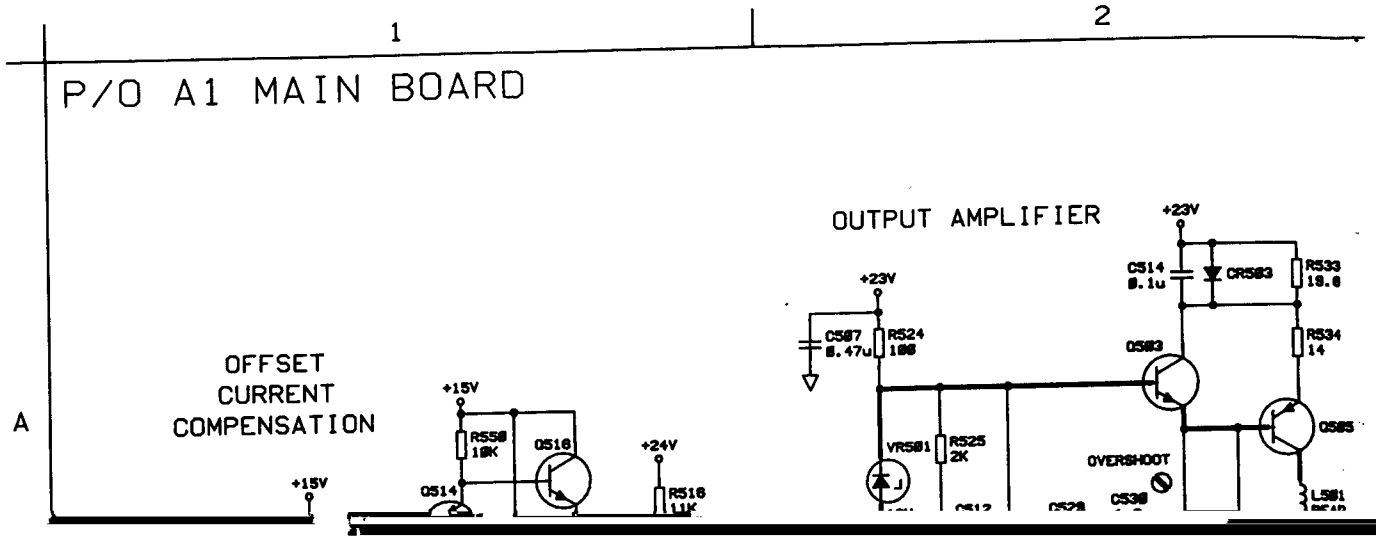


1F

MODEL HP8112A
FIGURE 10.4-4.
MAIN BOARD A1 SCHEMATIC 6


P/O A1 MAIN BOARD
1
2
A
B
C
+15V
BIAS ADJ
+5V
R436 4.64K
R424 1K
R423 1.1K
R437 16.2K
TP10
TP11
N/C OFFSET
LIN. BAL.
R407 1K
R404 274
R405 1.62K
R406 825
R408 249
1D
34 OUT
35 OUT
36 ECCL
R124 121
INP WAVE FORMING
AM MODULATOR
NORM/ COMP
LEVEL SHIFT
FAST PULSE MODE
WAVEFORM LOGIC
OFFSET CORRECTION
TEMP COMP
U401
SHAPER
N.C. N.C.
R434 6.19K
R435 301K
R436 15.4K
R431 51.1K
GAUSS BAL.
R432 100K
FIXED BAL.
R433 100K
U406
MC14052
-5.2V
R413 1K
-5.25V
C402 0.1u
C403 0.1u
R418 20K
GAUSS AMPL.
-5V
FROM A2 CONTROL BOARD
A1/W7
2C 41 J4(9) AVC
2B 42 J4(10) OVC
1C 13 HILO
U508
74LS374N
WS2
LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7
K0 K1 K2 K3 K4 W1 W2
R557 2X10K
N.C.
1C 1 LD0-LD7, WS2


LEVEL CHECK
TRIGGER OUTPUT AMPLIFIER
TO FRONT PANEL
OUTPUT
REFERENCE TRIG OUT
+23V
+5V
+15V
-23V
74LS83N
1C
1F
K584


1
2
P/O A1 MAIN BOARD
A
OFFSET
CURRENT
COMPENSATION
+15V
+15V
R556
19K
Q516
Q514
+24V
R516
11K
OUTPUT AMPLIFIER
+23V
+23V
C514
0.1u
CR583
R533
19.6
C587
0.47u
R524
100
Q583
R534
14
Q585
VR581
R525
2K
OVERSHOOT
Q538
L581

Troubleshooting

Note

- If an error code is being displayed by the HP 8112A you must press a key, [LCL] for example, to return the microprocessor to normal operation before troubleshooting.
- The component layout and locator for the main board A1 is at the end of this chapter.

Shaper IC Inputs

1. Set up the HP 8112A as follows:

RCL	0
Output	Enabled

2. Press the [SET] key
3. Use an oscilloscope to check the signals at pins 19 and 18 of U401 against Figure 10.4-6. Note that the signals on pins 18 and 19 are not necessarily symmetrical.

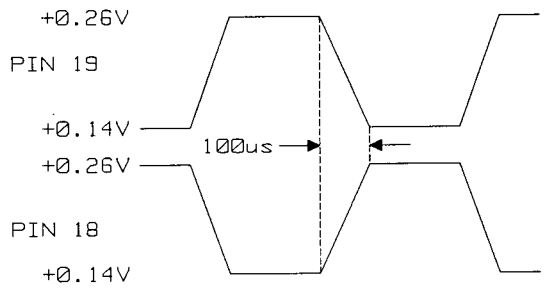


Figure 10.4-6. Shaper IC Input Signals on Pins 18/19

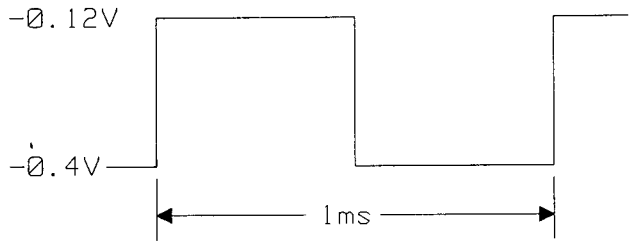


Figure 10.4-7. Shaper IC Output on Pin 12

4. Change the HP 8112A transition mode to FIXED.
5. Check the output on U401 pin 6 against Figure 10.4-8

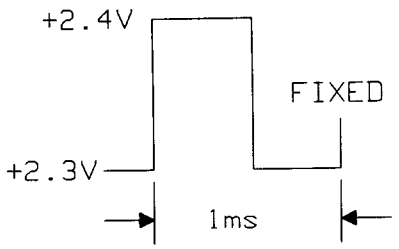


Figure 10.4-8. Shaper IC Output (FIXED)

6. Change the HP 8112A transition mode to LINEAR or GAUSSIAN.
7. Check the output on TP6 against Figure 10.4-9

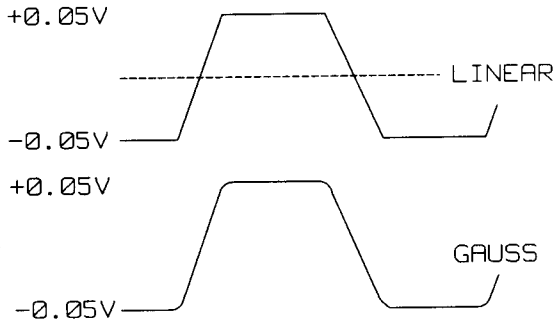


Figure 10.4-9. Shaper IC Output (LINEAR)

8. Change the HP 8112A HIL to +0.99 V and transition mode to FIXED.
9. Check the output on TP6 against Figure 10.4-10

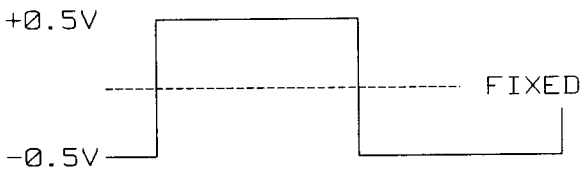


Figure 10.4-10. Shaper IC Output (FIXED, HIL +0.99 V)

Transition Mode and Output Control Signals

Check the logic levels on shaper IC pins for each type of transition and output mode, against Table 10.4-3:

Table 10.4-3. Waveform Control truth table

Transition Type	WF1 Pin 22	WF2 Pin 23	N/C Pin 19
Fixed	H	L	X
Linear	L	L	X
Gauss	H	L	X
Output Mode			
Norml	X	X	L
COMPL	X	X	H

Shaper IC Amplitude-vernier Control-voltage

Check the amplitude-vernier control-voltage with the HP 8112A HIL and LOL settings as indicated in Table 10.4-4. The voltage is measured at the board connector side of R422.

Table 10.4-4. Amplitude-vernier Control-voltages

HP 8112A Setting		Control voltage
HIL	LOL	at R422 (typ)
+0.5 V	−0.5 V	+5.03 V
+2.5 V	−2.5 V	+2.8 V
+4.99 V	−4.99 V	<10 mV

Shaper IC Reference Current

Shaper IC reference current (I_{ref}) can be checked by measuring the voltage across R411. The reading should be approximately 5.4 V which equates to I_{ref} of 2.5 mA.

Shaper IC Current-mirror

Check that the signal levels at the emitters of Q400A and Q400B are identical, as these transistors are a matched pair.

Pre-Attenuator and Output Attenuator Control Signals

Check the relay control signals $\overline{K0}$ –$\overline{K4}$ against Table 10.4-5:

Table 10.4-5. Attenuator Control truth table

Amplitude range	$\overline{K0}$	$\overline{K1}$	$\overline{K2}$	$\overline{K3}$	$\overline{K4}$
10.0 V – 16.0 V	H	H	H	L	L
1.00 V – 9.99 V	L	H	L	H	L
100 mV – 999 mV	L	L	H	H	L
Output Disabled	H	L	H	H	H

Offset-vernier Control-voltage

Check the offset-vernier control-voltage, received from the control board A2 at board connector side of R501, against Table 10.4-6:

Table 10.4-6. Offset-vernier Control-voltages

HP 8112A Setting		Control voltage
HIL	LOL	at R501 (typ)
+8.0 V	+7.9 V	−7.45 V
+5.5 V	+4.5 V	−4.8 V
+0.5 V	−0.5 V	< 10 mV
−4.5 V	−5.5 V	+4.8 V
−7.9 V	−8.0 V	+7.45 V

Output Amplifier

Caution

- Do not operate the HP 8112A without the heatsinks fitted on board A1
- If you need to replace one or more of the transistors Q505 – Q513, *do not attempt to remove the heatsink and transistor adaptors together, this is likely to damage the transistors.*

  1. Remove all the screws securing the heatsink(s).
  2. Remove the heatsink(s).
  3. Remove the adaptor(s) from the transistor(s) to be replaced.
  4. Replace the transistor(s).
  5. Re-fit the adaptor(s) and heatsink(s).

---

1. Set up the HP 8112A as follows:

RCL	0
LOL	−1 V
Output	Disabled

2. Press the [SET] key
3. Measure the voltage at CR501 and CR502 (typ. 10 mV):

   If it is fully negative (approximately -15 V) check U502, Q502, Q504 and Q506.

   If it is fully positive (approximately +15 V) check Q501, Q503, Q505 and U502.

4. Check if Q510/Q511 or Q512/Q513 have failed (emitter-collector short-circuit).

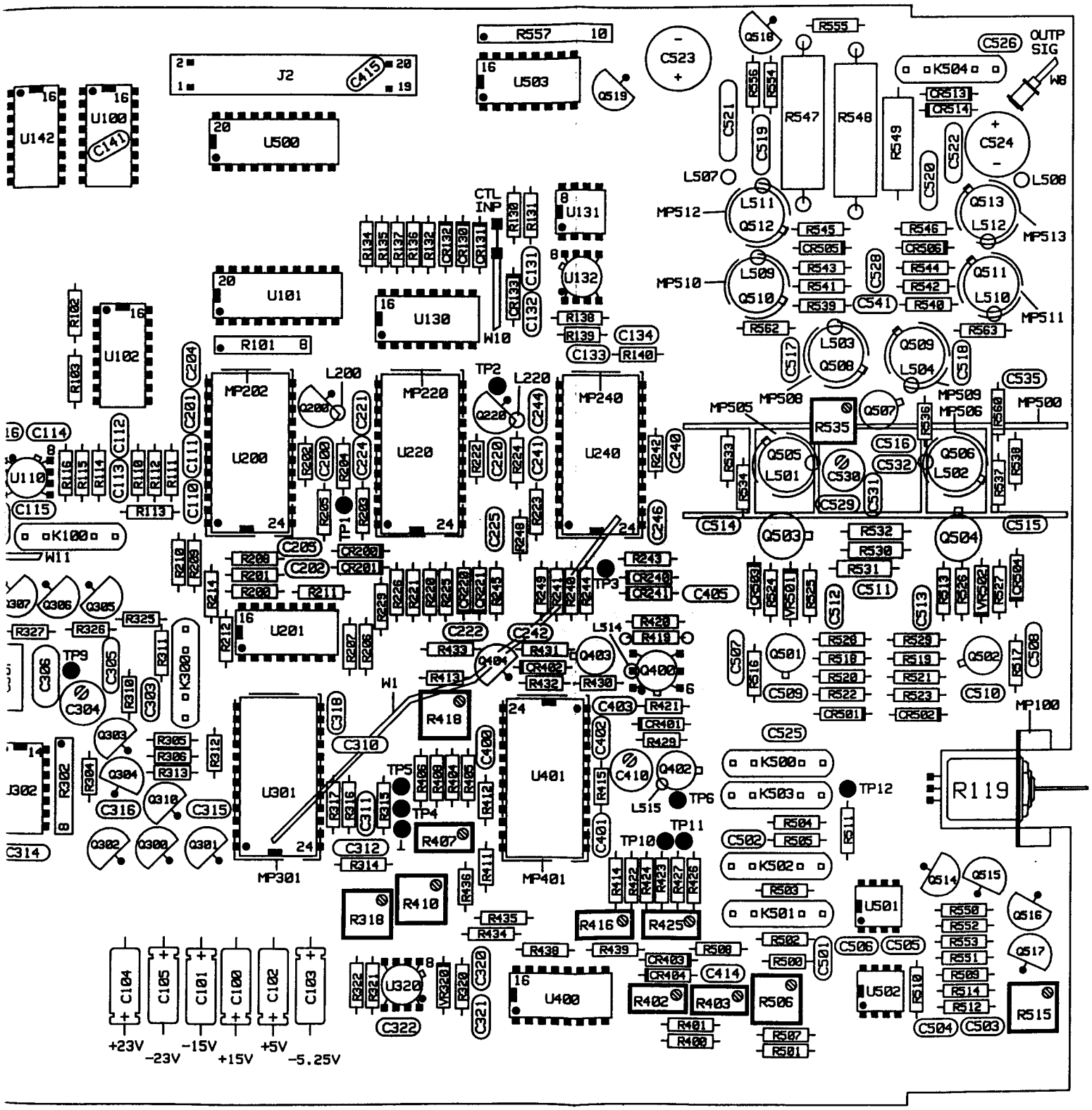
   If you need to change any of the output-stage transistors Q508 – Q513, also check CR505 and CR506. They protect the output stage at high amplitudes and frequencies by discharging the base-emitter capacitor of Q510 –Q513.

5. Set the HP 8112A to FIXED mode, output ENABLED.

6. Observe the main output using an oscilloscope and check the leading and trailing edges for distortion.
7. If there is distortion, check the output-amplifier input signal at TP4. Then do the following:
   a. Set up the HP 8112A as follows:

HIL	+8.0 V
LOL	−8.0 V

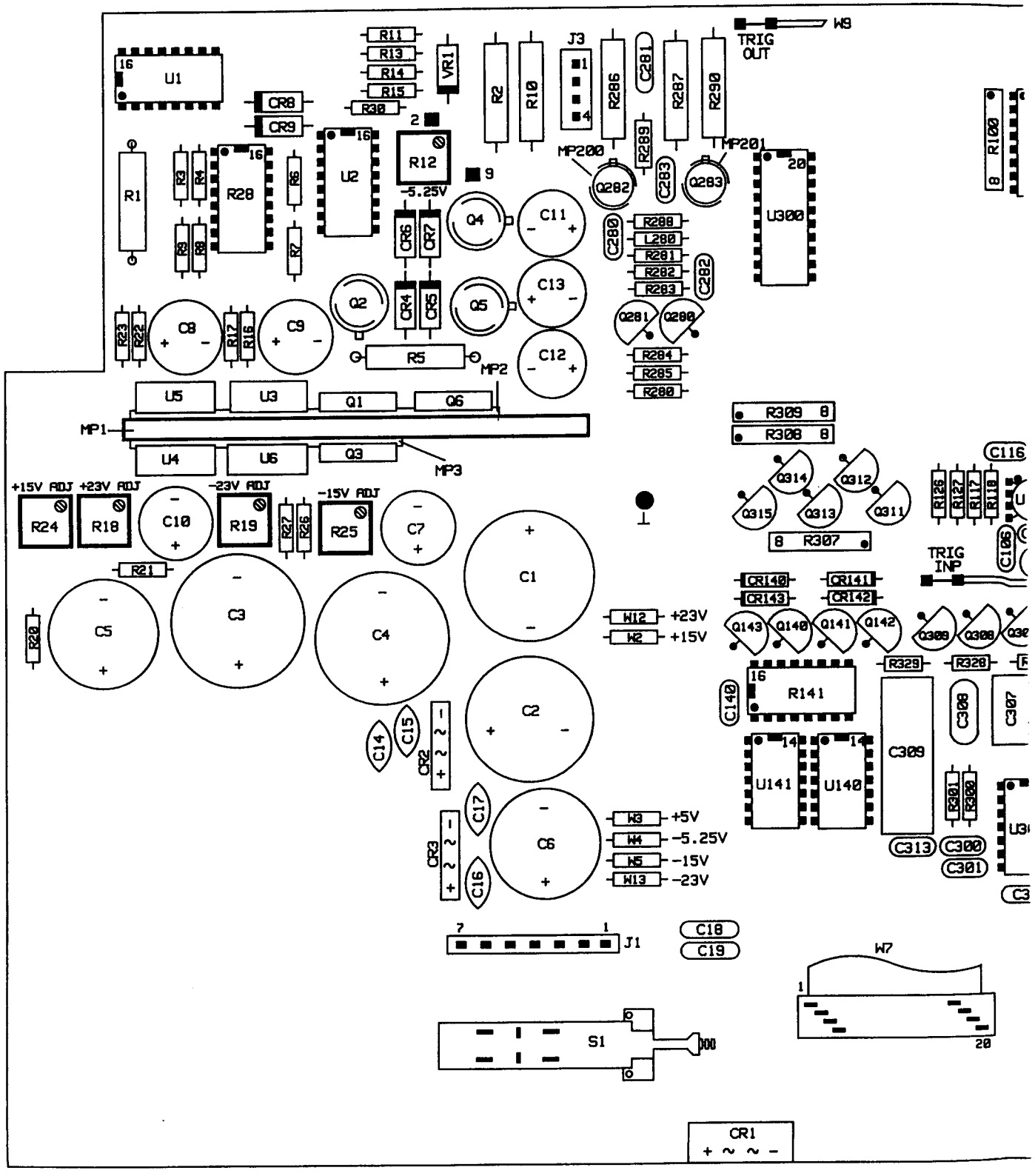
   b. If the input signal is clean but the leading edge of the output signal is distorted, check Q503 and Q505.
   c. If the trailing edge is distorted, check Q504 and Q506.



NOTE: C141,C415,W1 FITTED ON THE NON. COMPONENT SIDE OF THE BOARD
C141 FITTED UNDER IC U100, C415 FITTED UNDER CONNECTOR J2
C245,C409,C554,C336,R437 NOT ALWAYS FITTED

FIGURE 10.4-11. MAIN BOARD A1 COMPONENT LAYOUT
SERVICING THE SHAPER AND OUTPUT AMPLIFIER

A1 BD AY MAIN


A
B
1
2
U1
U2
U3
U4
U5
U6
U141
U140
U300
R1
R2
R10
R11
R12
R13
R14
R15
R24
R18
R19
R25
R28
R30
R100
R126
R127
R112
R118
R141
R286
R287
R290
R289
R307
R308
R309
R328
R329
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C15
C16
C17
C18
C19
C116
C140
C300
C301
C307
C308
C309
C313
Q1
Q2
Q3
Q4
Q5
Q6
Q140
Q141
Q142
Q143
Q280
Q281
Q282
Q283
Q311
Q312
Q313
Q314
Q315
VR1
J1
J3
S1
W2
W3
W4
W5
W7
W8
W12
W13
MP1
MP2
MP3
MP200
MP201
TRIG OUT
TRIG INP
+15V ADJ
+23V ADJ
-23V ADJ
-15V ADJ
-5.25V
+23V
+15V
+5V
-5.25V
-15V
-23V
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR140
CR141
CR142
CR143

REF. DES.	GRID LOC.
C1	B2
C2	B2
C3	A2
C4	A2
C5	A2
C6	B2
C7	A1
C8	A1
C9	A1
C10	A1
C11	B1
C12	B1
C13	B1
C14	A2
C15	A2
C16	A2
C17	A2
C18	B2
C19	B2
C100	C2
C101	C2
C102	C2
C103	C2
C104	C2
C105	C2
C106	B2
C110	C1
C111	C1
C112	B1
C113	B1
C114	B1
C115	B2
C116	B1
C131	C1
C132	C1
C133	C1
C134	C1
C140	B2
C141	B1
C200	C1
C201	C1
C202	C2
C204	C1
C205	C1
C220	C1
C221	C1
C222	C2
C224	C1
C225	C1
C240	C1
C241	C1
C242	C2
C244	C1
C245	C1
C246	C1
C280	B1
C281	B1
C282	B1
C283	B1
C300	B2
C301	B2
C303	C2
C304	B2
C305	B2
C306	B2
C307	B2
C308	B2
C309	B2
C310	C2
C311	C2
C312	C2
C313	B2
C314	B2
C315	C2
C316	B2
C318	C2
C320	C2
C321	C2
C322	C2
C400	C2
C401	C2
C402	C2
C403	C2
C405	D2
C409	C2
C410	C2
C414	D2
C415	C1
C501	D2
C502	D2
C503	D2
C504	D2
C505	D2
C506	D2
C507	D2
C508	D2
C509	D2
C510	D2
C511	D2
C512	D2
C513	D2
C514	D2
C515	D2
C516	D1
C517	D1
C518	D1
C519	D1
C520	D1
C521	D1
C522	D1
C523	C1
C524	D1
C525	D2
C526	D1
C528	D1
C529	D1
C530	D2
C531	D1
C532	D1
C535	D1
C541	D1
C554	D2
C556	D2
CR1	B2
CR2	A2
CR3	A2
CR4	A1
CR5	A1
CR6	A1
CR7	A1
CR8	A1
CR9	A1
CR130	C1
CR131	C1
CR132	C1
CR133	C1
CR140	B2
CR141	B2
CR142	B2
CR143	B2
CR200	C2
CR201	C2
CR220	C2
CR221	C2
CR240	C2
CR241	C2
CR401	C2
CR402	C2
CR403	C2
CR404	C2
CR501	D2
CR502	D2
CR503	D2
CR504	D2
CR505	D1
CR506	D1
CR513	D1
CR514	D1
J1	B2
J2	C1
J3	B1
K100	B2
K300	C2
K500	D2
K501	D2
K502	D2
K503	D2
K504	D1
L200	C1
L220	C1
L280	B1
L501	D1
L502	D1
L503	D1
L504	D1
L507	D1
L508	D1
L509	D1
L510	D1
L511	D1
L512	D1
L514	C2
L515	C2
MP1	A1
MP2	A1
MP3	A1
MP100	D2
MP200	B1
MP201	B1
MP202	C1
MP220	C1
MP240	C1
MP301	C2
MP401	C2
MP500	D1
MP505	D1
MP506	D1
MP508	D1
MP509	D1
MP510	D1
MP511	D1
MP512	D1
MP513	D1
Q1	A1
Q2	A1
Q3	A1
Q4	A1
Q5	A1
Q6	A1
Q140	B2
Q141	B2
Q142	B2
Q143	B2
Q200	C1
Q220	C1
Q280	B1
Q281	B1
Q282	B1
Q283	B1
Q300	C2
Q301	C2
Q302	B2
Q303	B2
Q304	B2
Q305	B2
Q306	B2
Q307	B2
Q308	B2
Q309	B2
Q310	B2
Q311	B1
Q312	B1
Q313	B1
Q314	B1
Q315	B1
Q400	C2
Q402	C2
Q403	C2
Q404	C2
Q501	D2
Q502	D2
Q503	D2
Q504	D2
Q505	D1
Q506	D1
Q507	D1
Q508	D1
Q509	D1
Q510	D1
Q511	D1
Q512	D1
Q513	D1
Q514	D2
Q515	D2
Q516	D2
Q517	D2
Q518	D1
Q519	D1
R1	A1
R2	A1
R3	A1
R4	A1
R5	A1
R6	A1
R7	A1
R8	A1
R9	A1
R10	A1
R11	A1
R12	A1
R13	A1
R14	A1
R15	A1
R16	A1
R17	A1
R18	A1
R19	A1
R20	A2
R21	A2
R22	A1
R23	A1
R24	A1
R25	A1
R26	A1
R27	A1
R28	A1
R30	A1
R100	B1
R101	C1
R102	B1
R103	B1
R110	C1
R111	C1
R112	C1
R113	C2
R114	B1
R115	B1
R116	B1
R117	B1
R118	B1
R119	D2
R126	B1
R127	B1
R130	C1
R131	C1
R132	C1
R134	C1
R135	C1
R136	C1
R137	C1
R138	C1
R139	C1
R140	C1
R141	B2
R200	C2
R201	C2
R202	C1
R203	C2
R204	C1
R205	C2
R206	C2
R207	C2
R208	C2
R209	C2
R210	C2
R211	C2
R212	C2
R214	C2
R220	C2
R221	C2
R222	C1
R223	C1
R224	C1
R225	C2
R226	C2
R229	C2
R240	C2
R241	C2
R242	C1
R243	C2
R244	C2
R245	C2
R248	C1
R249	C2
R280	B1
R281	B1
R282	B1
R283	B1
R284	B1
R285	B1
R286	B1
R287	B1
R288	B1
R289	B1
R290	B1
R300	B2
R301	B2
R302	B2
R304	B2
R305	C2
R306	C2
R307	B1
R308	B1
R309	B1
R310	B2
R311	C2
R312	C2
R313	C2
R314	C2
R315	C2
R316	C2
R317	C2
R318	C2
R320	C2
R321	C2
R322	C2
R325	B/C2
R326	B2
R327	B2
R328	B2
R329	B2
R400	C2
R401	C2
R402	C2
R403	D2
R404	C2
R405	C2
R406	C2
R407	C2
R408	C2
R410	C2
R411	C2
R412	C2
R413	C2
R414	C2
R415	C2
R416	C2
R418	C2
R419	C2
R420	C2
R421	C2
R422	C2
R423	C2
R424	C2
R425	C2
R426	C2
R427	C2
R429	C2
R430	C2
R431	C2
R432	C2
R433	C2
R434	C2
R435	C2
R436	C2
R437	C2
R438	C2
R439	C2
R500	D2
R501	D2
R502	D2
R503	D2
R504	D2
R505	D2
R506	D2
R507	D2
R508	D2
R509	D2
R510	D2
R511	D2
R512	D2
R513	D2
R514	D2
R515	D2
R516	D2
R517	D2
R518	D2
R519	D2
R520	D2
R521	D2
R522	D2
R523	D2
R524	D2
R525	D2
R526	D2
R527	D2
R528	D2
R529	D2
R530	D2
R531	D2
R532	D1
R533	D1
R534	D1
R535	D1
R536	D1
R537	D1
R538	D1
R539	D1
R540	D1
R541	D1
R542	D1
R543	D1
R544	D1
R545	D1
R546	D1
R547	D1
R548	D1
R549	D1
R550	D2
R551	D2
R552	D2
R553	D2
R554	D1
R555	D1
R556	D1
R557	C1
R560	D1
R562	D1
R563	D1
S1	B2
TP1	C2
TP2	C1
TP3	C2
TP4	C2
TP5	C2
TP6	C2
TP9	B2
TP10	C2
TP11	C2
TP12	D2
U1	A1
U2	A1
U3	A1
U4	A1
U5	A1
U6	A1
U100	C1
U101	C1
U102	B1
U1[illegible]0	B1
U130	C1
U131	C1
U132	C1
U140	B2
U141	B2
U142	B1
U200	C1
U201	C2
U220	C1
U240	C1
U300	B1
U301	C2
U302	B2
U320	C2
U400	C2
U401	C2
U500	C1
U501	D2
U502	D2
U503	C1
VR1	A1
VR320	C2
VR501	D2
VR502	D2
W1	C2
W2	B2
W3	B2
W4	B2
W5	B2
W7	B2
W8	D1
W9	B1
W10	C1
W11	B2
W12	B2
W13	B2

FIGURE 10.4-12. MAIN BOARD A1 COMPONENT LOCATOR

10.5

Servicing the Control Board

Theory of Operation

Introduction

The main function of the control board A2 is to convert digital control data into analog control signals used on the main board A1. The main board supplies power to the control board and the microprocesor board A3 supplies the digital control data. The standard control board is divided into the following areas:

- Timer circuit
- Address decoders
- Timing range decoder
- DAC Reference circuit
- Digital to Analog Converters (DACs)
- Byte Offset and Offset DAC
- Parameter control

Timer

Refer to Figure 10.5-3. The timer circuit, U26 and associated components, provides the Non-Maskable Interrupt signal NMI, used by the microprocessor to produce the flashing error display when an error condition is detected. The 555 timer is configured as an astable multivibrator which produces an output of approximately 100 Hz when enabled when $\overline{\text{TIRE}}$ is active (low).

RESET is held high for a short time at instrument switch on, to disable the timer so that NMI cannot be transmitted before the power supplies have settled.

Note

If an error code is shown in the display, it is necessary to press a key, e.g. [LCL], to set the microprocessor to normal, then commence troubleshooting.

Address Decoders

Refer to Figure 10.5-3. Local address decoding is performed by U1 and U16. Both decoders share LA3 - LA5 from the microprocessor board as address inputs, $\overline{\text{WS5}}$ enables decoder U1 and $\overline{\text{WS4}}$ enables decoder U16. The decoder outputs enable the various devices on the latched-data bus LD0—LD7.

Timing Range Decoder

The timing range decoder U2, controlled by $\overline{RCT}$ from U1, latches data from the data bus which is then used to select the timing ranges required by the period, delay, width and transition time control sources.

DAC Reference Circuit

Refer to Figure 10.5-4. The references are used by DACs. Op amps U10A and U10B with associated components, provide constant current sources of −9 V and −1 V, derived from the −15 V and +5 V supplies.

Digital to Analog Converters

Normal operation

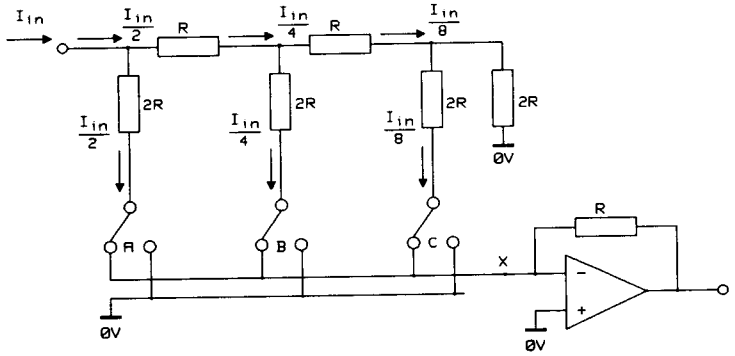


Figure 10.5-1. Principle of DAC Operation

The amplitude control DAC (U23) operates on the principle summarised in Figure 10.5-1. The current I_{in} comes from a reference voltage and is repeatedly divided by two at each branch of the resistance network. This process provides a series of binary current-fractions which are switched to ground or the summing point X. Each switch is operated by the data bit which has the same significance as the current it controls (A=Most Significant Bit). The total current summed at X therefore represents the data value as a fraction of I_{in}. For example, in Figure 10.5-1 with all three switches on (all three data bits on):

$$I_X = \frac{I_{in}}{2} + \frac{I_{in}}{4} + \frac{I_{in}}{8} = \frac{7}{8} I_{in}$$

Reciprocal operation

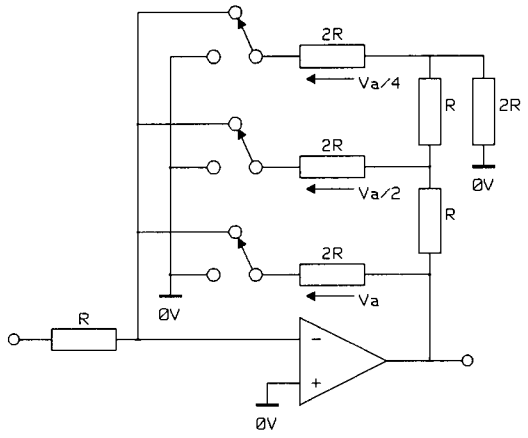


Figure 10.5-2. DAC - Reciprocal operation

The remaining DACs operate in a similar manner to the amplitude control but are set up to produce an output which is the reciprocal of the input value. Refer to Figure 10.5-2. The currents summed at the inverting input of the op-amp can be expressed as:

$$\frac{V_a}{2R} + \frac{V_a}{4R} + \frac{V_a}{8R} = -\frac{V_{ref}}{R}$$

Therefore:

$$V_a = -\frac{8}{7}V_{ref}$$

Byte offset latches and Offset DAC

Note

Although this description describes output in terms of offset and amplitude, instrument output levels are programmed as high and low levels (HIL, LOL).

Refer to Figure 10.5-4 and Figure 10.5-1.

Byte Latching

U20 has no internal latches and, since the DAC output must be available continuously and simultaneously with the amplitude DAC output, external latches are provided (See Figure 10.5-3). The low and high bytes of the offset value are loaded seperately from the latched-data bus into latches U19 and U17 using the negative edges of $\overline{\text{LBO}}$ and $\overline{\text{HBO}}$ to enable the latches. The $\overline{\text{LRC}}$ ($\overline{\text{WS2}}$) signal is then used to pass the data to U20 via U27 and U18 simultaneously as a 12-bit word. The $\overline{\text{LRC}}$ signal is also inverted by U15 and used to enable the amplitude DAC U23. Therefore the microprocessor can prepare new data for U20 and U23 before enabling both with $\overline{\text{WS2}}$.

The time difference between LRC, enabling U23, and $\overline{\text{LRC}}$, enabling new data for U20, is the propagation delay through U19.

Offset DAC

The offset level output from U21 can be attenuated using R42.

The offset DAC U20 is a 12-bit multiplying device which provides two output currents. I_{out1} is the summed current derived from the reference voltage via the selected $\frac{R}{2R}$ networks. (I_X in "Digital to Analog Converters"). I_{out2} is the sum of the unselected currents and hence:

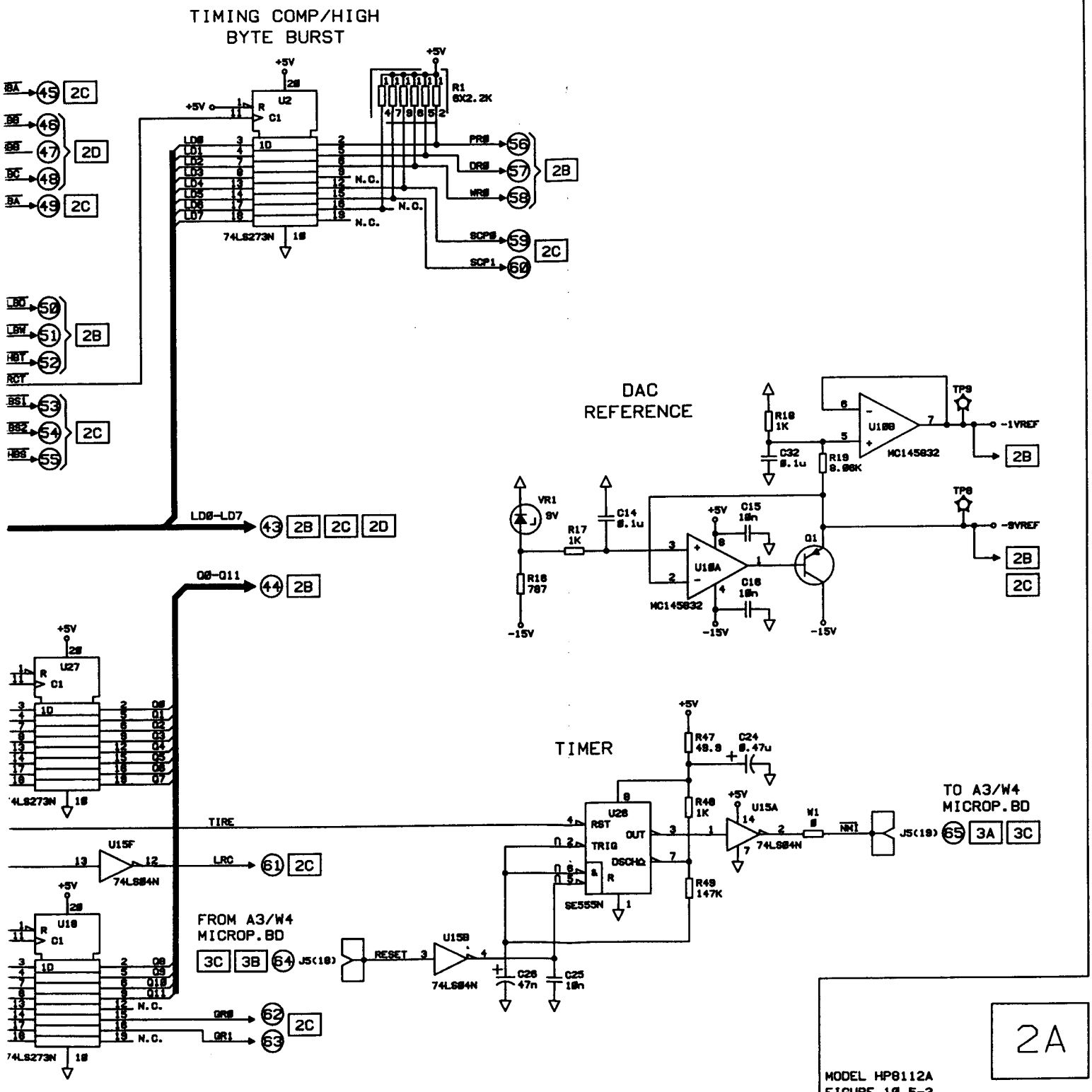
$$I_{out1} + I_{out2} = I_{in}$$

Parameter Control

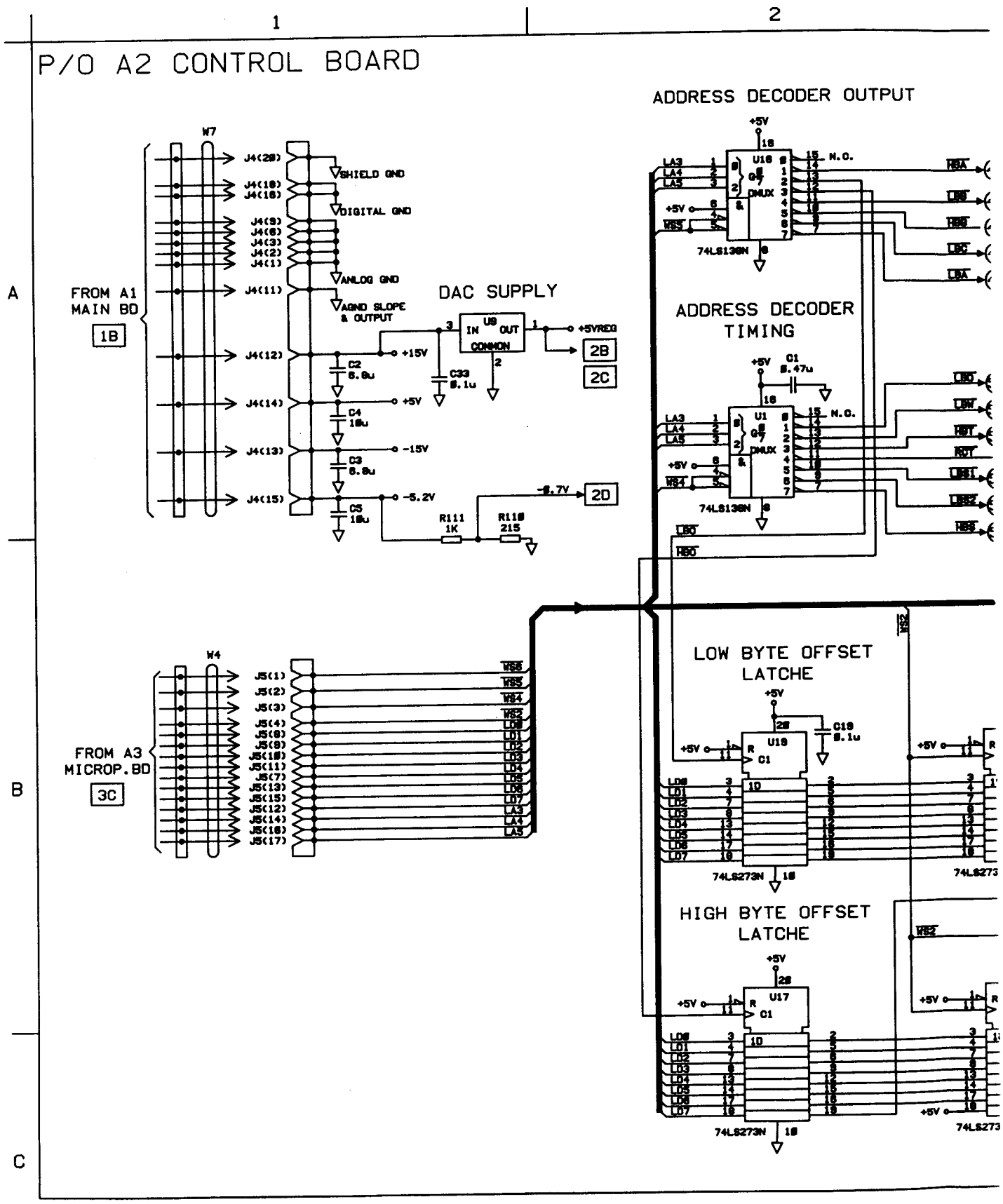
The remaining DACs, U4-U6, U12, U13 and U23, convert the digital vernier values input to the microprocessor from the instrument front panel or system controller, into analogue signals for use by:

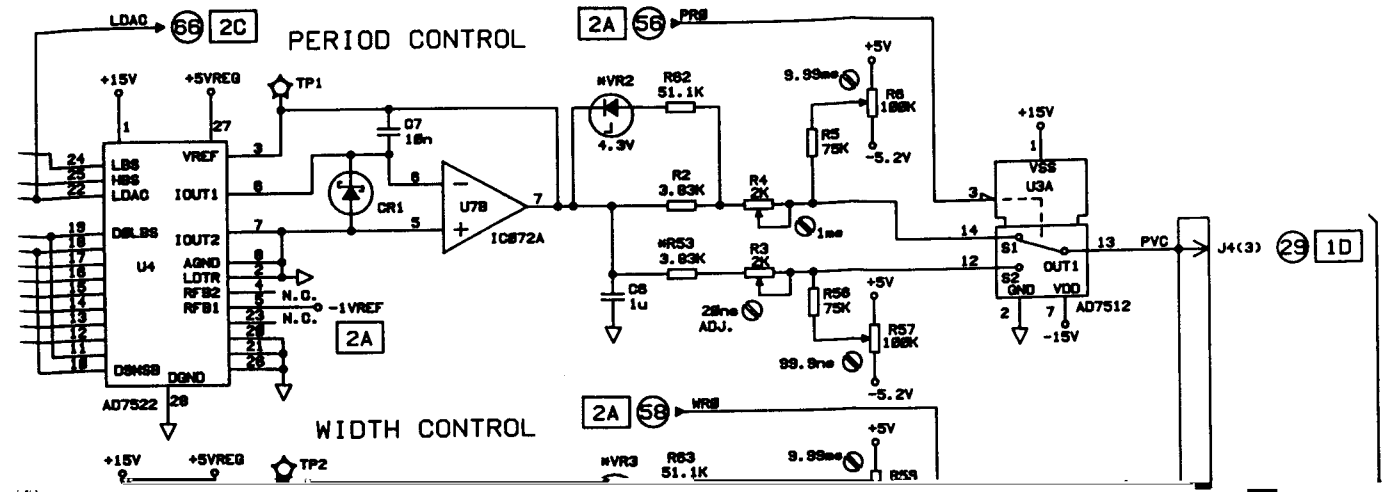
- Timing ICs on A1 Main Board which generate the required period, delay and width delay signals.
- Slope IC on A1 Main Board which generates the leading and trailing edges of the output pulse.
- Shaper IC on the A1 Main Board which governs the final amplitude of the output pulse.

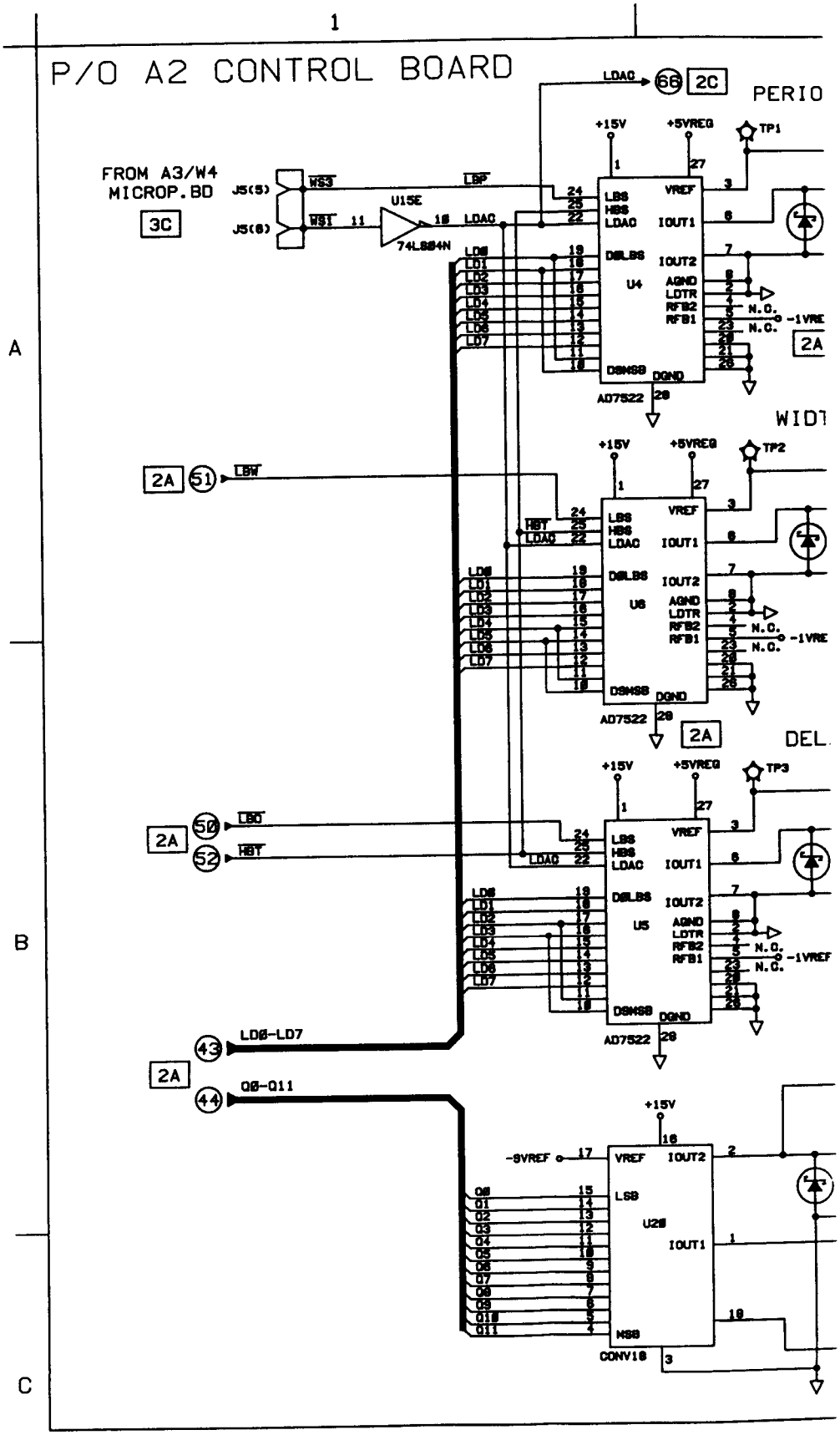
Range switching circuits are included in the outputs of these DACs, that are selected automatically by the microprocessor in conjunction with the Timing range decoder.

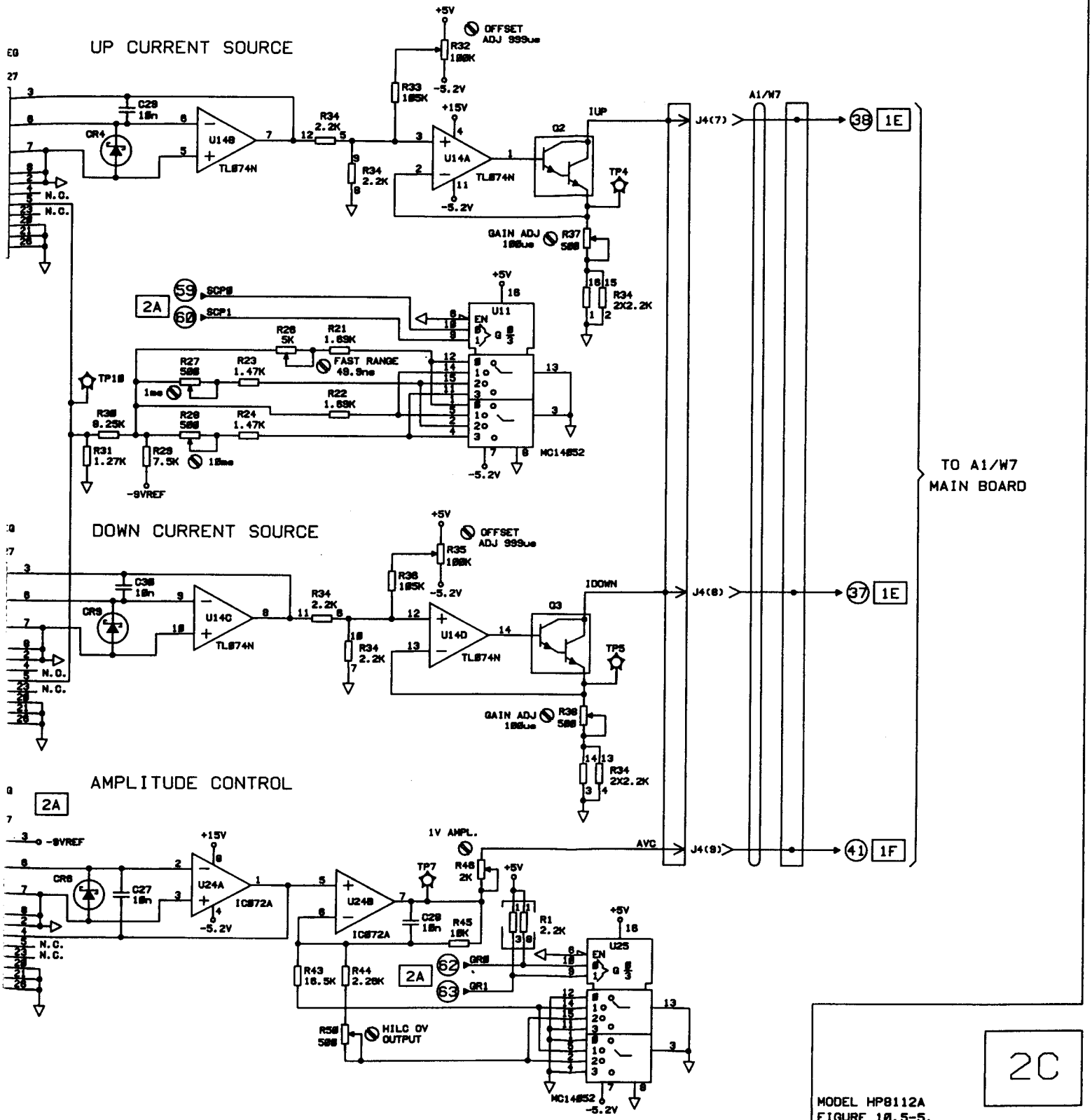


MODEL HP8112A
FIGURE 10.5-3.
CONTROL BD A2 SCHEMATIC 1


1
2
A
B
C
P/O A2 CONTROL BOARD
ADDRESS DECODER OUTPUT
W7
FROM A1
MAIN BD
1B
J4(28)
J4(18)
J4(16)
J4(9)
J4(6)
J4(3)
J4(2)
J4(1)
J4(11)
J4(12)
J4(14)
J4(13)
J4(15)
SHIELD GND
DIGITAL GND
ANLOG GND
AGND SLOPE
& OUTPUT
DAC SUPPLY
U9
IN
OUT
COMMON
+5VREG
+15V
+5V
-15V
-5.2V
-8.7V
C2
6.8u
C33
0.1u
C4
10u
C3
6.8u
C5
10u
R111
1K
R118
215
2B
2C
2D
+5V
U16
74LS138N
LA3
LA4
LA5
DMUX
N.C.
HBA
HBB
HBC
LBA
ADDRESS DECODER
TIMING
C1
0.47u
U1
LBC
LBB
HBT
HCT
LBT1
LBT2
HBT
LB0
HB0
W4
FROM A3
MICROP.BD
3C
J5(1)
J5(2)
J5(3)
J5(4)
J5(8)
J5(9)
J5(10)
J5(11)
J5(7)
J5(13)
J5(15)
J5(12)
J5(14)
J5(16)
J5(17)
WS6
WS5
WS4
WS2
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LA3
LA4
LA5
LOW BYTE OFFSET
LATCHE
U19
C19
0.1u
74LS273N
74LS273
HIGH BYTE OFFSET
LATCHE
U17

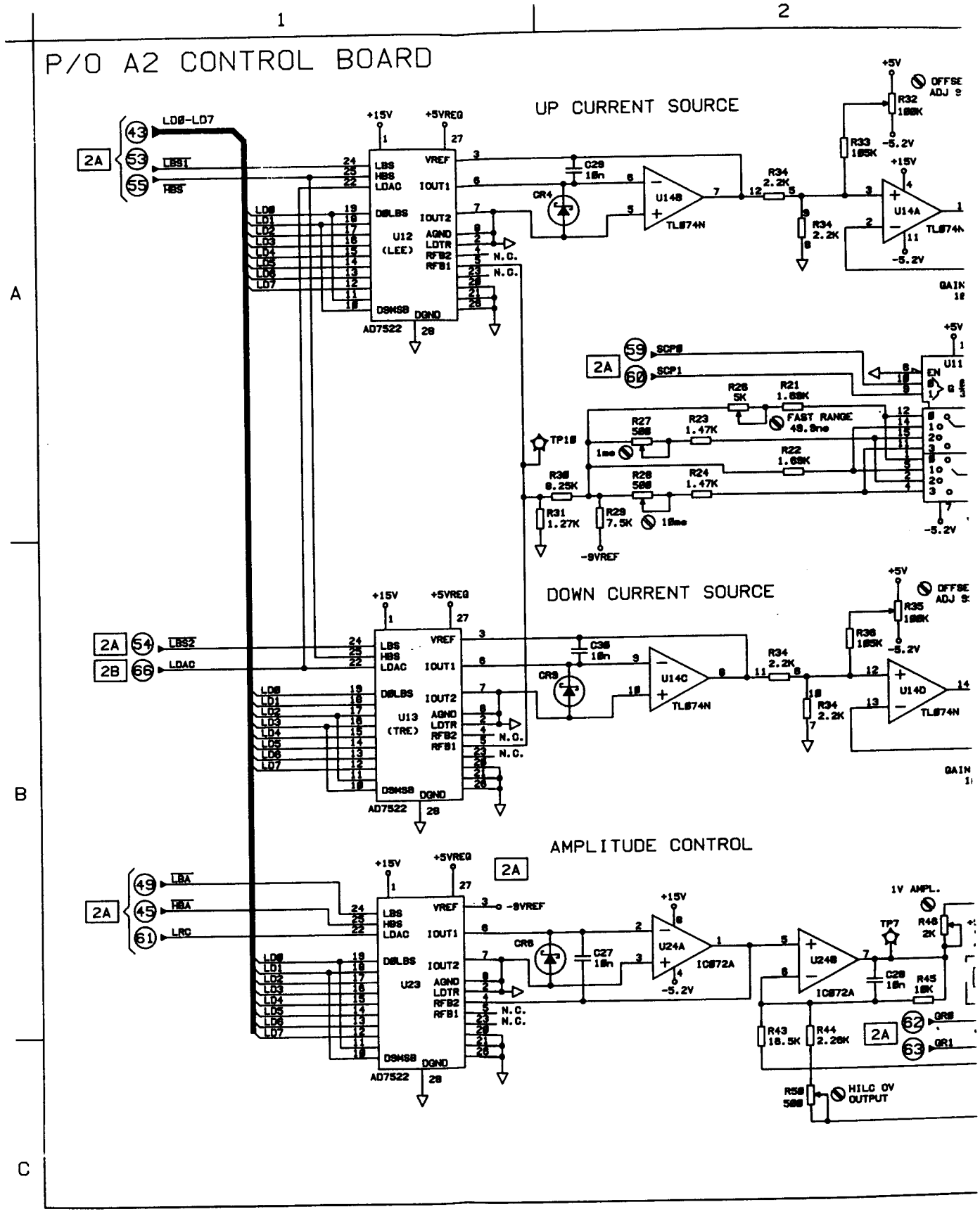

LDAC
PERIOD CONTROL
+15V
+5VREG
TP1
VREF
LBS
HBS
LDAC
IOUT1
IOUT2
DBLBS
DBHBS
AGND
LDTR
RFB2
RFB1
N.C.
N.C.
-1VREF
DGND
AD7522
C7 15n
CR1
U7B
IC672A
#VR2
R62 51.1K
4.3V
R2 3.83K
R4 2K
R5 75K
R6 100K
9.99ms
+5V
-5.2V
1ms
#R53 3.83K
R3 2K
C8 1u
25ms ADJ.
R56 75K
R57 100K
99.9ms
PRB
WRB
WIDTH CONTROL
TP2
#VR3
R63 51.1K
R58
VSS
U3A
S1
S2
GND
VDD
OUT1
AD7512
PVC
J4(3)
1D
2A
2C


1
P/O A2 CONTROL BOARD
A
B
C
FROM A3/W4
MICROP.BD
3C
J5(5)
J5(6)
WS3
WS1
LBP
U15E
74LS84N
LDAC
66
2C
PERIO
+15V
+5VREG
TP1
LBS
HBS
LDAC
VREF
IOUT1
IOUT2
DBLBS
U4
AGND
LDTR
RFB2
RFB1
N.C.
-1VRE
DBMSB
DGND
AD7522
2A
WID
TP2
2A
51
LBW
HBT
U6
2A
DEL
TP3
2A
50
LBO
52
HBT
U5
-1VREF
43
LD0-LD7
2A
44
Q0-Q11
-8VREF
U2#
CONV16
3



2C

MODEL HP8112A
FIGURE 10.5-5.
CONTROL BD A2 SCHEMATIC 3


P/O A2 CONTROL BOARD
UP CURRENT SOURCE
DOWN CURRENT SOURCE
AMPLITUDE CONTROL
LD0-LD7
LBS1
HBS
LBS2
LDAC
SCP0
SCP1
U12 (LEE)
U13 (TRE)
U23
AD7522
TL074N
IC872A
FAST RANGE
1V AMPL.
HILC 0V OUTPUT
-9VREF
+15V
+5V
-5.2V
N.C.
1
2

Troubleshooting

Note

- If an error code is being displayed by the HP 8112A you must press a key, [LCL] for example, to return the microprocessor to normal operation before troubleshooting.
- The component layout and locator for the standard control board A2 is at the end of the chapter.

Verify the following voltages:

- DAC supply U9 pin 2: +5 V
- DAC reference TP9: −1 V
- DAC reference TP8: −9 V

Timer

1. Set up the HP 8112A as follows:

RCL	0
PER	10 μs

2. Check that pin 3 of U26 is delivering a signal of approximately 100 Hz.

Address Decoders

The address decoders can be checked using signature analysis:

1. Set the microprocessor to free run mode as follows:
   a. Set the P1 wire on board A3 (See Chapter 10.7) to position **P1**.
   b. Disconnect Jumper A2W1.
   c. Connect RES on A3 to ground for a short time to ensure the microprocessor is reset.
   d. Connect the signature analyser ground to the Control Board ground and connect the probes as follows:

Sig. Analyser	**A3 μP Board Connections**
Start ƒ	TP "SA"
Stop ƒ	TP "SP"
Clock ⌇	TP "E"

   e. Verify that the reading at the Microprocessor +5 V is 0003. If it is not, then the microprocessor is not free running.
   f. Check the signatures of U1, U15 and U16 against those given in Table 10.5-1

Table 10.5-1. A2 Address Decoder Signatures

U1 pin	Mnemonic	Description	Free run S.A.	Area
7	$\overline{\text{HBS}}$	High Byte Slope	HHF2	U12,U13/25
9	$\overline{\text{LBS2}}$	Low Byte Slope (TRE)	63A2	U13/24
10	$\overline{\text{LBS1}}$	Low Byte Slope (LEE)	FAFP	U12/24
11	$\overline{\text{RCT}}$	Range Compensation	9CPH	U2/11
12	$\overline{\text{HBT}}$	High Byte Timing	0P16	U4,U5,U6/25
13	$\overline{\text{LBW}}$	Low Byte Width	FP31	U6/24
14	$\overline{\text{LBD}}$	Low Byte Delay	509H	U5/24
$\overline{\text{WS3}}$	$\overline{\text{LPB}}$	Low Byte Period	79HU	U4/24
LA3		Sub coded address	050H	U1,U16/1
LA4		Sub coded address	CH9U	U1,U16/2
LA5		Sub coded address	8759	U1,U16/3
$\overline{\text{WS4}}$		Sub coded address	55F4	U1/4,5
$\overline{\text{WS5}}$		Sub coded address	8U95	U16/4,5
U16 Pin				
7	$\overline{\text{LBA}}$	Low Byte Amplitude	F2F2	U23/24
14	$\overline{\text{HBA}}$	High Byte Amplitude	P10H	U23/25
13	$\overline{\text{LBO}}$	Low Byte Offset	F491	U19/11
12	$\overline{\text{HBO}}$	High Byte Offset	27A6	U17/11

Timing Ranges

Measure levels at U2 Timing Range Decoder IC against readings in Table 10.5-2

Table 10.5-2. Timing range decoder

Timing Range Decoder U2		Pin 2 PR0	Pin 5 DR0	Pin 6 WR0	Pin 12 SCP0	Pin15 SCP1
Period range 1	PER 20 ns-99.9 ns	L				
all other ranges	PER 100 ns-950 ms	H				
Double range 1	DBL 20 ns-99.9 ns		L			
all other ranges	DBL 100 ns-950 ms		H			
Width range 1	WID 20 ns-99.9 ns			L		
all other ranges	WID 100 ns-950 ms			H		
Slope range 1	LEE=TRE 5.5 ns-99.9 ns				L	L
Slope range 2	LEE=TRE 50 ns-999 ns				H	L
Slope range 3	LEE=TRE 0.5 μs-9.99 μs				H	L
Slope range 4	LEE=TRE 5 μs-99.9 μs				H	L
Slope range 5	LEE=TRE 50 μs-999 μs				H	L
Slope range 6	LEE=TRE 0.5 ms-9.99 ms				L	H
Slope range 7	LEE=TRE 5 ms-99.9 ms				H	H
	Area	U3/3	U28/4	U3/4	U11/10	U11/9

Period Control

1. Set the HP 8112A to RCL 0
2. Check the Period DAC output according to the following table:

Table 10.5-3. Typical Period Control DAC Output

HP 8112A PER	Voltage at TP1
1 ms	+9.8 V
5 ms	+1.95 V
9.99 ms	+0.98 V

Delay Control

1. Set the HP 8112A to RCL 0, PER 15 ms
2. Check the Delay DAC output according to the following table:

Table 10.5-4. Typical Delay Control DAC Output

HP 8112A DEL	Voltage at TP3
1 ms	+9.8 V
5 ms	+1.95 V
9.99 ms	+0.98 V

Width Control

1. Set the HP 8112A to RCL 0, PER 15 ms
2. Check the Width DAC output according to the following table:

Table 10.5-5. Typical Width Control DAC Output

HP 8112A WID	Voltage at TP2
1 ms	+9.8 V
5 ms	+1.95 V
9.99 ms	+0.98 V

Slope Control

1. Set up the HP 8112A as follows:

RCL	0
DTY	50%
PER	10 ms
TRE	500μs

2. Check the Slope DAC leading edge output according to the following table:

Table 10.5-6. Typical Slope (LEE) Control DAC Output

HP 8112A LEE	Voltage at TP4
50 μs	+1.65 V
500 μs	+0.16 V
999 μs	+0.08 V

3. Set the HP 8112A LEE to 500μs
4. Check the Slope DAC trailing edge output according to the following table:

Table 10.5-7. Typical Slope (TRE) Control DAC Output

HP 8112A TRE	Voltage at TP5
50 μs	+1.65 V
500 μs	+0.16 V
999 μs	+0.08 V

Amplitude Control

1. Set up the HP 8112A as follows:

RCL	0
LOL	−8.0 V
Output	Enabled

2. Check that U18 operates according to the following table:

Table 10.5-8. Amplitude Gain Control truth table

HP 8112A Setting	U18 Pin		Amplitude Range
	15 GR 0	16 GR 1	
HIL +8.0 V to HIL +2.0 V	: L :	L	1
HIL +1.99 V to HIL −7.9 V	: H :	L	2 3
HILC Mode	L	H	
Area	U25/10	U25/9	

Offset Control

1. Set the HP 8112A as follows:

   RCL 0
   Output Enabled

2. Check the offset DAC's output-voltage against the following table. If necessary you can also check that the DAC is receiving the correct data from the offset latches.

Table 10.5-9. Offset DAC - Output Voltages

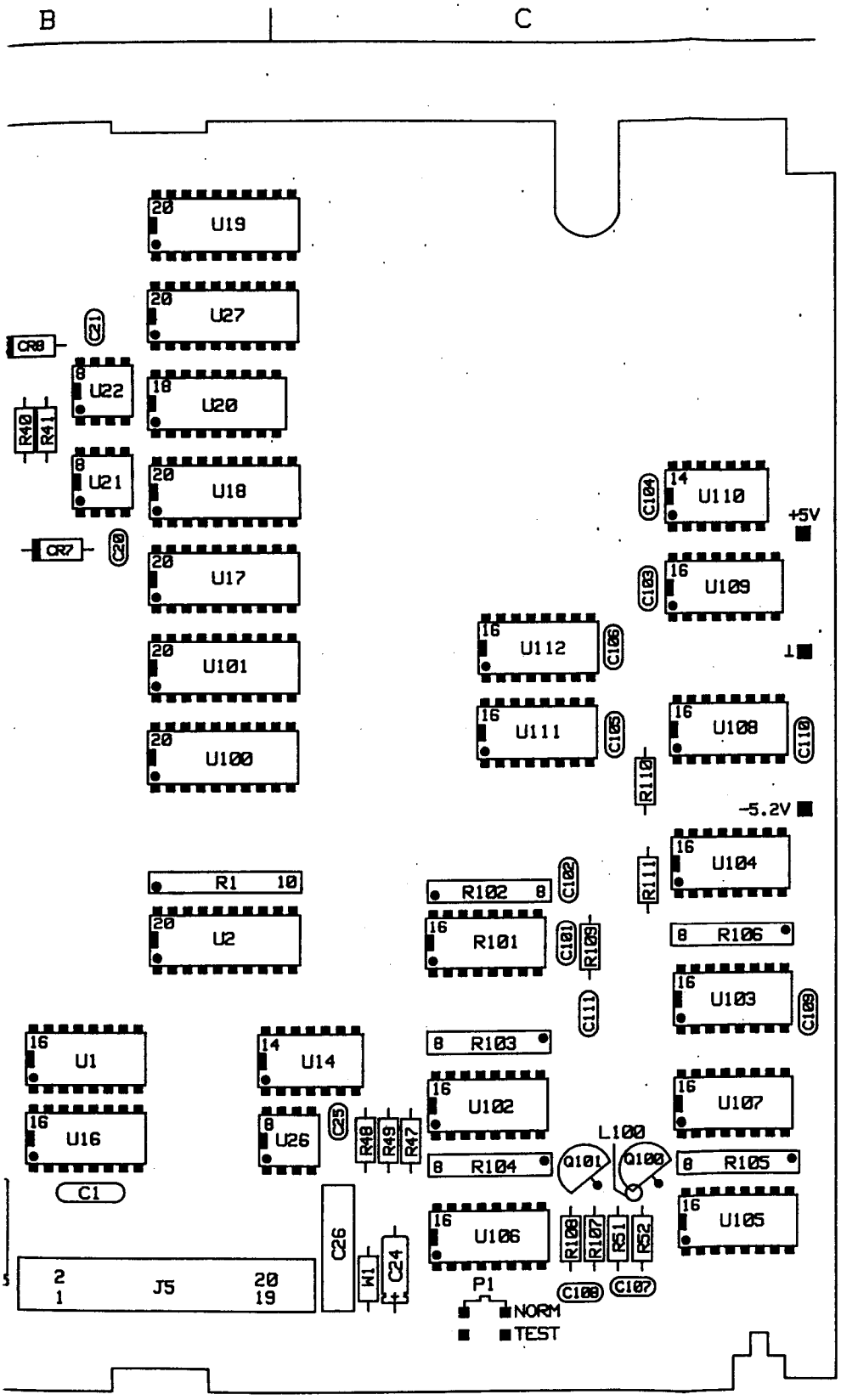
HP 8112 Setting		Voltage at TP6
HIL	LOL	
+8.00 V	+7.90 V	−7.45 V
+5.62 V	+4.62 V	−4.80 V
+1.05 V	+0.95 V	−0.94 V
+0.55 V	+0.45 V	−0.47 V
+0.15 V	+0.05 V	−0.09 V
+0.10 V	0.00 V	−0.05 V
+0.05 V	−0.05 V	< 10 mV
0.00 V	−0.10 V	+0.05 V
−0.05 V	−0.15 V	+0.09 V
−0.45 V	−0.55 V	+0.47 V
−0.95 V	−1.05 V	+0.95 V
−4.62 V	−5.62 V	+4.80 V
−7.90 V	−8.00 V	+7.45 V

Timer

1. Set the HP 8112A as follows:

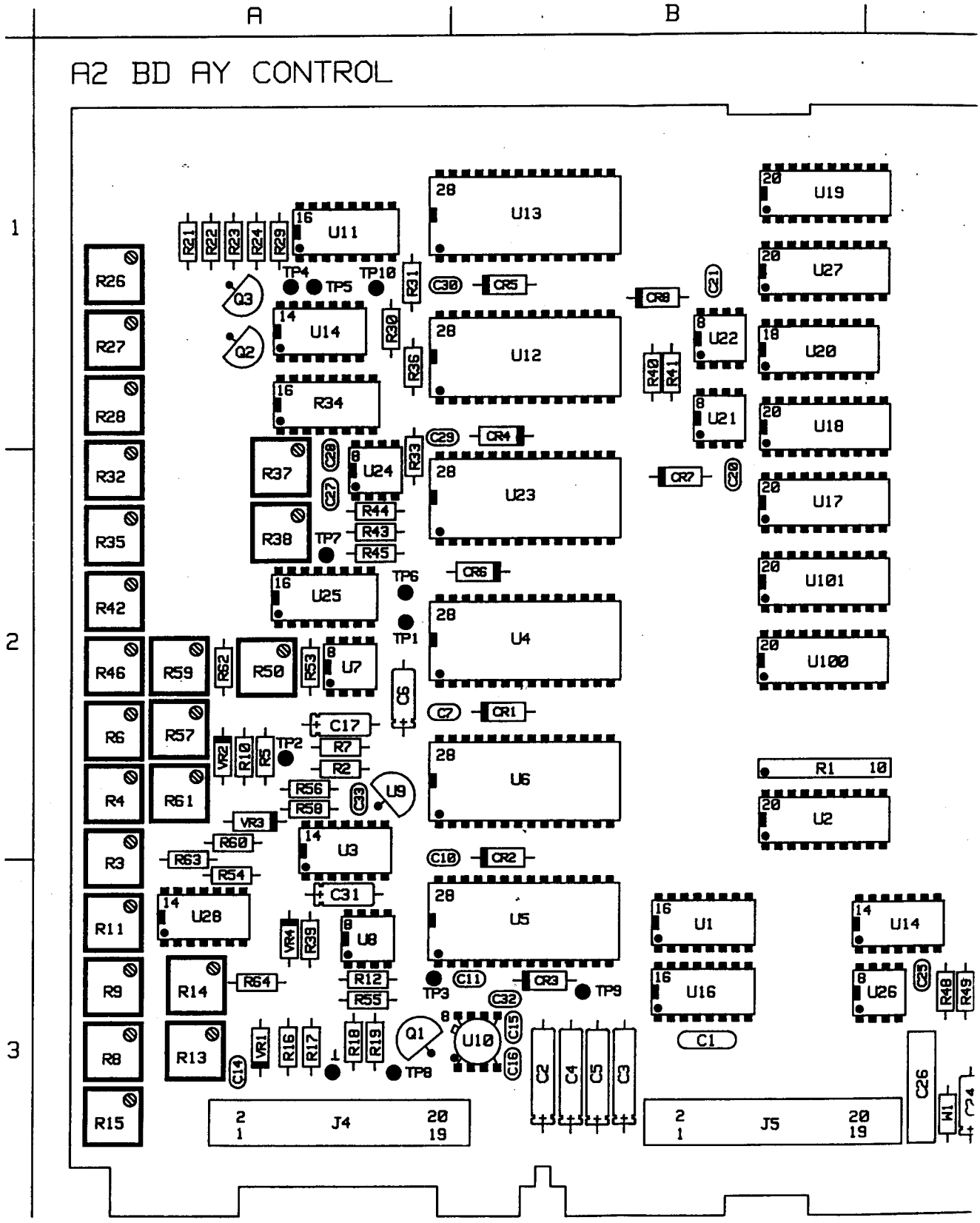
RCL	0
PER	10 μs
Output	Enabled

2. Check the $\overline{\text{TIRE}}$ signal on U26 pin 4 is HIGH.
3. Check U26 pin 3 for a 100 Hz signal.



REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
C1	B3	R8	A3	TP1	A2
C2	B3	R9	A3	TP2	A2
C3	B3	R10	A2	TP3	A3
C4	B3	R11	A3	TP4	A1
C5	B3	R12	A3	TP5	A1
C6	A2	R13	A3	TP6	A2
C7	A2	R14	A3	TP7	A2
C10	A2	R15	A3	TP8	A3
C11	B3	R16	A3	TP9	B3
C14	A3	R17	A3	TP10	A1
C15	B3	R18	A3	U1	B3
C16	B3	R19	A3	U2	B2
C17	A2	R21	A1	U3	A2
C20	B2	R22	A1	U4	B2
C21	B1	R23	A1	U5	B3
C24	C3	R24	A1	U6	B2
C25	C3	R26	A1	U7	A2
C26	C3	R27	A1	U8	A3
C27	A2	R28	A1	U9	A2
C28	A2	R29	A1	U10	B3
C29	A1	R30	A1	U11	A1
C30	A1	R31	A1	U12	B1
C31	A3	R32	A2	U13	B1
C32	B3	R33	A2	U14	A1
C33	A2	R34	A1	U15	C3
C101	C2	R35	A2	U16	B3
C102	C2	R36	A1	U17	B2
C103	C2	R37	A2	U18	B1
C104	C1	R38	A2	U19	B1
C105	C2	R39	A3	U20	B1
C106	C2	R40	B1	U21	B1
C107	C3	R41	B1	U22	B1
C108	C3	R42	A2	U23	B2
C109	C3	R43	A2	U24	A2
C110	C2	R44	A2	U25	A2
C111	C3	R45	A2	U26	C3
CR1	B2	R46	A2	U27	B1
CR2	B2	R47	C3	U28	A3
CR3	B3	R48	C3	U100	B2
CR4	B1	R49	C3	U101	B2
CR5	B1	R50	A2	U102	C3
CR6	B2	R51	C3	U103	C3
CR7	B2	R52	C3	U104	C2
CR8	B1	R53	A2	U105	C3
J4	A3	R54	A3	U106	C3
J5	B3	R55	A3	U107	C3
K1	A2	R56	A2	U108	C2
K2	A2	R57	A2	U109	C2
K3	A2	R58	A2	U110	C1
K4	A2	R59	A2	U111	C2
L100	C3	R60	A2	U112	C2
P1	C3	R61	A2	VR1	A3
Q1	A3	R62	A2	VR2	A2
Q2	A1	R63	A2/3	VR3	A2
Q3	A1	R64	A3	W1	C3
Q100	C3	R101	C2		
Q101	C3	R102	C2		
R1	B1	R103	C3		
R2	A2	R104	C3		
R3	A2/3	R105	C3		
R4	A2	R106	C2		
R5	A2	R107	C3		
R6	A2	R108	C3		
R7	A2	R109	C2		
		R110	C2		
		R111	C2		

FIGURE 10.5-6. CONTROL BD A2 COMPONENT LAYOUT AND LOCATOR


A
B
1
2
3
A2 BD AY CONTROL
U11
U13
U19
U27
U14
U12
U22
U20
U21
U18
U24
U23
U17
U25
U101
U4
U100
U7
U6
U2
U3
U28
U5
U1
U14
U16
U8
U26
U10
J4
J5
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
Q1
Q2
Q3
U9
C1
C2
C3
C4
C5
C6
C7
C10
C11
C14
C15
C16
C17
C26
C29
C30
C31
C32
C33
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R21
R22
R23
R24
R26
R27
R28
R29
R30
R31
R32
R34
R35
R36
R37
R38
R40
R41
R42
R43
R44
R45
R46
R48
R49
R50
R53
R54
R55
R56
R57
R58
R59
R60
R61
R62
R63
R64
VR1
VR2
VR3
VR4

10.6

Servicing the Burst Control Circuit

Theory of Operation

Introduction

This chapter covers the burst control circuit on the A2 control-board that controls the output of the period generator on board A1 (See Chapter 10-3), when burst mode is selected.

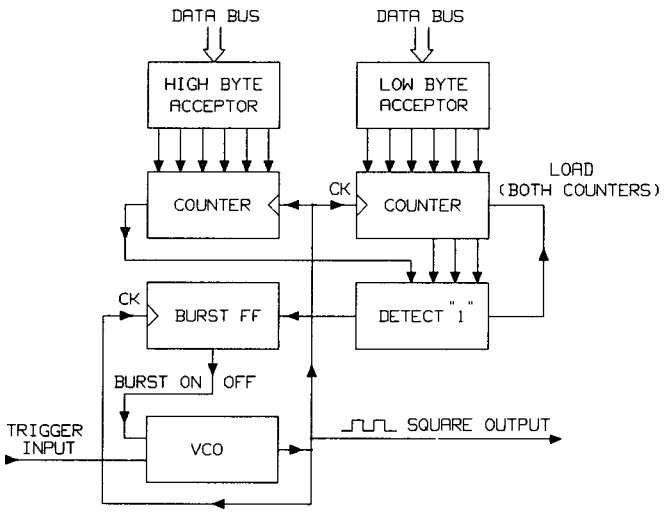


Figure 10.6-1. Simplified Burst Generator

Figure 10.6-1 shows a simplified view of the burst-generator circuits. The burst flip-flop is located on the main board, not on the control board. Refer to Figure 10.6-2.

Operation of the burst control circuit can be categorised as follows:

- Burst number acceptors
- Counter
- Blocking flip-flop

Burst Number Acceptors

The burst number input from the front panel or system controller, is loaded into latches U100 and U101 on receipt of $\overline{\text{LBB}}$ (low byte burst) and $\overline{\text{HBB}}$ (high byte burst), from the control-board address decoder. The $\overline{\text{LBC}}$ signal loads the preset burst number into the counter circuits and resets the blocking flip-flop U109 which allows the counter to start counting down.

Counter

Burst is triggered by external trigger or operation of the (MAN) key. The counter is then clocked by output pulses from the period generator on the main board A1.

The 11-bit counter consists of two 4-bit counter ICs (U111 and U112) and three flip-flops U105 and U106A which handle the three least-significant bits. The whole counter counts down when clocked by the burst-clock signal from the main board. The burst-clock signal is enabled by the burst-on signal which is withdrawn when the counter reaches "1" (See "Blocking Flip-flop").

Blocking Flip-flop

The blocking flip-flop U109A performs two functions:

- Period Generator control
- Counter resetting

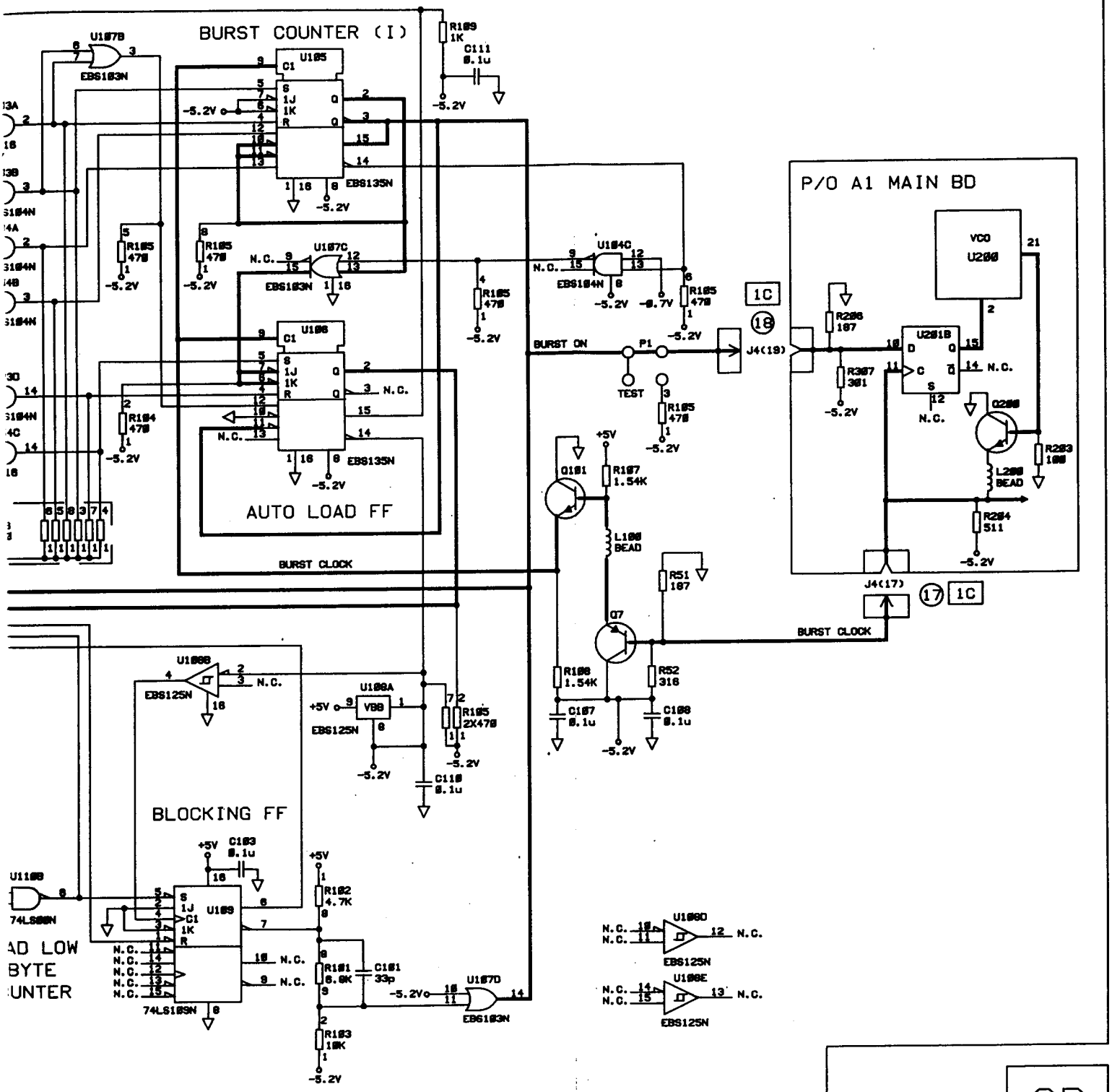
Period Generator Control

When counters U111 and U112 have both cleared, the TC output from them (pin 12), gated by U110, sets the flip-flop U109A. The Q output disables counter U111 and the $\overline{Q}$ output enables the wired-or "Burst On" circuit via U107B. In this configuration the BURST ON signal is active (low), only when all the the counter inputs are low signifying the burst is complete.

Counter reset

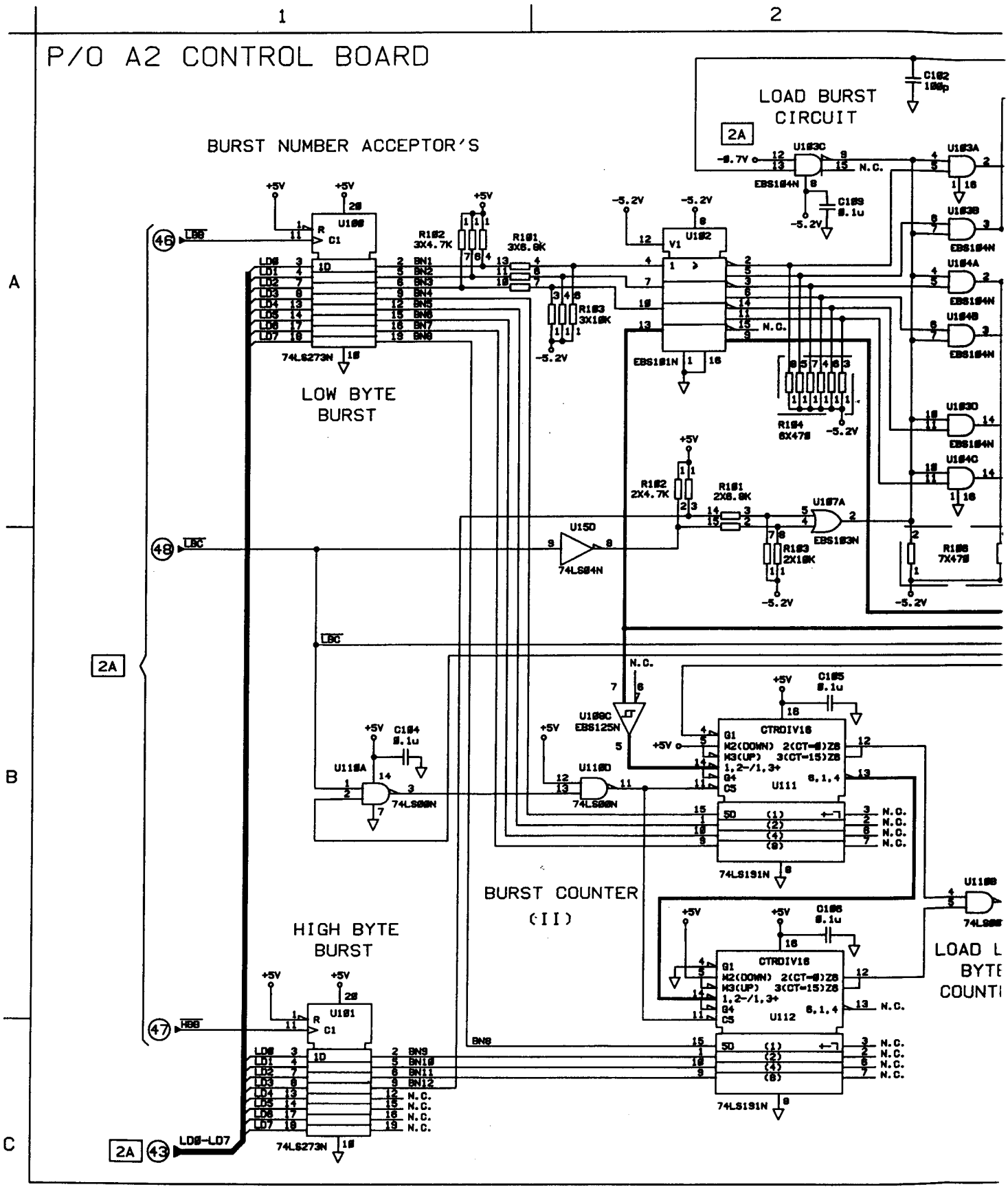
For the counter to be re-enabled, the logic signal $\overline{LBC}$ from the address decoder U16 must be set true (low). This resets the blocking flip-flop, re-loads the burst counter and sets the counter enable input ($\overline{CE}$) low. The burst circuitry is then in a stand-by state awaiting the next period generator pulse train.

Once started, count-down continues until the counter flip-flops (U105 and U106A) reach 1 and the burst-on signal is withdrawn, stopping the burst-clock signal.



2D

MODEL HP8112A
FIGURE 10.6-2.
BURST CONTROL BD A2 SCHEMATIC 1


P/O A2 CONTROL BOARD
1
2
A
B
C
BURST NUMBER ACCEPTOR'S
LOAD BURST CIRCUIT
LOW BYTE BURST
HIGH BYTE BURST
BURST COUNTER (II)
LOAD L BYTE COUNTI
74LS273N
74LS04N
74LS08N
74LS191N
EBS125N
EBS193N
EBS184N
CTRDIV16
LBB
LBC
HBB
LD0-LD7
BN0
2A
+5V
-5.2V
-8.7V
N.C.

Troubleshooting

Note

- If an error code is being displayed by the HP 8112A you must press a key, [LCL] for example, to return the microprocessor to normal operation before troubleshooting.
- The component layout and locator for the burst control part of board A2 is the same as Figure 10.5-6.

Output Address Decoder

Address decoder U16 provides control signals for the burst control circuits. These can be checked using signature analysis:

1. Set the microprocessor to free run mode as follows:
   a. Set the P1 wire on board A3 (See Chapter 10.7) to position **P1**.
   b. Disconnect Jumper A2W1.
   c. Connect RES on A3 to ground for a short time to ensure the microprocessor is reset.
   d. Connect the signature analyser ground to the Control Board ground and connect the probes as follows:

Sig. Analyser	**A3 μP Board Connections**
Start ƒ	TP "SA"
Stop ƒ	TP "SP"
Clock ↘	TP "E"

   e. Verify that the reading at the Microprocessor +5 V is 0003. If it is not, then the microprocessor is not free running.
   f. Check the signatures of U16 against those given in Table 10.6-1

Table 10.6-1. Output Address Decoder Signatures

U16 pin	Mnemonic	Description	Free run Signature
1	LA3	Sub decoded address	P50H
2	LA4	Sub decoded address	CH9U
3	LA5	Sub decoded address	8759
4 & 5	$\overline{\text{WS5}}$	Sub decoded address	8U95
9	$\overline{\text{LBC}}$	Load Burst Counter	0F4F
10	$\overline{\text{HBB}}$	High Byte Burst	71P0
11	$\overline{\text{LBB}}$	Low Byte Burst	58F8

Burst Counter

Test the burst counter circuits using the following procedure:

1. Set up the HP 8112A up as follows:

PER	1 μs
Mode	E.BURST
DTY	50%
BUR	1024

2. Switch off the HP 8112A
3. Desolder wire W3 on the control board A2 and resolder it to the "test" position. This pulls BURST ON low via R105.
4. Connect A1 U201 pin 10 to ground.
5. Switch on the HP 8112A and check that error number E52 is displayed.
6. Press (LCL)
7. Press the (MAN) button
8. Check the TTL logic levels at the burst acceptors U100 and U101 as follows:

Table 10.6-2.

Signal	Pin	Level
BN1	U100 Pin 2	L
BN2	U100 Pin 5	L
BN3	U100 Pin 6	L
BN4	U100 Pin 9	L
BN5	U100 Pin 12	L
BN6	U100 Pin 15	L
BN7	U100 Pin 16	L
BN8	U100 Pin 19	L
BN9	U101 Pin 2	L
BN10	U101 Pin 5	L
BN11	U101 Pin 6	H

9. Using an oscilloscope and ECL- and TTL-logic probes you can test the burst- counter waveform and timing data against Figure 10.6-3.

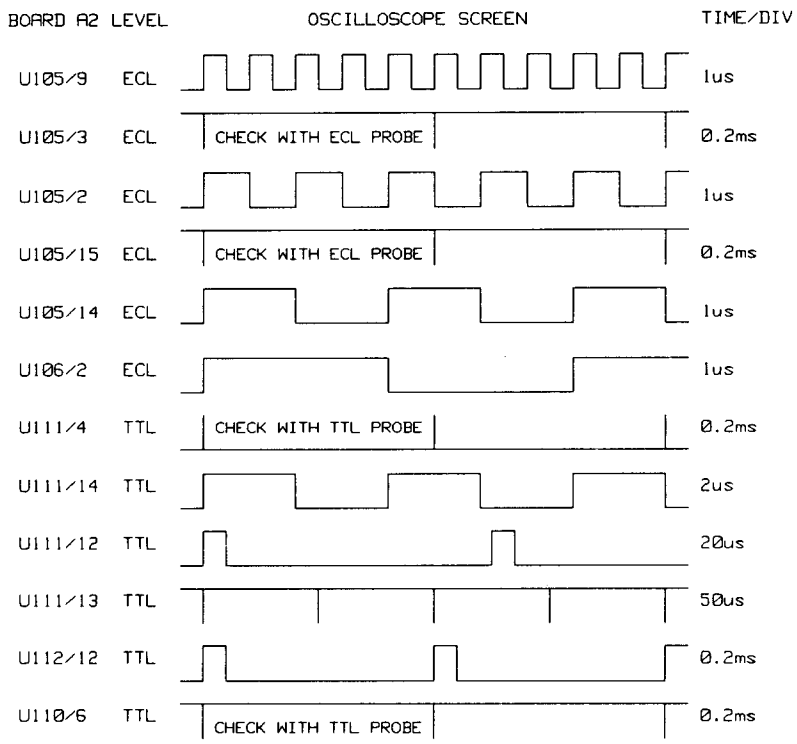


Figure 10.6-3. Burst-counter waveforms and timing

10.7

Servicing the Microprocessor and Front-panel

Theory of Operation

Introduction

The microprocessor board is the control center of the HP 8112A. The microprocessor monitors the keyboard and HP-IB, interprets the key-presses and commands, and implements them by sending control data to the control circuits and updating the front-panel display and LEDs.

When in remote control mode all the front panel keys, except [LCL], are ignored by the microprocessor. If the local lockout command has been received on the HP-IB then the [LCL] key is also ignored.

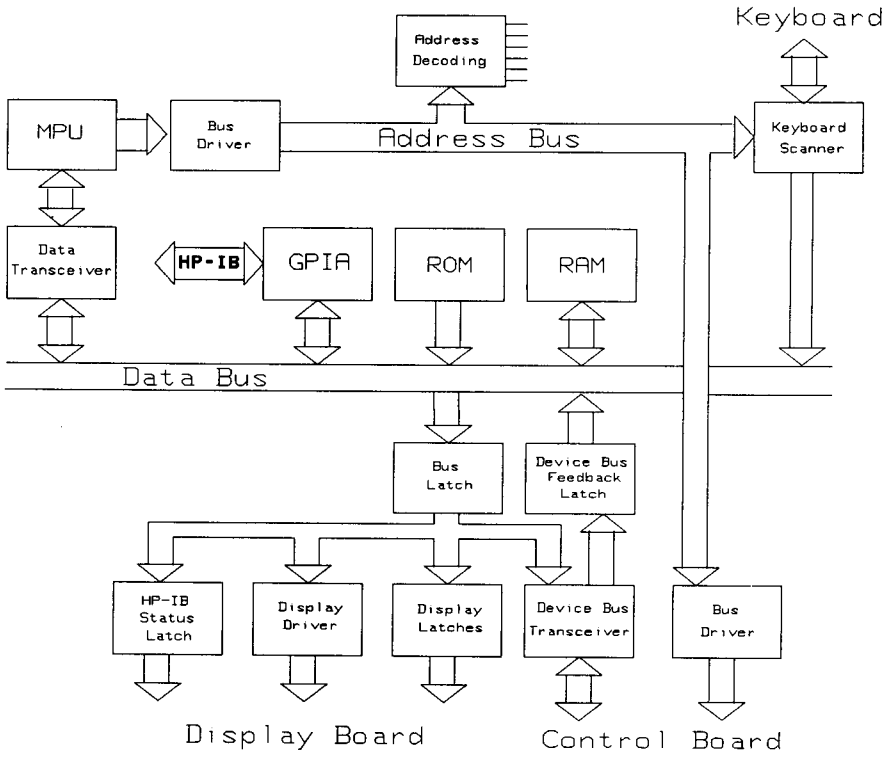


Figure 10.7-1. Microprocessor board architecture

Figure 10.7-1 summarises the parts of the microprocessor board and the connecting busses. The purpose of the address bus is to allow the microprocessor to select a particular location in the instrument. The location can be in ROM, in RAM, in the GPIA, or one of the other devices. The data bus allows the microprocessor to read data from,

or write data to, the addressed location. Note that some devices can only be read from, others can only be written to, and others can both be read from and written to.

Read Only Memory (ROM)

The ROM is a permanent data-store which contains the microprocessor program and other fixed data such as the standard parameter set.

Random Access Memory (RAM)

The RAM is a data-store which the microprocessor can write to and read from using the read/write (R/$\overline{W}$) control line to choose which operation is required.

The RAM is used to store the current parameter set and temporary data needed by the microprocessor. The HP 8112A RAM has a battery back-up power supply, described in the following section, which means the data in the RAM is maintained while the instrument is switched off. This allows the current parameter set to be restored when the instrument is switched on again.

The normally negative "Power Down Detected" signal is used to ensure that the RAM data is not corrupted when the instrument is switched off.(Refer to Figure 10.7-5). Normally U27A output is low, U27B output is therefore positive and the RAM SELECT output from U15C can enable the RAM by switching on U29C. When the "Power Down Detect" signal goes high, U27A output goes low, U27B output goes low and U15C cannot switch on U29C. Therefore the RAM becomes, or remains, disabled.

RAM Battery Supply

When the instrument is operating, U27C output is high, Q1 is switched on and the RAM U10 is powered from the +5 V supply. (Refer to Figure 10.7-5). "Power Down Detected" signal goes high, U27C output goes low and switches off Q1. The +5V supply to the RAM is now maintained by the battery BT1.

HP-IB General Purpose Interface Adapter

The GPIA IC U30 interfaces between the microprocessor and the HP-IB, as shown in Figure 10.7-4. The IC pin configuration is given in Figure 10.7-2.

Microprocessor Interface Signals

D0-D7. Eight bi-directional, tri-state data lines allowing data transfer between the microprocessor and the GPIA.

$\overline{CS}$. A negative edge selects the GPIA enabling the microprocessor to communicate with the GPIA.

R/$\overline{W}$. The READ/$\overline{WRITE}$ input controls GPIA register access and the direction of data transfer on the data pins. It is connected to the microprocessor READ/$\overline{WRITE}$ output.

RS0–RS2. The register select lines are connected to the three lowest address lines A0–A2 and allow the microprocessor to choose a GPIA register to read from or write to.

$\overline{\text{IRQ}}$. The interrupt request output allows the GPIA to interrupt the microprocessor.

$\overline{\text{RESET}}$. This input is used to initialize the GPIA. The signal is the same $\overline{\text{RESET}}$ signal generated to reset the microprocessor.

E. The enable input activates the address inputs, R/$\overline{\text{W}}$ input and enables data transfer with the data bus. It is also used internally as a state counter, allowing the GPIA to change interface states. E is connected to the micropocessor clock output.

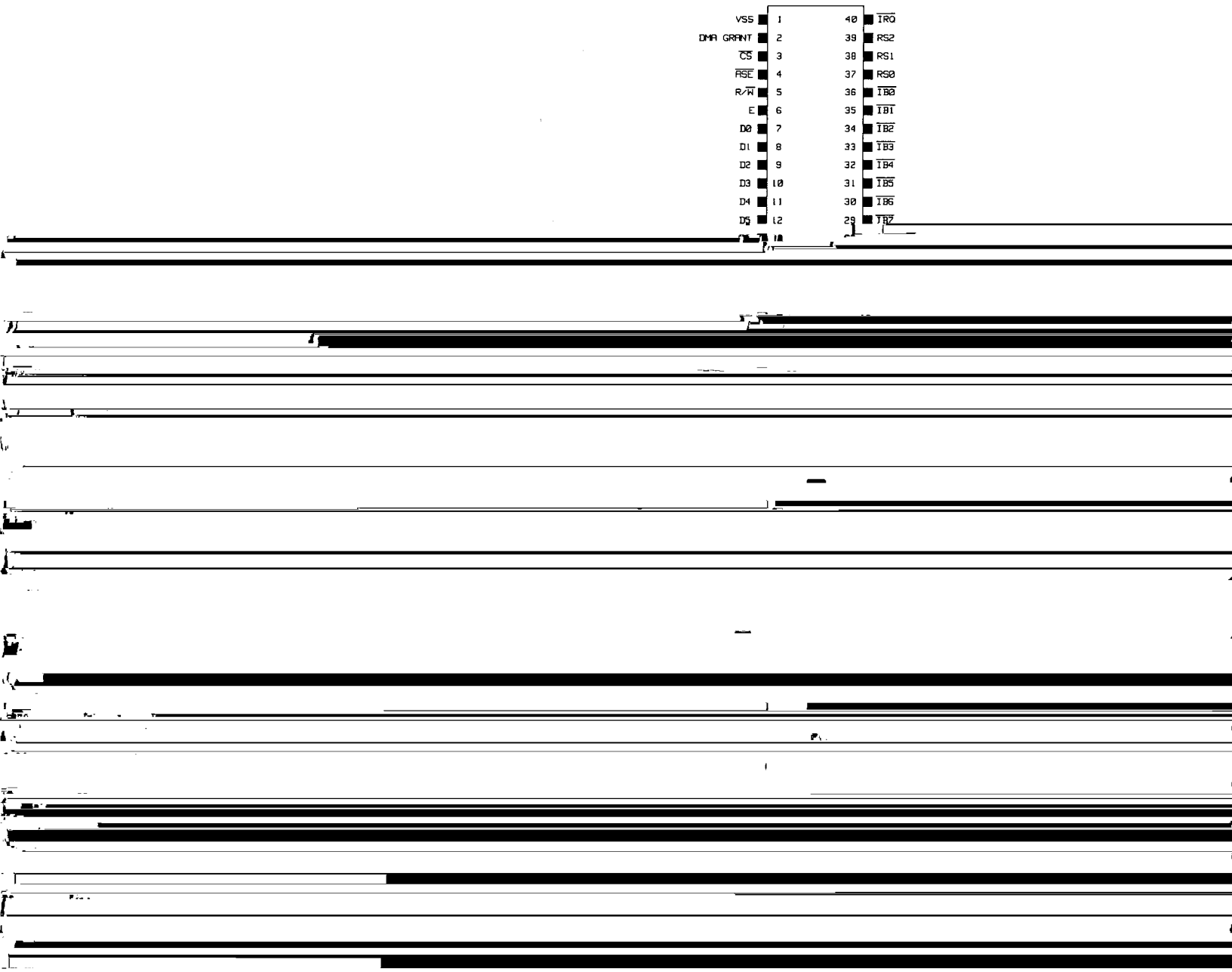


Figure 10.7-2. GPIA IC pins

HP-IB Interface Signals

IB0–IB7. Eight HP-IB data lines.

Address Decoding

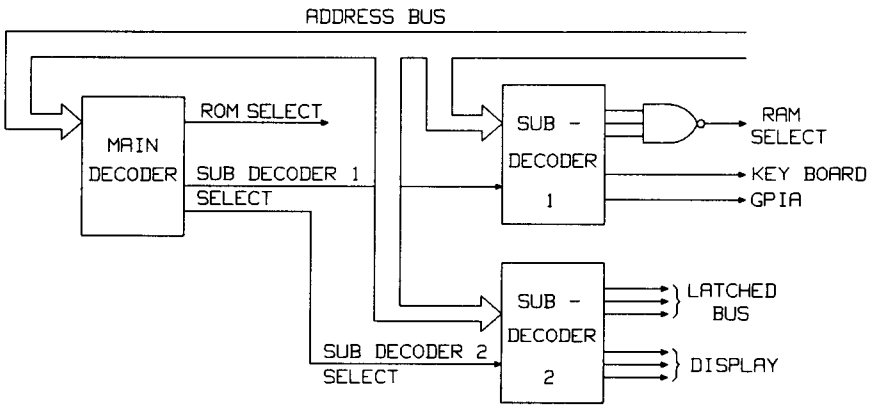


Figure 10.7-3. Address decoding

Address decoding is performed at two levels, as shown in Figure 10.7-3. The main decoder U12 uses microprocessor addresss lines A12, A13 and A15 to enable one of the following:

- ROM U40
- Sub-decoder 1 U13
- Sub-decoder 2 U14

Sub-decoder 1

If sub-decoder 1 U13 is enabled by the main decoder, it uses microprocessor address lines A8, A9 and A10 to enable one of the following:

- RAM U10
- Keyboard Scanner U19
- GPIA U30

Sub-decoder 2

If sub-decoder 2 U14 is enabled by the main decoder, it uses microprocessor address lines A0, A1 and A2 to enable one of the following:

- Latched Data Bus Latch U16
- Control Board Addressing via U18,U21,U17 (Refer to "Control Board Address Decoding")
- Device Bus Feedback Latch U26
- Display Latche U23
- HP-IB Status Latch U37

Control Board Address Decoding

Address decoding for the control board functions is partially carried out on the microprocessor board. Address lines A3–A9 and A14 are passed through latch U18 under the control of sub-decoder 2 (U14). A14 then becomes the $\overline{\text{MODE}}$ control for the display driver (refer to "Display Driving"), while A3–A9 pass through bus driver U21. Decoder U17 uses A6 and A7 to produce the "write select" signals $\overline{\text{WS1}}$–$\overline{\text{WS6}}$ and the $\overline{\text{WRITE}}$ signal to the display driver (refer to "Display Driving").

Key Scanning

Refer to Figure 10.7-6 and Figure 10.7-7 The keyboard assembly A4 is a switch panel on which all mode, control, parameter, waveform, output and trigger control pushbuttons are mounted. The microprocessor scans the frontpanel key matrix using a BCD to decimal converter U20 and an 8-to-1 multiplexer U19. A3, A4 and A5 are the inputs to U20 and are continuously incremented from one to six by the microprocessor. The six "decimal" outputs from U20, KD0–KD5, are used as the vertical signal paths to the key matrix.

The horizontal signal paths of the key matrix, KS0–KS7, form the inputs to the multiplexer U19, which is controlled by address lines A0, A1 and A2. The output from U19 therefore represents the state of the key joining the vertical signal path (addressed by A3–A5) and the horizontal signal path (addressed by A0–A2). Each time the microprocessor increments the address to U20 it cycles the address to U19 through all 8 horizontal paths.

Display Driving

Display Driver U22

The display driver operates the key, mode, control and unit LEDs, along with the individual digital display segments, using a matrix technique similar to the keyboard. The outputs DIG0–DIG7 form the vertical signal paths while the outputs a–g and DP form the horizontal paths. The display driver contains 8 bytes of RAM which store 8 data bits (a–g and DP) to be used with each of the 8 "digit" outputs DIG0–DIG7.

The MODE signal determines whether the display driver interprets data as control instructions or display data to be stored in RAM:

Table 10.7-1. Display Driver Control Signals

Signal	Pin	Status	Function
MODE	9	HIGH	Load control instruction on $\overline{\text{WRITE}}$ pulse
		LOW	Load display data on $\overline{\text{WRITE}}$ pulse
$\overline{\text{WRITE}}$	8	HIGH	Data not loaded
		LOW	Data loaded

After the appropriate control instruction, eight bytes of display data are loaded by the microprocessor using eight successive $\overline{\text{WRITE}}$ pulses.

HP-IB Status Latch U37

The data stored in the HP-IB status latch drives the HP-IB status LEDs on the frontpanel.

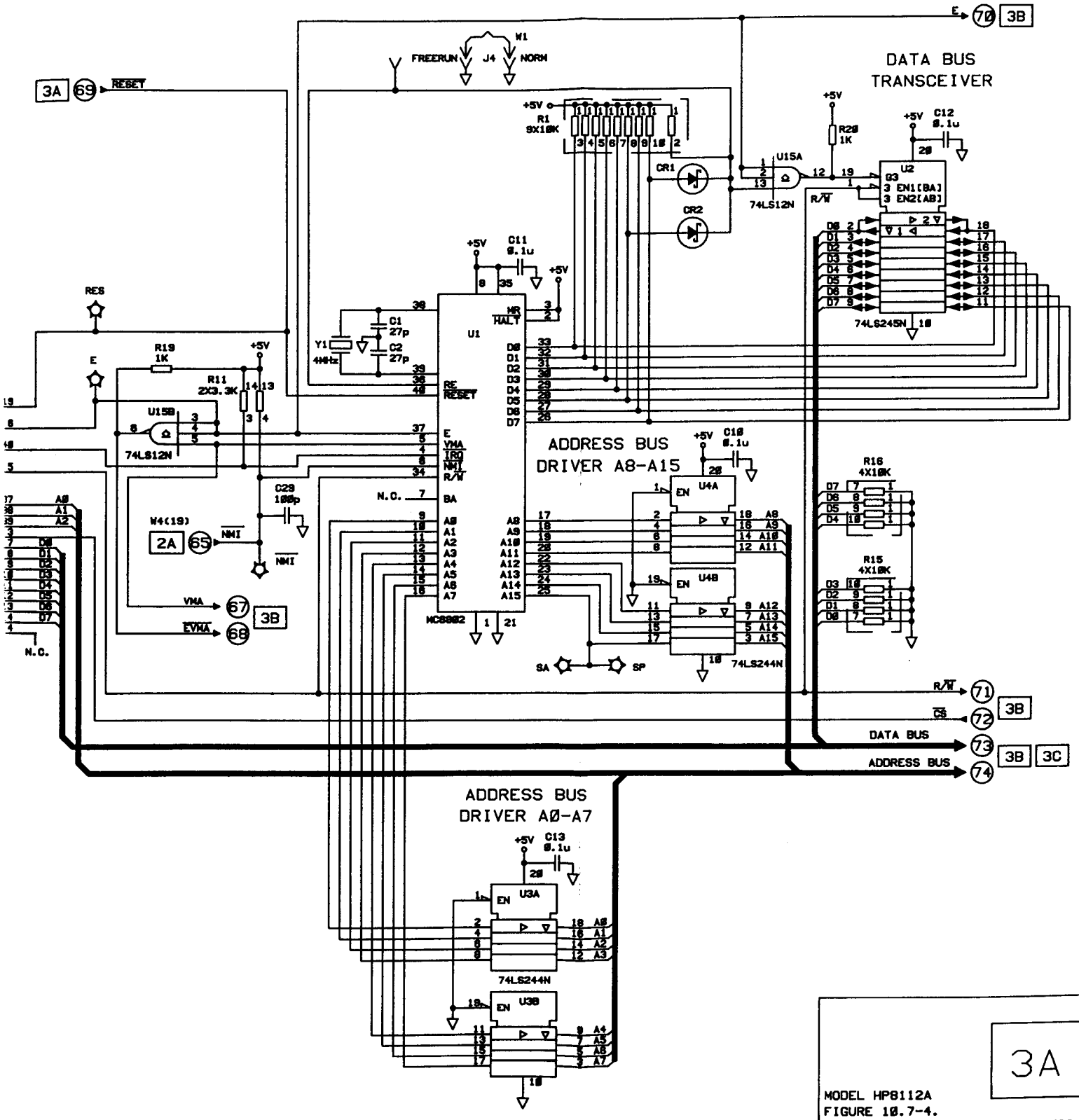
Display Latche U23

The data stored in the display latch drives the parameter LEDs on the frontpanel.

Reset Circuits

When the instrument is switched on, the microprocessor $\overline{\text{RESET}}$ input is held low (reset) for approximately 2.5 ms. This allows the power supplies to become established before the microprocessor starts running. This delay is achieved using the CR network R12 (3 x 10K) and C4 (0.1 μF). U27D output goes high when C4 has charged to approximately 420 mV and the $\overline{\text{RESET}}$ signal is withdrawn.

When the instrument is switched off, the "Power Down Detected" signal goes high forcing the output of U27A high. This switches on transistor U29A which discharges C4 and switches the output of U27D low. The $\overline{\text{RESET}}$ signal to the microprocessor and GPIA is therefore established before their power supply is totally withdrawn.

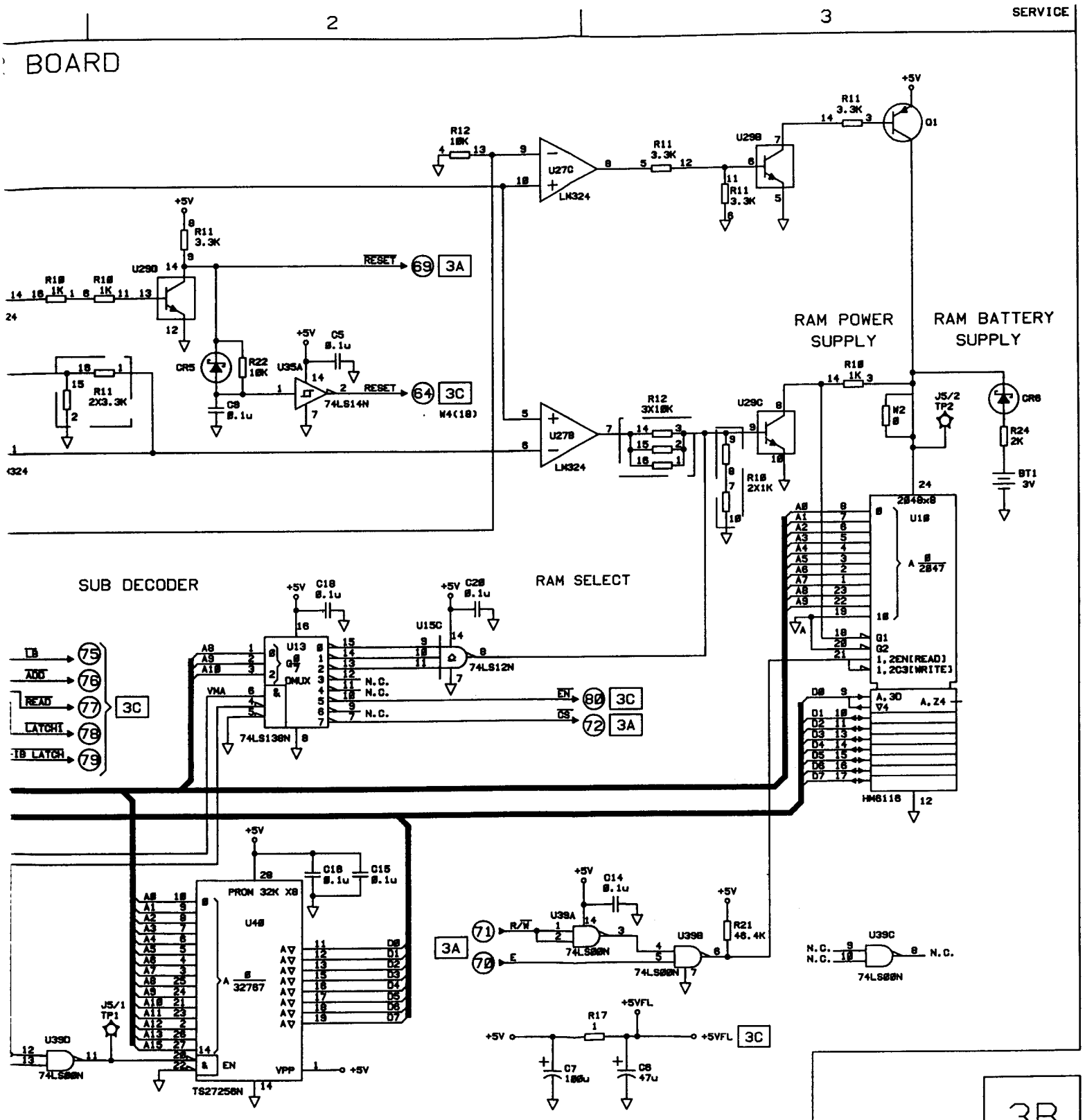


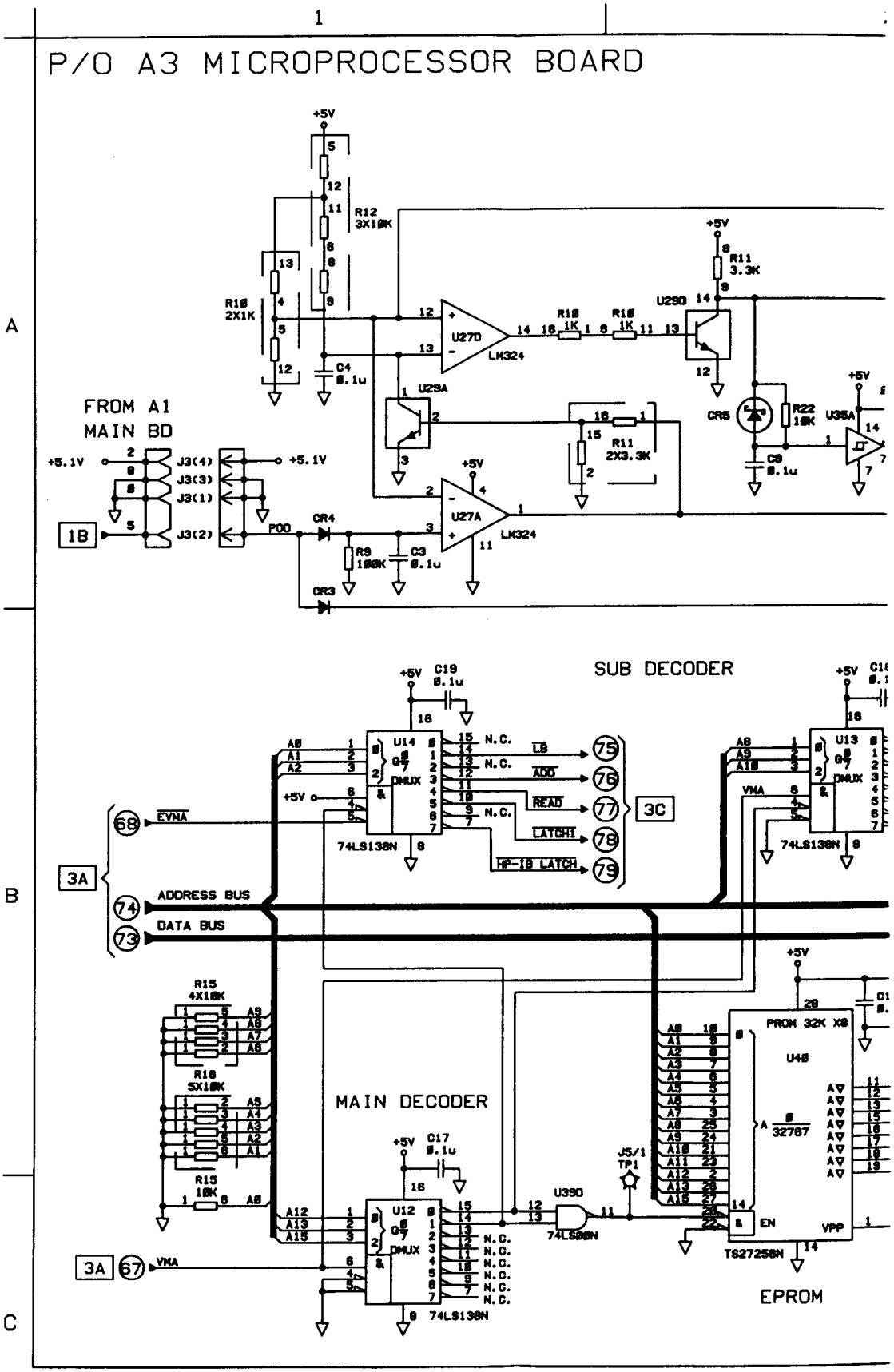
MODEL HP8112A
FIGURE 10.7-4.
MICROPROCESSOR BD A3 SCHEMATIC 1

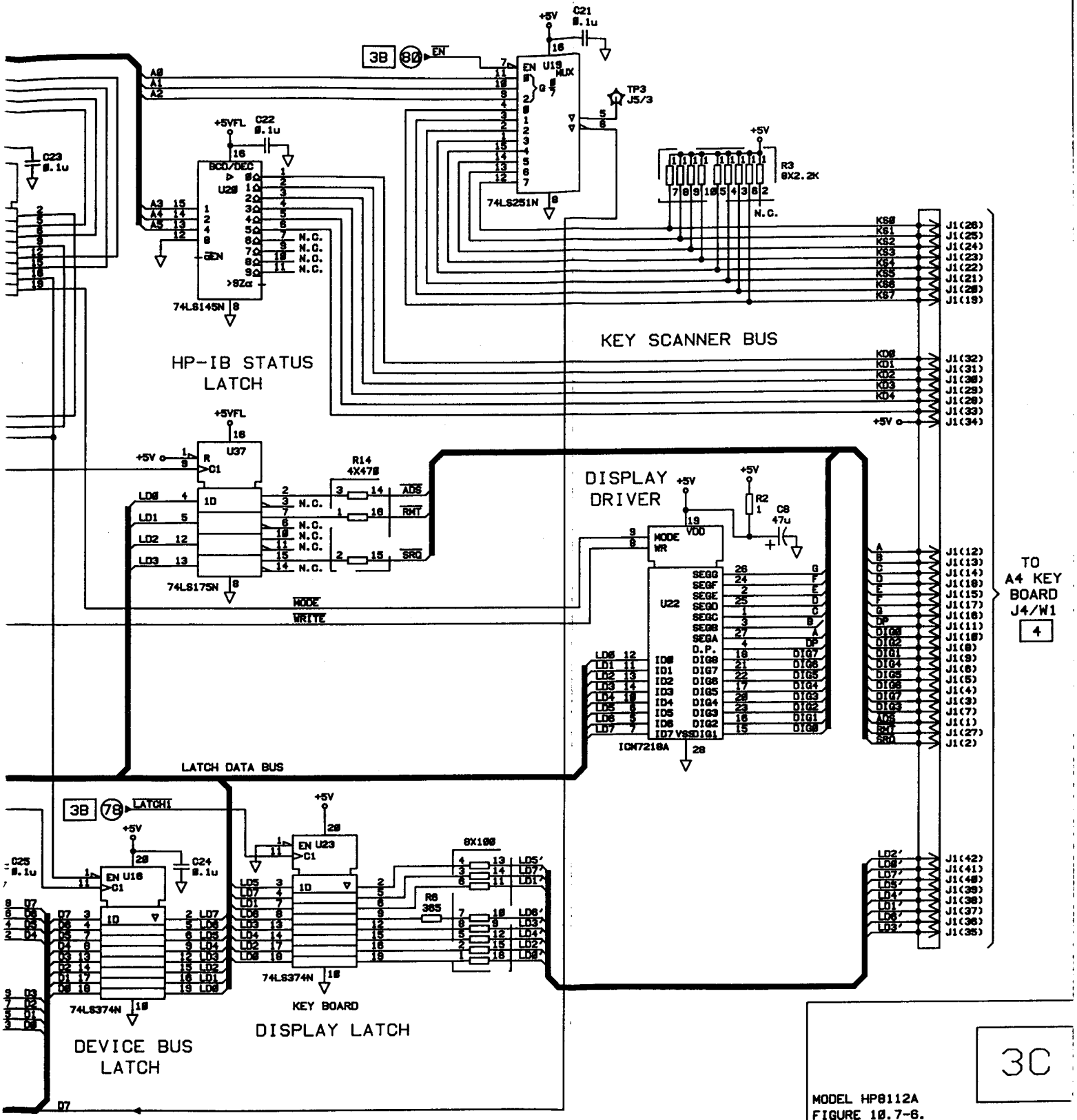
1 2

P/O A3 MICROPROCESSOR BOARD

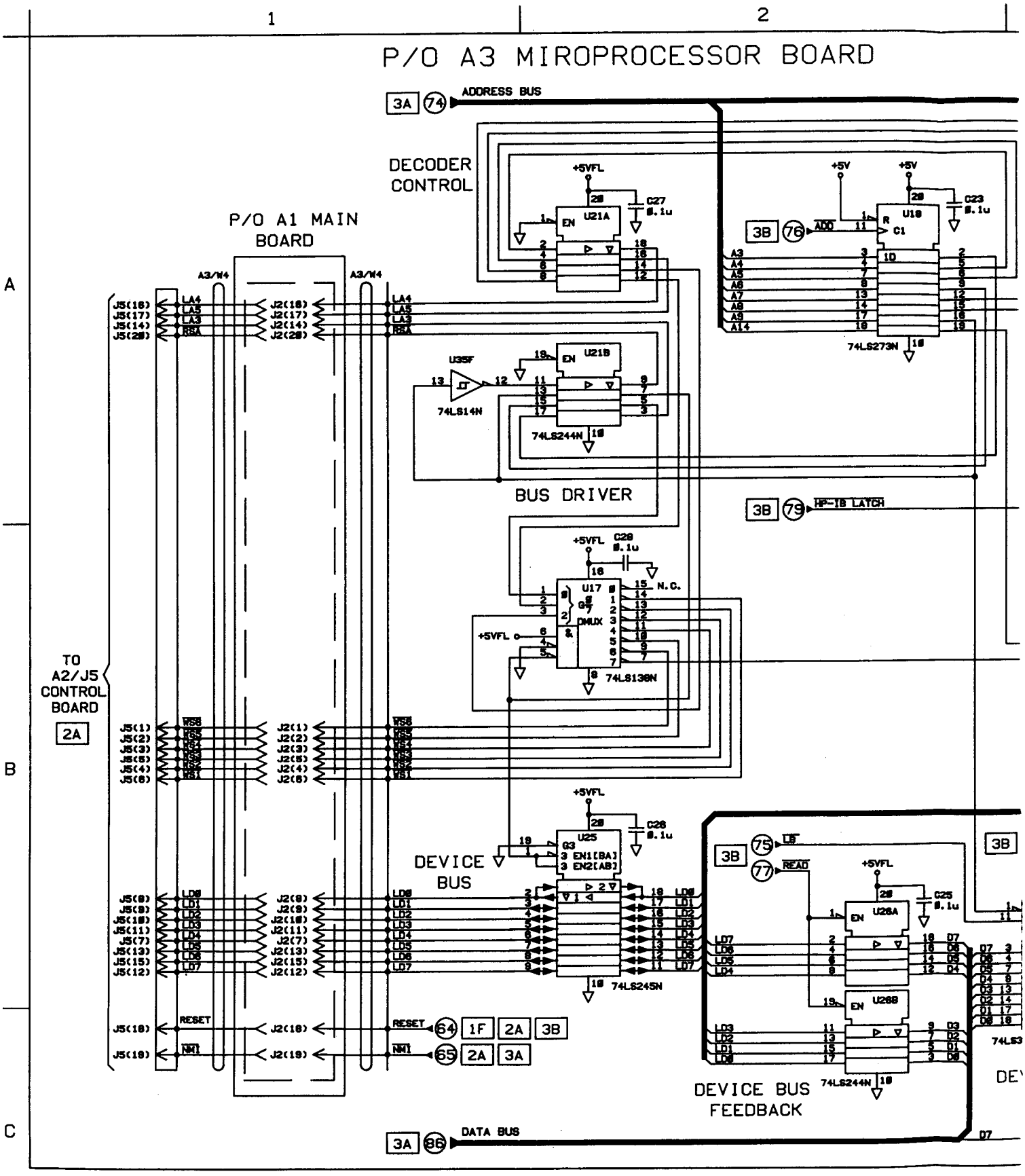
+5V C31


2
3
BOARD
RAM POWER SUPPLY
RAM BATTERY SUPPLY
SUB DECODER
RAM SELECT
EPROM
U27C
LM324
U27B
LM324
U29B
U29C
U29D
U35A
74LS14N
U15C
74LS12N
U13
74LS138N
U18
2048x8
HM6116
U39A
74LS00N
U39B
74LS00N
U39C
74LS00N
U39D
74LS00N
U40
PROM 32K X8
TS27256N
RESET
CS
EN
R/W
E
+5V
+5VFL
BT1
3V
CR5
CR6
Q1
TP1
TP2
3A
3B
3C
MODEL HP8112A
FIGURE 10.7-5.
MICROPROCESSOR BD A3 SCHEMATIC 2

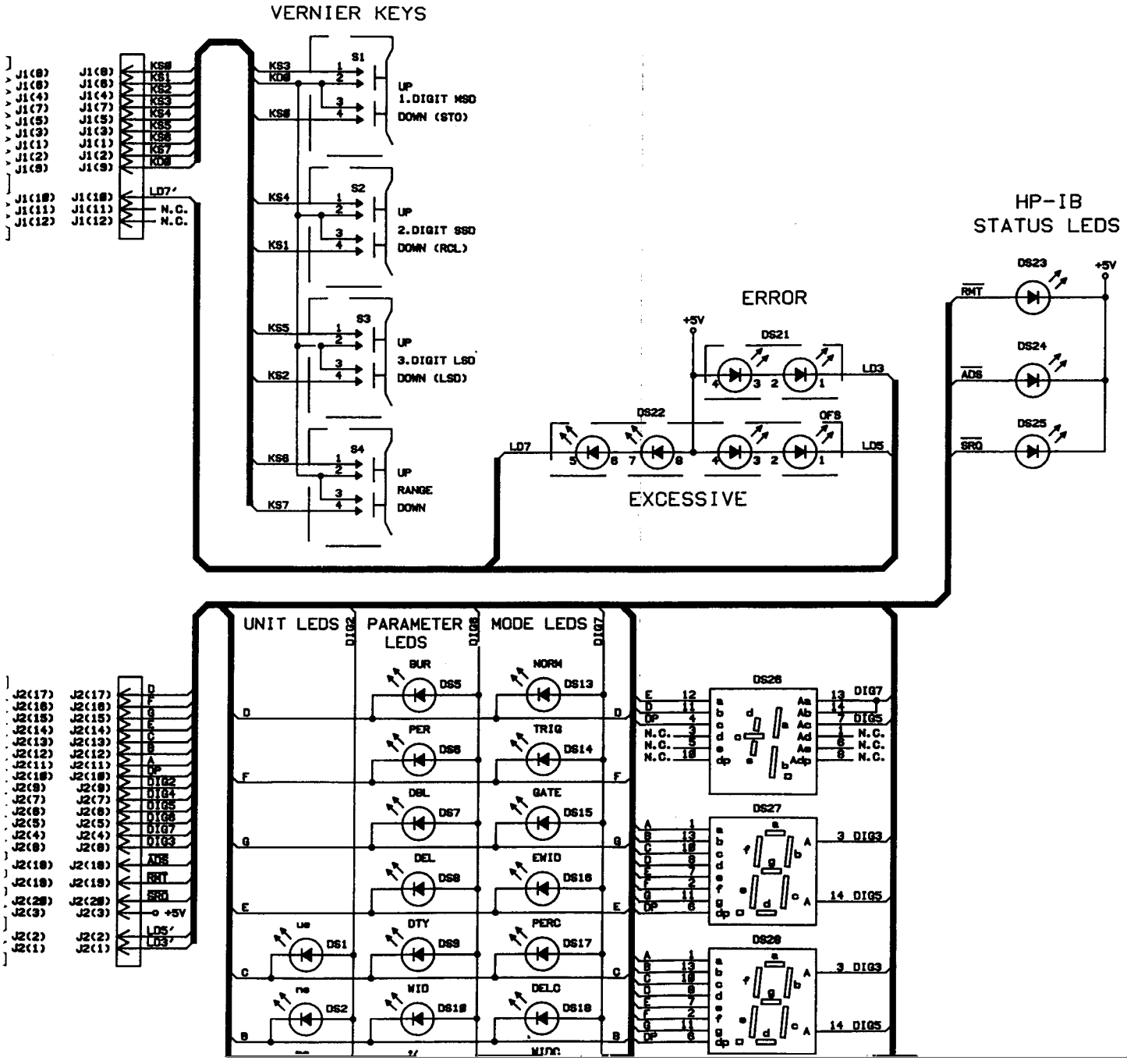

P/O A3 MICROPROCESSOR BOARD
1
A
B
C
FROM A1
MAIN BD
1B
+5.1V
J3(4)
J3(3)
J3(1)
J3(2)
POD
CR4
CR3
R9
100K
C3
0.1u
U27A
LM324
U27D
R12
3X10K
R10
2X1K
C4
0.1u
U29A
U29D
R10
1K
R11
3.3K
R11
2X3.3K
CR5
R22
1K
C9
0.1u
U35A
SUB DECODER
C19
0.1u
U14
74LS138N
N.C.
LB
ADD
READ
LATCH1
HP-IB LATCH
3C
EVMA
3A
ADDRESS BUS
DATA BUS
R15
4X10K
R16
5X10K
R15
10K
MAIN DECODER
C17
0.1u
U12
U39D
74LS00N
J5/1
TP1
U13
VMA
PROM 32K X8
U48
A
32767
EN
VPP
TS27256N
EPROM



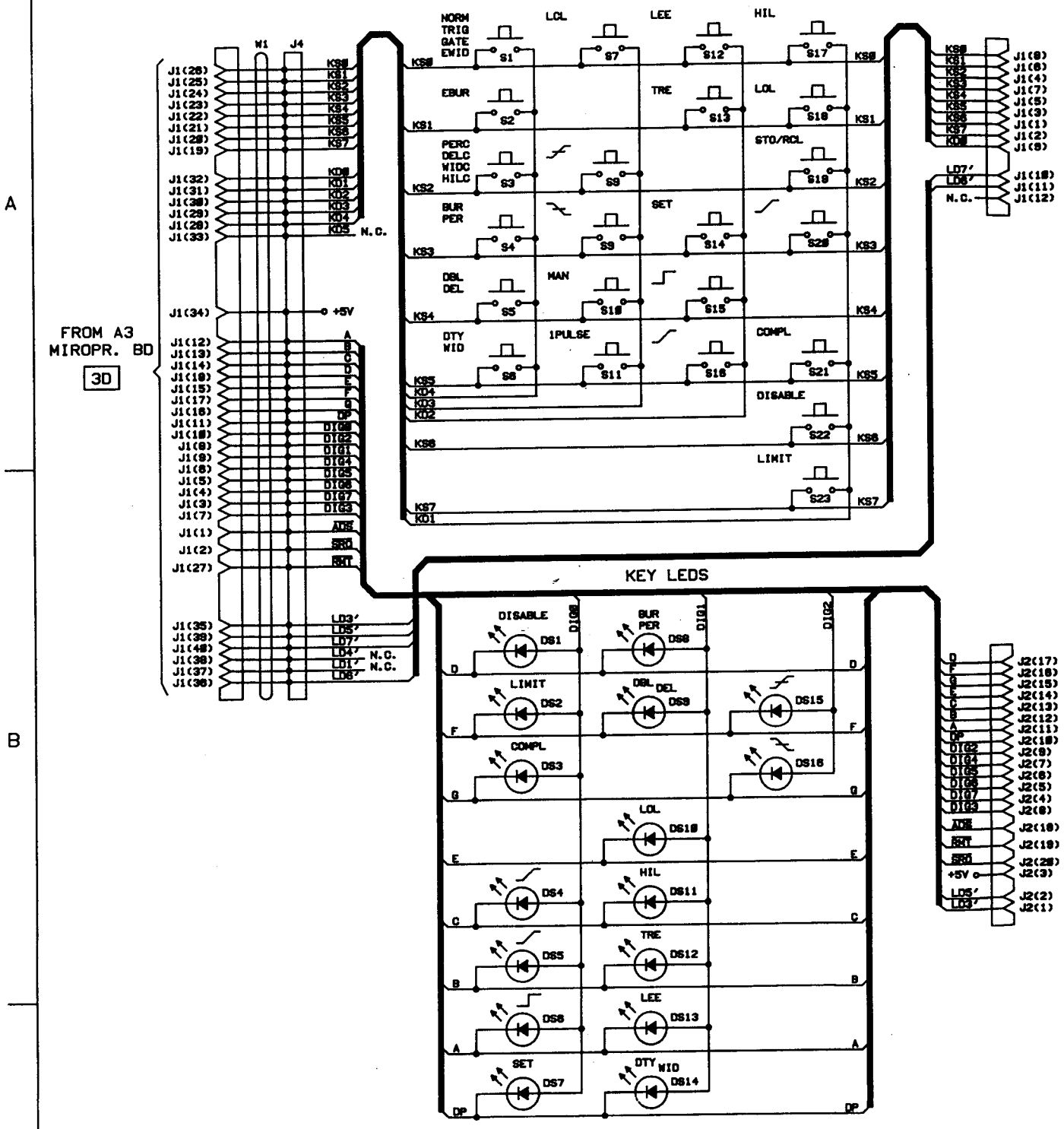
MODEL HP8112A
FIGURE 10.7-6.
MICROPROCESSOR BD A3 SCHEMATIC 3


P/O A3 MIROPROCESSOR BOARD
ADDRESS BUS
DECODER CONTROL
P/O A1 MAIN BOARD
BUS DRIVER
HP-IB LATCH
TO A2/J5 CONTROL BOARD
DEVICE BUS
DEVICE BUS FEEDBACK
DATA BUS
RESET
NMI
READ
74LS273N
74LS244N
74LS14N
74LS138N
74LS245N

A5 DISPLAY BOARD



A4 KEY BOARD


1
2
A
B
C
FROM A3
MIROPR. BD
3D
W1
J4
NORM
TRIG
GATE
EWID
LCL
LEE
HIL
EBUR
TRE
LOL
PERC
DELC
WIDC
HILC
STO/RCL
BUR
PER
SET
DBL
DEL
MAN
DTY
WID
1PULSE
COMPL
DISABLE
LIMIT
N.C.
+5V
KEY LEDS
DIG0
DIG1
DIG2
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
DS11
DS12
DS13
DS14
DS15
DS16

Troubleshooting

Note

- If an error code is being displayed by the HP 8112A you must press a key, [LCL] for example, to return the microprocessor to normal operation before troubleshooting.
- The component layouts and locators for the microprocessor board A3, the keyboard A4 and the display board A5 are at the end of the chapter.

Free Running Signature

To carry out signature analysis the microprocessor must be set to free-running routine in which it increments through all addresses continuously. To set the microprocessor to free-run:

1. Move the jumper on J4 to the free-run position.
2. Disconnect the W4, (the cable to the Control Board) to force NMI high.
3. Reset the microprocessor by shorting TP RES to ground (the pin beside TP RES) for a short time

Note

When you have finished testing, return the jumper on J4 to its normal position and reconnect W4.

Address Bus

The address bus drivers and decoders can be checked using signature analysis.

1. Set the microprocessor to free-run as described in "Free Running Signature Analysis" and connect the signature analyzer probes as given in Table 10.7-2.

Table 10.7-2. Signature Analyzer Probe connections

Probe	Trigger	Connect to

Table 10.7-3. Signatures for Address Drivers and Decoders

Pin	U3	U4	U12	U13	U14	U10	U36	U17	U18	U21
1							667C			
2									P50H	
3	6F9A	0002								P50H
4										
5	U759	9UP1							CH9U	3P76
6									8759	
7	0356	4868	41P4	748C	PHCC			5U3F		9H1H
8						UUUU				
9	1U5P	4FCA	31AC	8069	C6P1			1FH6	3P76	9H1P
10			36F8	U638	HC8A			8U95		
11			4685	9CPH	6P25			55F4	C898	9H1P
12	P763	6U28	20U0	359H	C898			79HU	65A5	65A5
13			18H7	H883	P26P			PU99		
14	8484	37C5	1C66	0A8U	89C7			1P50		FF4H
15			2340	5HP5	26H1				FF4H	
16	FFFF	6321							9H1H	8759
17										
18	UUUU	7791				8UP9			9UP1	CH9U

ROM The ROM can be checked using signature analysis.

1. Set the microprocessor to free-run as described in "Free Running Signature Analysis" and connect the signature analyzer probes as given in Table 10.7-4.

Table 10.7-4.
Signature Analyzer Probe connections for ROM Test

Probe	Trigger	Connect to
Start	↘	See Table 10.7-5
Stop	↗	See Table 10.7-5
Clock	↘	TP "E"
Ground		Ground

2. Verify the reading at microprocessor +5 V supply is is 0003. If it is not, the microprocessor is not free-running.
3. Use the data, start and stop probes to check the signatures given in Table 10.7-5:

Table 10.7-5. ROM U40 signatures

Data probe U140 pin	Connect Start/Stop probes to U12 pin:				
	7	9	10	11	12
11	P191	3HA1	5808	U88F	0A6P
12	618A	3HFH	60F5	70CU	UP1C
13	01UP	03A9	452P	6PC3	95FH
15	H862	34PH	7733	3C35	4102
16	61C1	C3F0	41PU	U623	AHUA
17	F8H8	73UF	3H0H	A4HF	06AF
18	5U29	FP6U	P912	2C09	7000
19	P3F3	A795	8PF7	2125	4C7P

Changing the ROM

If the ROM is changed, the data saved in the RAM has to be made compatible with the new ROM. This can be done by setting the HP 8112A to RCL0 and turning the instrument off and on again.

If the instrument becomes totally inoperable switch it off and disconnect the RAM back-up battery (by removing W2 jumper) for at least 30 seconds. This will destroy the stored RAM data. Re-connect the RAM back-up battery and switch the instrument on. The Standard Parameter Set is now loaded into the RAM.

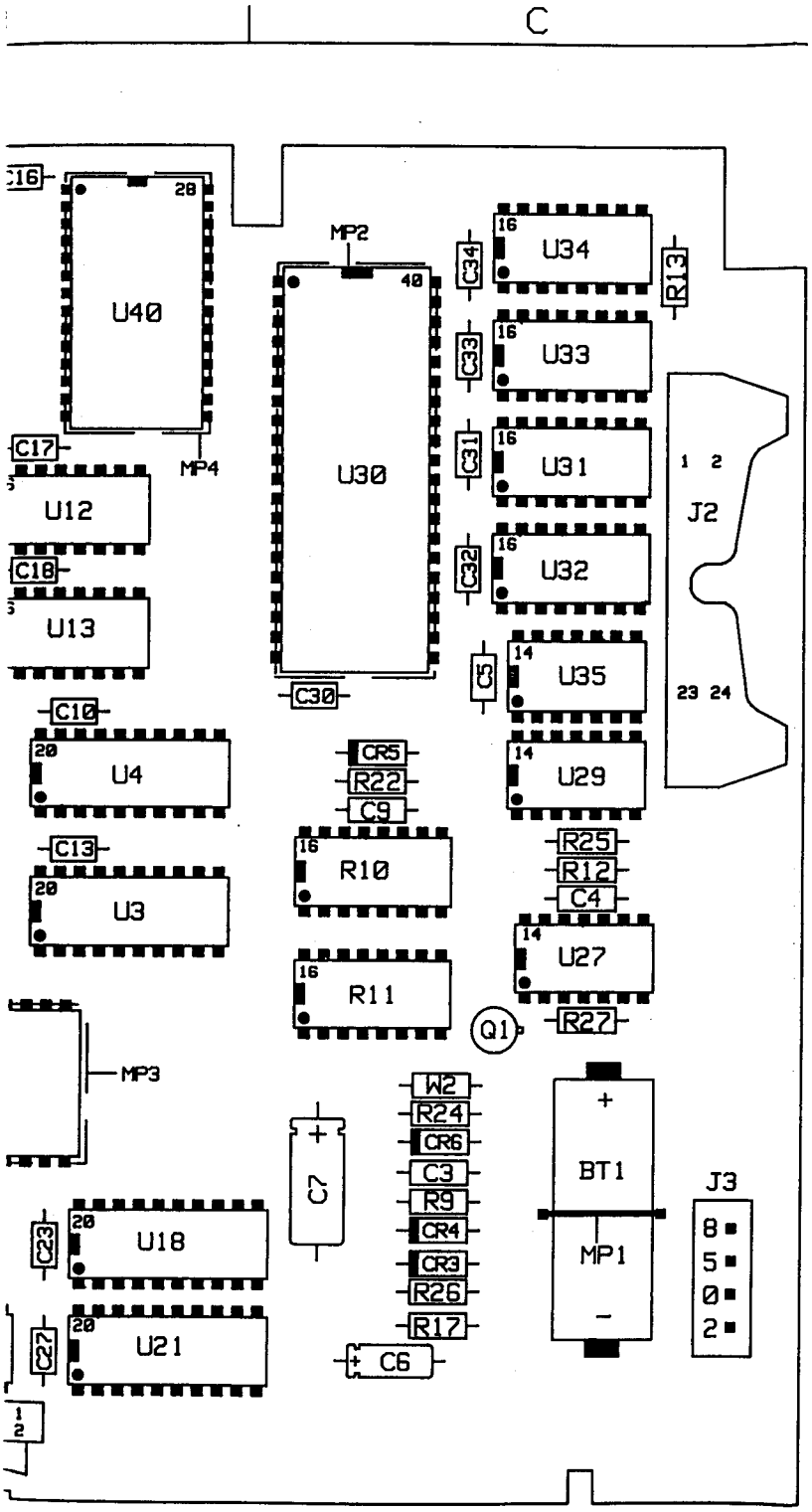
Keyboard

The keyboard can be checked using signature analysis:

1. Set the microprocessor to free-run as described in "Free Running Signature Analysis" and connect the signature analyzer probes as given in Table 10.7-2.
2. Verify the reading at microprocessor +5 V supply is is 0003. If it is not, the microprocessor is not free-running.
3. Connect the data probe to TP7, on the microprocessor board A3, and check the signature obtained when each key is pressed against Table 10.7-6.

Table 10.7-6. Keyboard signatures

Key	TP7 Signature
no key pressed	0003
LCL	9HP6
MODE1 (NORM ...)	P28A
MODE2 (E.BUR ...)	U8A1
CTRL	3P2C
PER	0U89
DEL	83P1
WID	20UC
LEE	7CUC
TRE	5PUH
HIL	F980
LOL	3263
Slope /	99HH
Slope \	2674
MAN	899P
1 Pulse	A264
Set	95PF
FIXED	P578
LINEAR	795H
GAUSS	P325
STO/RCL	8F5C
LIMIT	PUP0
COMPL	UP31
DISABLE	CU8U
Vernier MSD UP	0P5P
Vernier MSD DOWN	973F
Vernier middle UP	8394
Vernier middle DOWN	P5H4
Vernier LSD UP	60P6
Vernier LSD DOWN	3976
RANGE UP	983A
RANGE DOWN	260H



REF. DES.	GRID LOC.	REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
BT1	C3	MP1	C3	U29	C2
		MP2	C1	U30	C1
C1	B2	MP3	B2	U31	C1
C2	B2	MP4	B1	U32	C1
C3	C3			U33	C1
C4	C2	Q1	C2		
C5	C2			U34	C1
		R1	B2	U35	C2
C6	C3	R2	A3	U37	A3
C7	C3	R3	A2	U39	A1
C8	A3	R4	A2	U40	B1
C9	C2	R6	A/B2		
C10	B2			W1	A1
		R9	C3	W2	C2
C11	B2	R10	C2	W4	B3
C12	B2	R11	C2		
C13	B2	R12	C2	Y1	B3
C14	A1	R13	C1		
C15	B1				
		R14	A3		
C16	B1	R15	B1		
C17	B1	R16	B1		
C18	B1	R17	C3		
C19	B1	R19	B1		
C20	B1				
		R20	B1		
C21	A2	R21	A1		
C22	A2	R22	C2		
C23	B3	R24	C3		
C24	A2	R25	C2		
C25	A2				
		R26	C3		
C26	A3	R27	C2		
C27	B3				
C28	B3				
C29	B3	U1	B2		
C30	C2	U2	B2		
		U3	B2		
C31	C1	U4	B2		
C32	C1	U10	B1		
C33	C1				
C34	C1	U12	B1		
C35	A1	U13	B2		
C37	A3	U14	B2		
		U15	B1		
		U16	A2		
CR1	B2				
CR2	B2	U17	B3		
CR3	C3	U18	B3		
CR4	C3	U19	A2		
CR5	C2	U20	A2		
CR6	C3	U21	B3		
		U22	A2		
J1	A2	U23	A2		
J2	C1	U25	A/B3		
J3	C3	U26	A2		
J4	A1	U27	C2		
J5	A1				

FIGURE 10.7-8. MICROPROCESSOR BD A3 COMPONENT LAYOUT AND LOCATOR

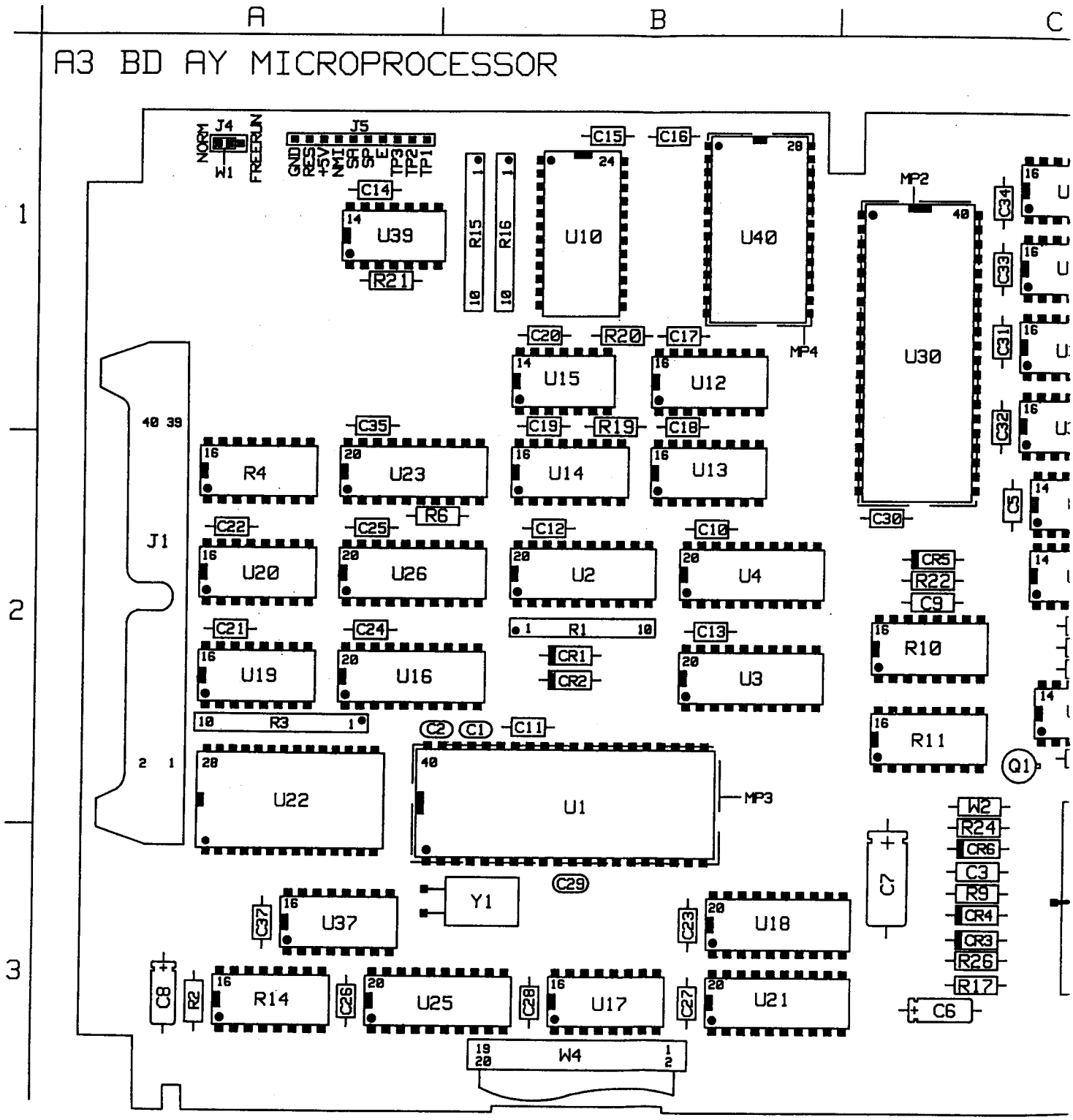
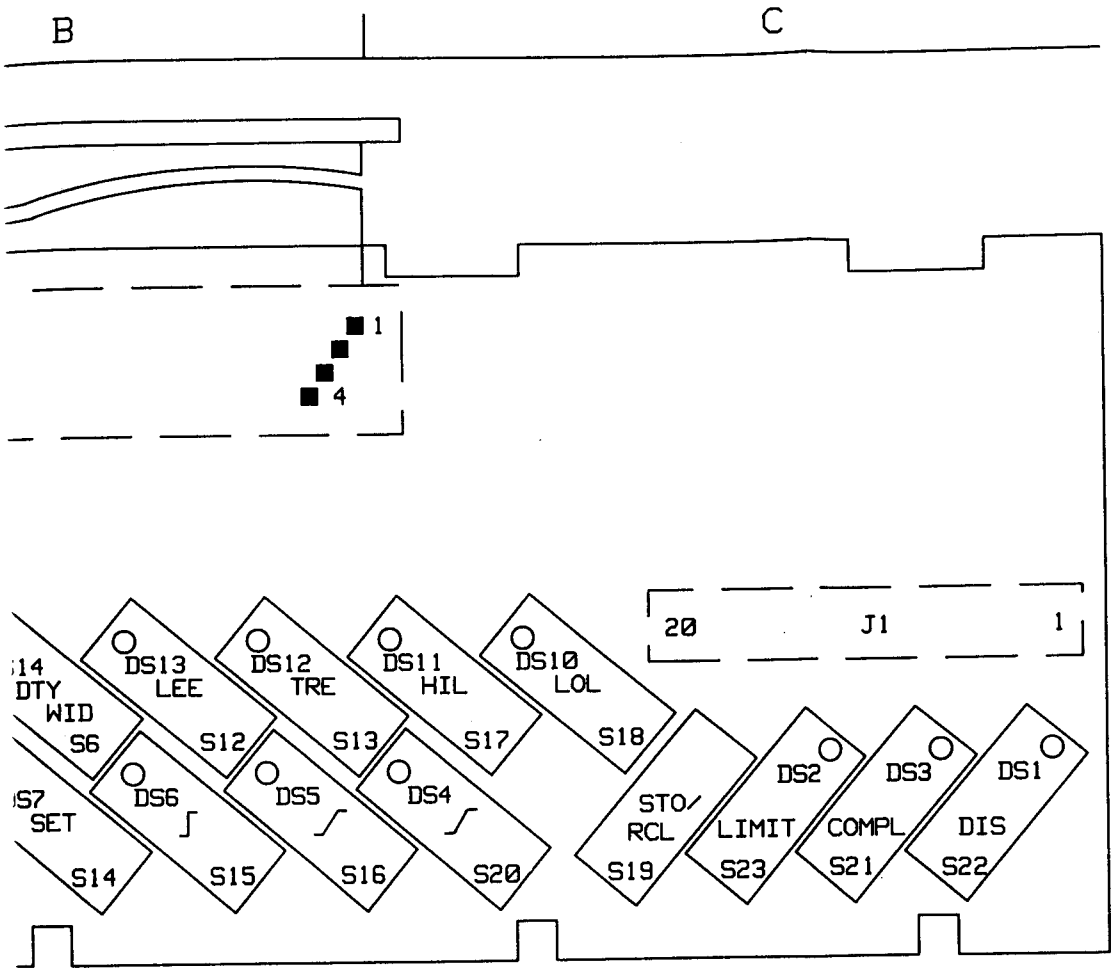
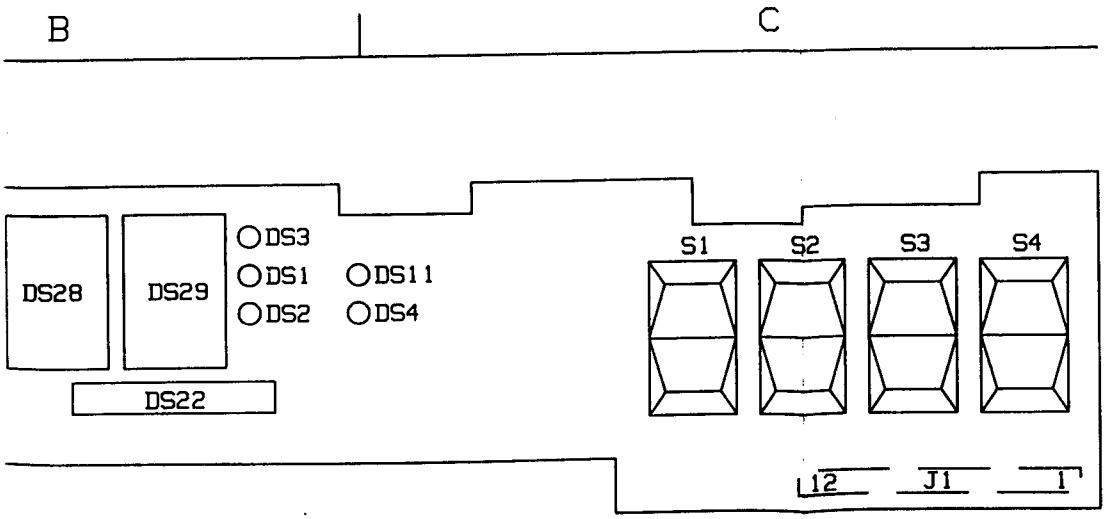

A
B
C
1
2
3
A3 BD AY MICROPROCESSOR
J4
NORM
FREERUN
W1
J5
GND
RES
+5V
NMI
SYA
SYB
SWE
TP3
TP2
TP1
C14
U39
R21
R15
R16
C15
C16
U10
U40
MP2
MP4
U30
C34
C33
C31
C32
C5
C30
C20
R20
C17
U15
U12
C19
R19
C18
U14
U13
C35
R4
U23
R6
C22
C25
C12
C10
U20
U26
U2
U4
J1
40 39
2 1
C21
C24
C13
U19
U16
U3
R1
CR1
CR2
CR5
R22
C9
R10
R11
Q1
R3
C2
C1
C11
U22
U1
MP3
W2
R24
CR6
C3
R9
CR4
CR3
R26
R17
C6
C7
Y1
C29
C37
U37
C23
U18
C8
R2
R14
C26
U25
C28
U17
C27
U21
W4

FIGURE 10.7-8.



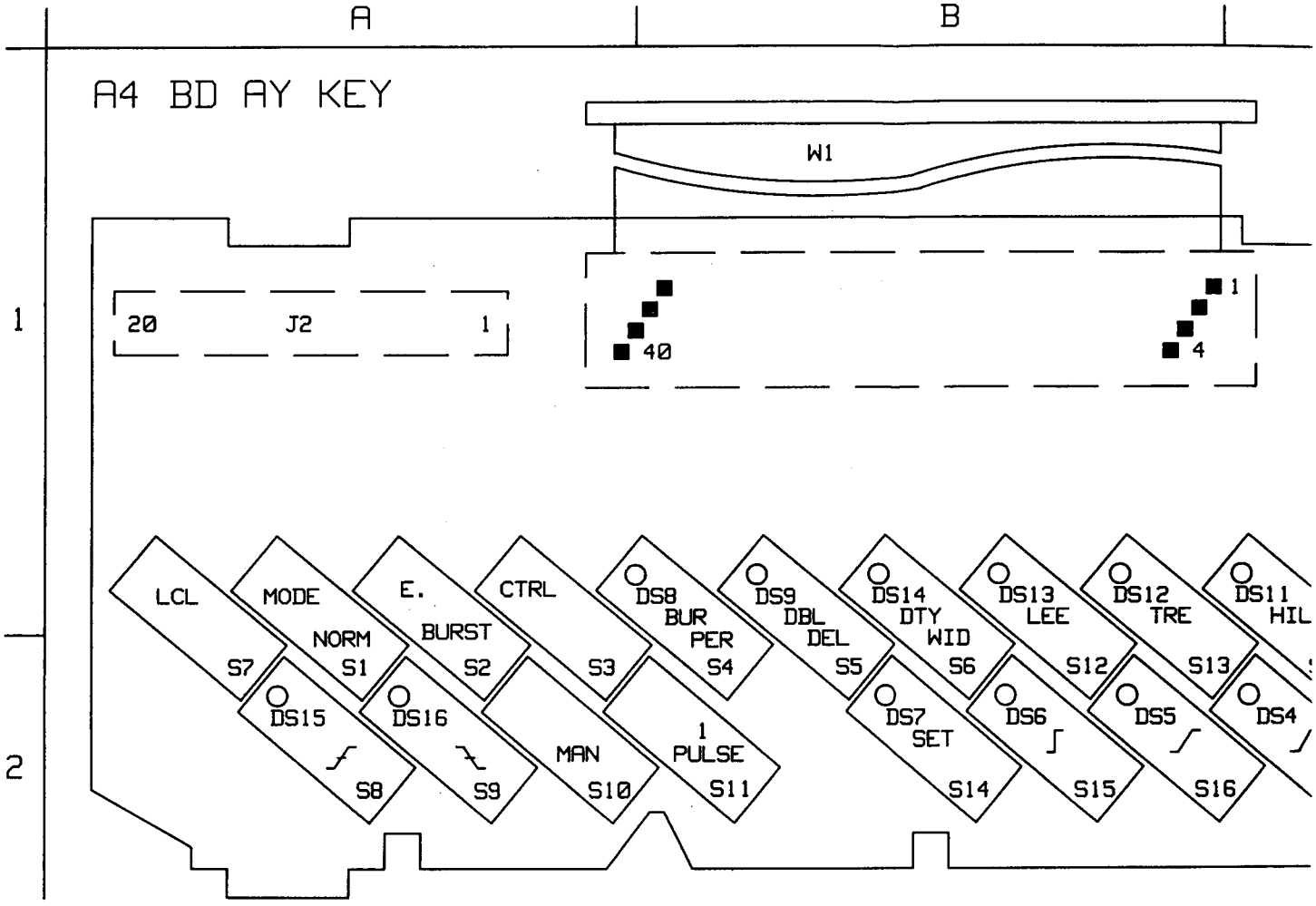
MODEL HP8112A

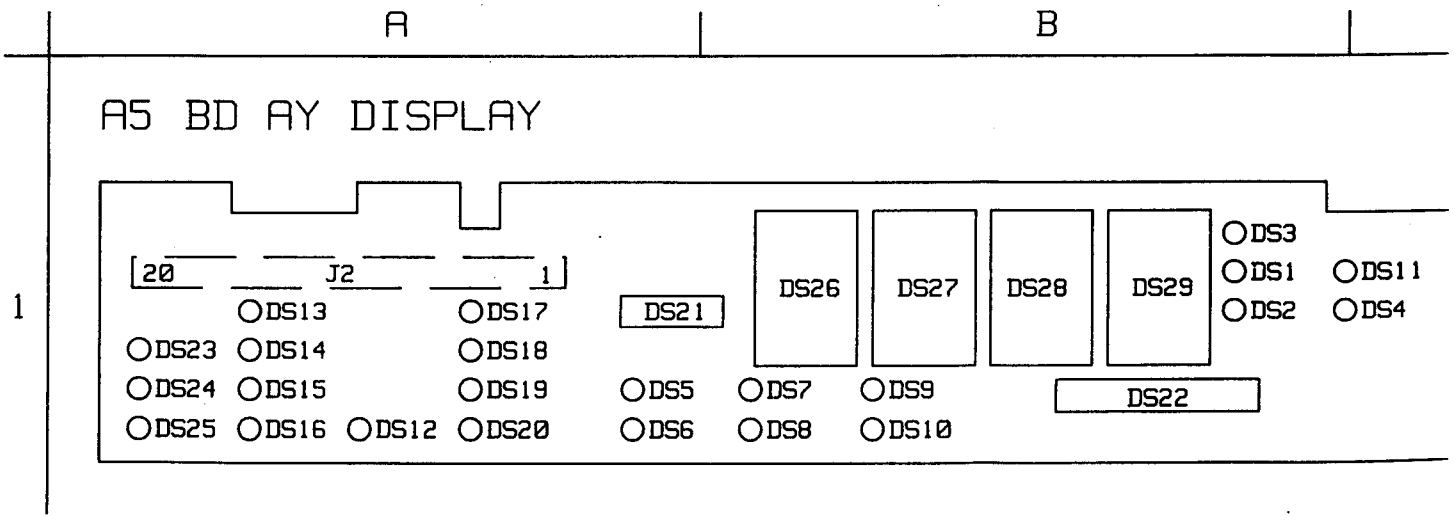
REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
DS1	C2	S18	C2
DS2	C2	S19	C2
DS3	C2	S20	C2
DS4	C2	S21	C2
DS5	B2	S22	C2
		S23	C2
DS6	B2		
DS7	B2	W1	B1
DS8	B1		
DS9	B1		
DS10	C1		
DS11	C1		
DS12	B1		
DS13	B1		
DS14	B1		
DS15	A2		
DS16	A2		
J1	C2		
J2	A1		
S1	A2		
S2	A2		
S3	A2		
S4	B2		
S5	B2		
S6	B2		
S7	A2		
S8	A2		
S9	A2		
S10	A2		
S11	A2		
S12	B2		
S13	B2		
S14	B2		
S15	B2		
S16	B2		
S17	C2		



REF. DES.	GRID LOC.	REF. DES.	GRID LOC.
DS1	B1	DS20	A1
DS2	B1	DS21	A1
DS3	B1	DS22	B1
DS4	C1	DS23	A1
DS5	A1	DS24	A1
DS6	A1	DS25	A1
DS7	B1	DS26	B1
DS8	B1	DS27	B1
DS9	B1	DS28	B1
DS10	B1	DS29	B1
DS11	C1	J1	C1
DS12	A1	J2	A1
DS13	A1		
DS14	A1	S1	C1
DS15	A1	S2	C1
		S3	C1
DS16	A1	S4	C1
DS17	A1		
DS18	A1		
DS19	A1		

FIGURE 10.7-9. KEYBOARD A4 AND DISPLAY BOARD A5 COMPONENT LAYOUTS AND LOCATORS


A
B
A4 BD AY KEY
W1
1
20
J2
1
40
1
4
2
LCL
S7
MODE
NORM
S1
E.
BURST
S2
CTRL
S3
DS8
BUR
PER
S4
DS9
DBL
DEL
S5
DS14
DTY
WID
S6
DS13
LEE
S12
DS12
TRE
S13
DS11
HIL
DS15
S8
DS16
S9
MAN
S10
1
PULSE
S11
DS7
SET
S14
DS6
S15
DS5
S16
DS4


A
B
A5 BD AY DISPLAY
1
20
J2
1
DS13
DS17
DS21
DS26
DS27
DS28
DS29
DS3
DS1
DS11
DS2
DS4
DS23
DS14
DS18
DS24
DS15
DS19
DS5
DS7
DS9
DS22
DS25
DS16
DS12
DS20
DS6
DS8
DS10

A

Replaceable Parts

Introduction

General

This Appendix contains information for ordering all the replaceable parts contained in the HP 8112A.

The information consists of the following:

- The schematic and component layout reference.
- The Hewlett-Packard part-number.
- The part-number check-digit.
- The part description.
- The Hewlett-Packard reference number for the part manufacturer.
- The manufacturer's part-number.

A list of manufacturers and their Hewlett-Packard reference numbers is given in Table A-1. Figure A-1 and Figure A-2 identify the main mechanical parts of the instrument.

Ordering Parts

To order a part listed in one of the parts-lists, you must quote the Hewlett-Packard part-number and check-digit, together with the quantity required, and send the order to the nearest Hewlett-Packard office. A list of Sales & Service offices is given in Appendix D.

If you require a part which is not listed in one of the parts-lists, then quote the instrument model-number, serial number, and the function/description of the part.

Within the USA you can use the Hewlett-Packard direct mail-order system. This offers the following advantages:

- Ordering and shipment are via the HP Parts Center in Mountain View, California.
- There is no maximum or minimum order value.
- A small handling charge means that all transportation is pre-paid.
- Payment must accompany the order, therefore there is no invoice processing.

The mail-order forms required to use this system are available from your local Hewlett-Packard office.

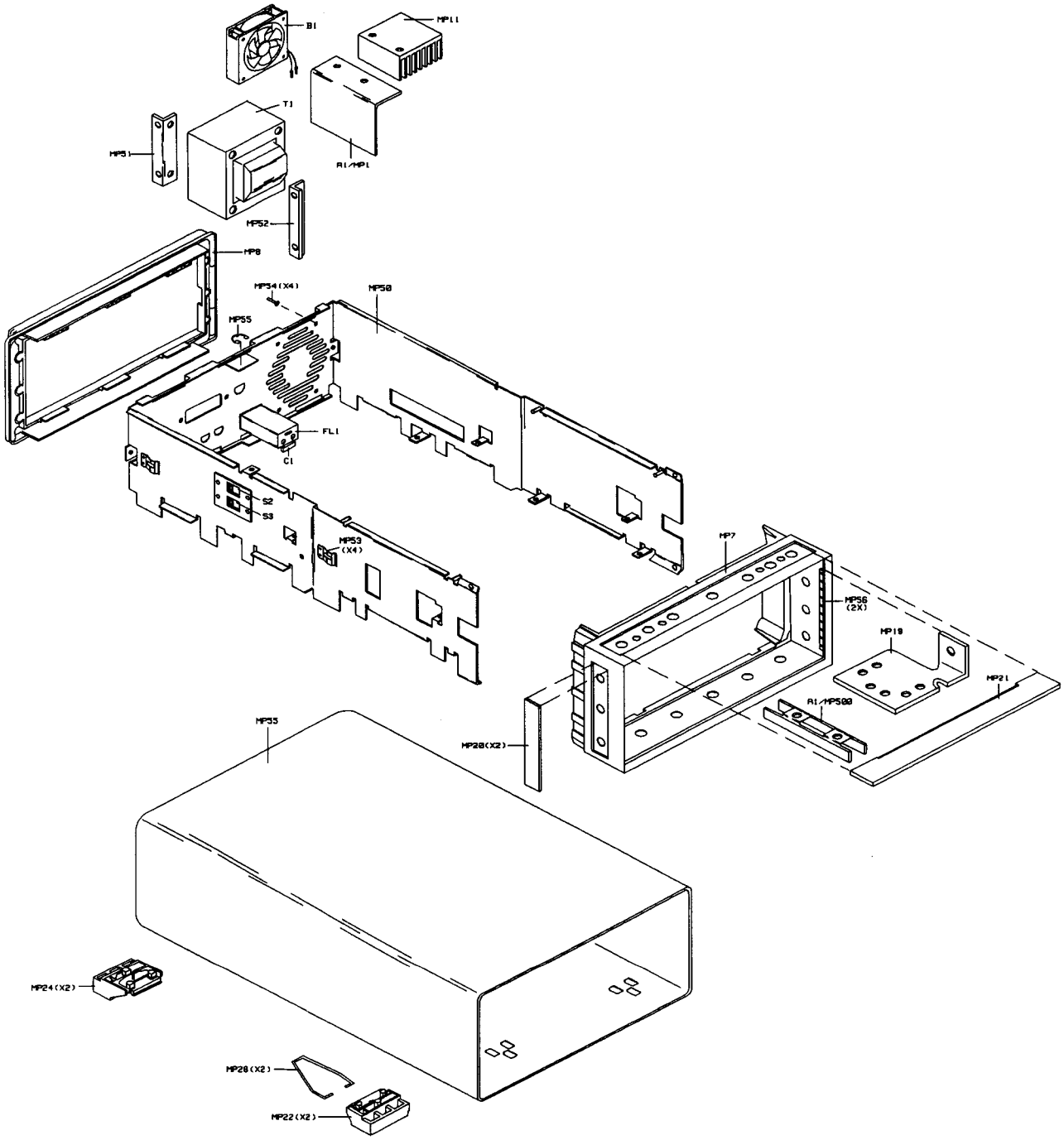


Figure A-1. Mechanical Parts - 1

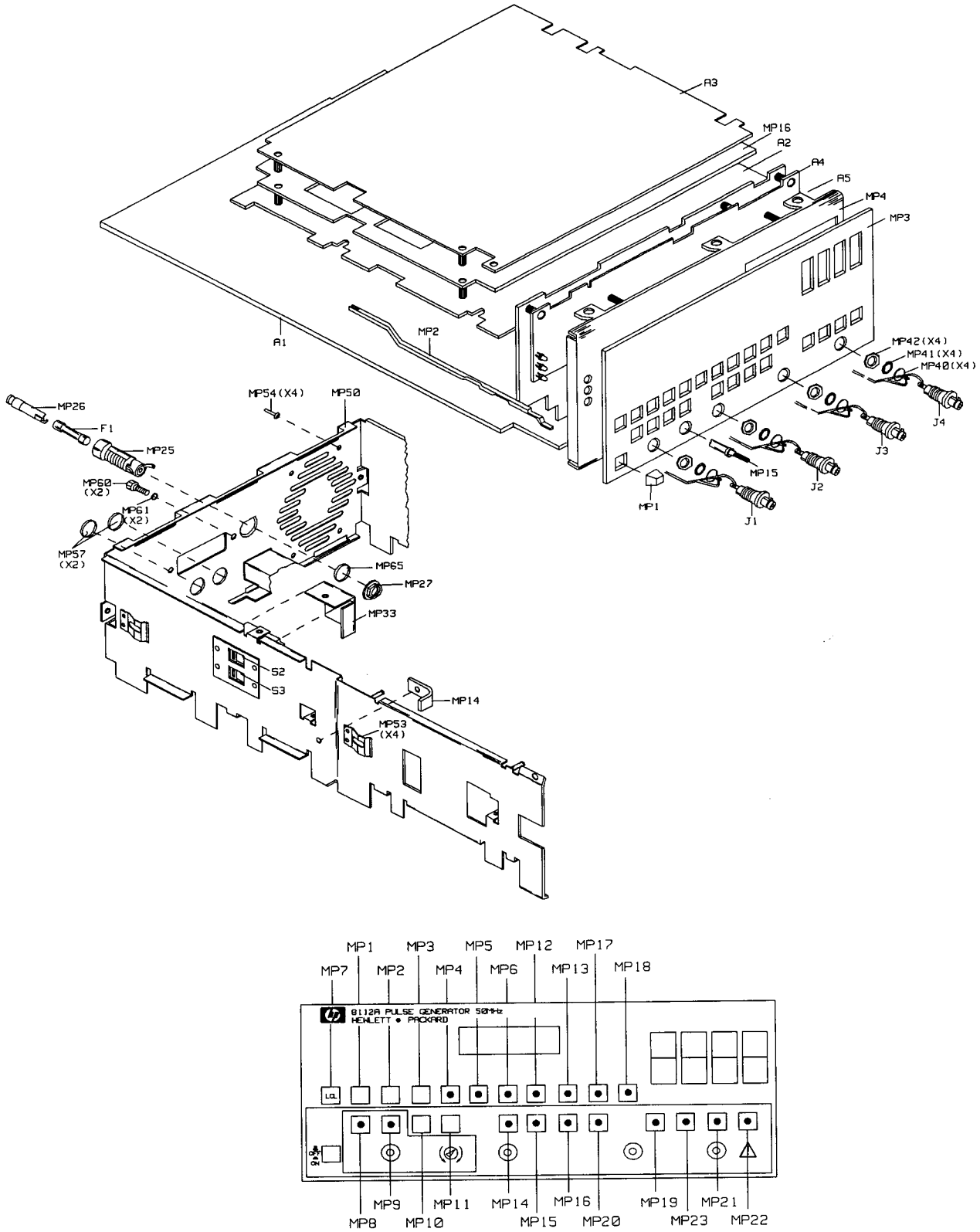


Figure A-2. Mechanical Parts - 2

Table A-1. HP 8112A Parts Manufacturers

Reference	Name
00046	UNITRODE CORP
00359	O'HARA METAL PRODUCTS CO
00493	UNITED CHEMI-CON INC
00746	ROHM CORP
01020	COLORADO SCREW MACHINE CO
01074	HOLSWORTHY ELECTRONICS LTD
01136	ELCO INDUSTRIES INC
01339	GETTIG ENGRG & MFG CO INC
01380	AMP INC
01461	GOE ENGINEERING CO INC
01468	STETTNER & CO
01542	HP DIV 01 SAN JOSE COMPONENTS
01607	ALLEN-BRADLEY CO INC
01698	TEXAS INSTRUMENTS INC
01854	RCL ELECTRONICS INC
01876	HP DIV 02 SCD IC'S
02010	AVX CORP
02037	MOTOROLA INC
02062	HP DIV 05 MSD
02121	LYN-TRON INC
02123	EG & G INC
02137	CHAMPLAIN CABLE CORP DIV HERCULES
02180	PRECISION MONOLITHICS INC
02367	CORNELL-DUBILIER/SANGAMO
02414	BURNDY CORP
02440	THOMPSON BREMER DIV VARE
02465	ANILLO INDUSTRIES INC
02483	CTS CORP
02499	IRC INC
02531	CHICAGO RIVET & MACHINE CO
02582	CLAROSTAT MFG CO INC
02608	THERMALLOY INC
02688	MICROSEMI CORP
02744	ELEC-TROL INC
02805	COOPER INDUSTRIES INC
02946	DUPONT E I DE NEMOURS & CO
02995	NORTH AMERICAN PHILIPS CORP
03273	GOWANDA ELECTRONICS CORP
03285	ANALOG DEVICES INC
03316	SPECIALTY CONNECTOR CO

Reference	Name
03394	METHODE ELECTRONICS INC
03406	NATIONAL SEMICONDUCTOR CORP
03418	MOLEX INC
03480	HEYCO MOLDED PRODUCTS
03744	BOURNS NETWORKS INC
03799	HARRIS CORP
03827	FAIR RITE PRODUCTS CORP
04068	LABINAL COMPONENTS & SYSTEMS INC
04078	SGS-THOMSON MICROELECTRONICS INC
04200	SPRAGUE ELECTRIC CO
04225	THOMAS & BETTS CORP
04486	ITT CORP
04504	GENERAL INSTRUMENT CORP
04539	G C ELECTRONICS CO
04568	BECKMAN INDUSTRIAL CORP
04605	FISCHER SPECIAL MFG CO
04703	LITTELFUSE INC
04726	3M CO
04775	NATIONAL LOCK WASHER CO
04805	ILLINOIS TOOL WORKS INC SHAKEPROOF
04821	TILLEY MFG CO
04822	STACKPOLE CARBON CO
04880	ZIERICK MFG CO
05131	ELECTRONIC DEVICES INC
05176	AMERICAN SHIZUKI CORP
05518	AUGAT INC
05524	DALE ELECTRONICS INC
05584	DURALITH CORP
05610	CAMCAR SCREW & MFG CO
05912	RUDOLF SCHADOW GMBH
05937	RAYCHEM GMBH
05992	EFCO COMPOSANTS
06113	HIPP ESSLINGEN
06121	SIEMENS AG
06328	SCHURTER AG
06352	TDK CORPORATION OF AMERICA
06653	KLAR
07492	ELECTRO DYNAMICS CORP
08360	DAUT + RIETZ GMBH & CO KG
08623	WOLFLE & CO

Table A-1. HP 8112A Parts Manufacturers (continued)

Reference	Name
08709	PANASONIC INDUSTRIAL CO
08839	COMATEL
09442	REAL-PACK
09538	TUSONIX
09939	MURATA ERIE NORTH AMERICA INC

Reference	Name
10358	VOGT AG
11039	PAPST MECHATRONIC CORP
12482	BRADFORD ELECTRONICS INC
28480	HEWLETT PACKARD COMPANY

Standard Instrument Parts-lists

Master List

Table A-2. Standard HP 8112A Master Parts List

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A0	8112A	8	1	PROGRAMM PULSGEN	28480	8112A
A0 A1	08112-66521	3	1	BD AY MAIN	28480	08112-66511
A0 A2	08112-66502	2	1	BD AY CONTROL	28480	08112-66502
A0 A3	08112-66535	0	1	BD AY MICROPROCR	28480	08112-66534
A0 A4	08112-66504	4	1	BD AY KEY	28480	08112-66504
A0 A5	08112-66505	5	1	BD AY DISPLAY	28480	08112-66505
A0 B1	3160-0497	2	1	FAN-TBAX	11039	612
A0 C1	0160-4323	8	1	CAP 0.047uF 0 V	11892	PME271M547M
A0 F1	2110-0043	8	1	FUSE 1.5A 250V	04703	312 01.5
A0 J1	1250-0083	1	1	CONN-RF BNC	05879	31-221-1020
A0 J2	1250-0083	1	1	CONN-RF BNC	05879	31-221-1020
A0 J3	1250-0083	1	1	CONN-RF BNC	05879	31-221-1020
A0 J4	1250-0083	1	1	CONN-RF BNC	05879	31-221-1020
A0 MP1	5041-0531	5	1		28480	5041-0531
A0 MP2	5040-9317	1	1		28480	5040-9317
A0 MP3	4040-1971	6	1	LABEL-INFO	05584	
A0 MP4	08112-00204	3	1		28480	08112-00204
A0 MP7	5021-8413	6	1		28480	5021-8413
A0 MP8	03478-88304	5	1	BEZEL REAR	28480	5021-5814
A0 MP11	08116-21107	7	1	HEATSINK POWER	28480	08112-21105
A0 MP14	08116-04154	0	1	KEEPER	28480	08112-04154
A0 MP15	5040-1136	6	1		28480	5040-1136
A0 MP16	08112-00601	4	1		28480	08112-00601
A0 MP19	08116-21102	8	1		28480	08116-21102
A0 MP20	5001-0538	8	1		28480	5001-0538
A0 MP21	5041-8803	0	1		28480	5041-8803
A0 MP22	5041-8801	8	1		28480	5041-8801
A0 MP24	5041-8822	3	1		28480	5041-8822
A0 MP25	2110-0566	8	1	FUSEHOLDER BODY	06328	031.1657
A0 MP26	2110-0565	9	1	FUSEHOLDER CAP	06328	031.1666

Table A-2. Standard HP 8112A Master Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A0 MP27	2110-0569	3	1	FUHLR-CMPNT	06328	098.0043
A0 MP28	1460-1345	5	1	TILT STAND	00359	
A0 MP30	1400-0290	1	1	BRACKET-RTANG	04604	129530
A0 MP33	08116-40601	2	1		28480	08116-40601
A0 MP40	0360-1190	5	1	TERM-SOLDER LUG	04880	720-.380H
A0 MP42	2950-0043	8	1	NUT-HEX-DBL-CHAM	04605	28200-10-101
A0 MP50	08116-60101	9	1	CHASSIS	28480	08116-60101
A0 MP51	08116-01203	8	1	BRACKET-XFMR	28480	08116-01203
A0 MP52	08116-01201	6	1	BRACKET-XFMR	28480	08116-01201
A0 MP54	0624-0413	3	1	SCR-TPG 8-16	05610	224-41390-382
A0 MP55	08116-04123	7	1	COVER	28480	08116-04123
A0 MP56	0363-0125	7	2	RFI STRP-FINGERS	03647	97-555
A0 MP57	6960-0001	7	2	HOLE PLUG		
A0 MP58	5180-2462	7	2	HP-IB CABLE ASSY		
A0 MP60	0380-1482	0	1	STDF-HEX .34-IN	02685	
A0 T1	08112-61101	7	1		28480	08112-61101

Main Board

Table A-3. Main Board Parts List

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1	08112-66521	3	1	BD AY-MAIN	28480	08112-66521
A1 C1	0180-3159	8	1	CAP 25 V	00493	NM25VN103Q25X51
A1 C2	0180-3158	7	1	CAP 6800uF 16 V	00493	NM16VN682Q22X41
A1 C3	0180-3160	1	1	CAP 2200uF 50 V	00493	NM50VN222Q22X41
A1 C4	0180-3160	1	1	CAP 2200uF 50 V	00493	NM50VN222Q22X41
A1 C5	0180-4313	8	1	CAP 2200uF 50 V	00493	KME50VB222M18X35LL
A1 C6	0180-3008	6	1	CAP 470uF 35 V	04200	502D477F035EG1D
A1 C7	0180-2984	5	1	CAP 47uF 50 V	00493	SM50VB47R(M)8X11
A1 C8	0180-2984	5	1	CAP 47uF 50 V	00493	SM50VB47R(M)8X11
A1 C9	0180-2984	5	1	CAP 47uF 50 V	00493	SM50VB47R(M)8X11
A1 C10	0180-2984	5	1	CAP 47uF 50 V	00493	SM50VB47R(M)8X11
A1 C11	0180-2962	9	1	CAP 220uF 10 V	00493	SL10VB221T10X16
A1 C12	0180-2962	9	1	CAP 220uF 10 V	00493	SL10VB221T10X16
A1 C13	0180-2962	9	1	CAP 220uF 10 V	00493	SL10VB221T10X16
A1 C14	0160-2055	9	1	CAP 0.01uF 100 V	09538	805-504 Y5V 103Z
A1 C15	0160-2055	9	1	CAP 0.01uF 100 V	09538	805-504 Y5V 103Z
A1 C16	0160-2055	9	1	CAP 0.01uF 100 V	09538	805-504 Y5V 103Z
A1 C17	0160-2055	9	1	CAP 0.01uF 100 V	09538	805-504 Y5V 103Z
A1 C18	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C19	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C100	0180-0116	1	1	CAP 6.8uF 35 V	04200	150D685X9035B2-DYS
A1 C101	0180-0116	1	1	CAP 6.8uF 35 V	04200	150D685X9035B2-DYS
A1 C102	0180-0374	3	1	CAP 10uF 20 V	04200	150D106X9020B2-DYS
A1 C103	0180-0374	3	1	CAP 10uF 20 V	04200	150D106X9020B2-DYS
A1 C104	0180-0116	1	1	CAP 6.8uF 35 V	04200	150D685X9035B2-DYS
A1 C105	0180-0116	1	1	CAP 6.8uF 35 V	04200	150D685X9035B2-DYS
A1 C106	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C110	0160-3873	1	1	CAP 4.7pF 200 V	06352	FD12C0G2D4R7D
A1 C111	0160-4385	2	1	CAP 15pF 200 V	09939	RPE121-105C0G150J200V
A1 C112	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 C113	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C114	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C115	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C116	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C131	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C132	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C133	0160-0572	1	1	CAP 2200pF 100 V	02010	SR201C222MAAH
A1 C134	0160-0573	2	1	CAP 4700pF 100 V	02010	SR201C472MAAH
A1 C140	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C200	0160-4521	8		CAP 12pF 200 V	06352	FD12C0G2D120J
A1 C201	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C202	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C204	0160-0575	4	1	CAP 0.047uF 50 V	02010	SR205C473MAAH
A1 C205	0160-0575	4	1	CAP 0.047uF 50 V	02010	SR205C473MAAH
A1 C220	0160-4521	8		CAP 12pF 200 V	06352	FD12C0G2D120J
A1 C221	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C222	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C224	0160-0575	4	1	CAP 0.047uF 50 V	02010	SR205C473MAAH
A1 C225	0160-0575	4	1	CAP 0.047uF 50 V	02010	SR205C473MAAH
A1 C240	0160-4385	2		CAP 15pF 200 V	09939	RPE121-105C0G150J200V
A1 C241	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C242	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C244	0160-0575	4	1	CAP 0.047uF 50 V	02010	SR205C473MAAH
A1 C246	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C280	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C281	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C282	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C283	0160-3878	6	1	CAP 1000pF 100 V	02010	SR201C102MAAH
A1 C300	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C301	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 C303	0160-4493	3	1	CAP 27pF 200 V	06352	FD12C0G2D270J
A1 C304	0121-0046	2	1	CAP 35pF 9pF 200	09538	538-016 D 9-35
A1 C305	0160-3766	1	1	CAP 1000pF 100 V	02367	CD15FA102FO3
A1 C306	0160-3548	7	1	CAP 0.01uF 100 V	02367	CD19.5FA103F03
A1 C307	0160-4622	0	1	CAP 0.1uF 160 V	05992	23410410
A1 C308	0160-3726	3	1	CAP 1uF 40 V	05992	23110550
A1 C309	0160-3998	1	1	CAP 10uF 40 V	05992	23110650
A1 C310	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C311	0160-0572	1	1	CAP 2200pF 100 V	02010	SR201C222MAAH
A1 C312	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C313	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C314	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C315	0160-4386	3	1	CAP 33pF 200 V	09939	RPE121-105C0G330J200V
A1 C316	0160-4385	2	1	CAP 15pF 200 V	09939	RPE121-105C0G150J200V
A1 C318	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C320	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C321	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C322	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C400	0160-0575	4	1	CAP 0.047uF 50 V	02010	SR205C473MAAH
A1 C401	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C402	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C403	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C405	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C409	0160-4381	8		CAP 1.5pF 200 V	06352	FD11C0G2D1R5C
A1 C410	0121-0466	0	1	CAP 3pF 1pF 100	09538	518-003 A 1-3
A1 C414	0160-5738	1		CAP 6.8pF 100 V	06121	B37979-J1060-D834
A1 C415	0160-5731	4	1	CAP 220pF 100 V	06121	B37986-J1221-J034
A1 C501	0160-5742	7		CAP 27pF 100 V	06121	B37979-J1270-J034
A1 C502	0160-4512	7	1	CAP 120pF 200 V	02010	SR202A121JAAH
A1 C503	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 C504	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C505	0160-0572	1	1	CAP 2200pF 100 V	02010	SR201C222MAAH
A1 C506	0160-3878	6	1	CAP 1000pF 100 V	02010	SR201C102MAAH
A1 C507	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C508	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C509	0160-3878	6	1	CAP 1000pF 100 V	02010	SR201C102MAAH
A1 C510	0160-3878	6	1	CAP 1000pF 100 V	02010	SR201C102MAAH
A1 C511	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A1 C512	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C513	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C514	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C515	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C516	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C517	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C518	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C519	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C520	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C521	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C522	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A1 C523	0180-0582	5	1	CAP 270uF 40 V	04200	672D277H040DT4C
A1 C524	0180-0582	5	1	CAP 270uF 40 V	04200	672D277H040DT4C
A1 C525	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C526	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A1 C528	0160-4381	8	1	CAP 1.5pF 200 V	06352	FD11C0G2D1R5C
A1 C529	0160-4381	8	1	CAP 1.5pF 200 V	06352	FD11C0G2D1R5C
A1 C530	0121-0466	0	1	CAP 3pF 1pF 100	09538	518-003 A 1-3
A1 C531	0160-4380	7	1	CAP 1pF 200 V	06352	FD11C0K2D1R0C
A1 C532	0160-3872	0		CAP 2.2pF 200 V	06352	FD12C0G2D2R2C
A1 C535	0160-4387	4		CAP 47pF 200 V	06352	FD12C0G2D470J
A1 C541	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 CR1	1901-0638	3	1	DIO-FW BRDG 100V	04504	KBU4B
A1 CR2	1906-0096	7	1	DIO-FW BRDG 200V	05131	
A1 CR3	1906-0096	7	1	DIO-FW BRDG 200V	05131	
A1 CR4	1901-1098	1	1	DIO-1N4150	04486	
A1 CR5	1901-1098	1	1	DIO-1N4150	04486	
A1 CR6	1901-1098	1	1	DIO-1N4150	04486	
A1 CR7	1901-1098	1	1	DIO-1N4150	04486	
A1 CR8	1901-1098	1	1	DIO-1N4150	04486	
A1 CR9	1901-1098	1	1	DIO-1N4150	04486	
A1 CR130	1901-1098	1	1	DIO-1N4150	04486	
A1 CR131	1901-1098	1	1	DIO-1N4150	04486	
A1 CR132	1901-1098	1	1	DIO-1N4150	04486	
A1 CR133	1901-1098	1	1	DIO-1N4150	04486	
A1 CR140	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A1 CR141	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A1 CR142	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A1 CR143	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A1 CR200	1901-1068	5	1	DIO- SCHOTTKY SM	02062	5082-5541
A1 CR201	1901-1068	5	1	DIO- SCHOTTKY SM	02062	5082-5541
A1 CR220	1901-1068	5	1	DIO- SCHOTTKY SM	02062	5082-5541
A1 CR221	1901-1068	5	1	DIO- SCHOTTKY SM	02062	5082-5541
A1 CR240	1901-1068	5	1	DIO- SCHOTTKY SM	02062	5082-5541
A1 CR241	1901-1068	5	1	DIO- SCHOTTKY SM	02062	5082-5541
A1 CR401	1901-1098	1	1	DIO-1N4150	04486	
A1 CR402	1901-1098	1	1	DIO-1N4150	04486	
A1 CR403	1901-0518	8	1	DIO- SCHOTTKY SM	02062	5082-5509
A1 CR404	1901-0518	8	1	DIO- SCHOTTKY SM	02062	5082-5509
A1 CR501	1901-1098	1	1	DIO-1N4150	04486	
A1 CR502	1901-1098	1	1	DIO-1N4150	04486	
A1 CR503	1901-0179	7	1	DIO-SWITCHING	03406	FD777

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 CR504	1901-0179	7	1	DIO-SWITCHING	03406	FD777
A1 CR505	1901-0179	7	1	DIO-SWITCHING	03406	FD777
A1 CR506	1901-0179	7	1	DIO-SWITCHING	03406	FD777
A1 CR513	1901-0732	8	1	DIO-PWR RECT	02037	SR3010-4RL
A1 CR514	1901-0732	8	1	DIO-PWR RECT	02037	SR3010-4RL
A1 J1	1251-5184	5	1	CONN-POST-TP-HDR	03418	26-60-0070
A1 J2	1252-0277	9	1	CONN-POST-TP-HDR	04726	3428-6202
A1 J3	1251-3305	8	1	CONN-POST-TP-HDR	03418	26-60-1040
A1 J200	1200-0541	1	1	SKT-IC-DIP	02414	DILB24P-308T
A1 J220	1200-0541	1	1	SKT-IC-DIP	02414	DILB24P-308T
A1 J240	1200-0541	1	1	SKT-IC-DIP	02414	DILB24P-308T
A1 J301	1200-0541	1	1	SKT-IC-DIP	02414	DILB24P-308T
A1 J401	1200-0541	1	1	SKT-IC-DIP	02414	DILB24P-308T
A1 K100	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 K300	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 K500	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 K501	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 K502	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 K503	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 K504	0490-1412	9	1	RLY-REED 1A	11263	3570.1332.053
A1 L200	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L220	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L280	9100-2255	4	1	L 470NH +-10%	03273	10M470K
A1 L501	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L502	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L503	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L504	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L507	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L508	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L509	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 L510	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L511	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L512	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L514	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 L515	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A1 MP1	08116-21106	6	1		28480	08116-21106
A1 MP2	08112-45401	6	1		28480	08112-45401
A1 MP3	08112-45401	6	1		28480	08112-45401
A1 MP100	08112-04155	1	1		28480	08112-04155
A1 MP200	1205-0235	0	1	HEAT SINK	02608	2224-B
A1 MP201	1205-0235	0	1	HEAT SINK	02608	2224-B
A1 MP500	08116-04152	2	1		28480	08116-04152
A1 MP505	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP506	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP508	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP509	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP510	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP511	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP512	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 MP513	1205-0662	7	1	HEAT SINK	02123	260-4TH5B-SPECIAL THREAD
A1 Q1	1854-0368	5	1	XSTR NPN 2N5191	02037	2N5191
A1 Q2	1854-0637	1	1	XSTR NPN 2N2219A	02037	2N2219A
A1 Q3	1854-0368	5	1	XSTR NPN 2N5191	02037	2N5191
A1 Q4	1854-0637	1	1	XSTR NPN 2N2219A	02037	2N2219A
A1 Q5	1853-0314	9	1	XSTR PNP 2N2905A	02037	2N2905A
A1 Q6	1853-0212	6	1	XSTR PNP 2N5194	02037	2N5194
A1 Q140	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q141	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q142	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q143	1854-1028	6	1	XSTR NPN SI	02037	2N3904

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 Q200	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q220	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q280	1854-1139	0	1	XSTR NPN SI	02037	MPSH10
A1 Q281	1854-1139	0	1	XSTR NPN SI	02037	MPSH10
A1 Q282	1853-0357	0	1	XSTR PNP SI	02037	
A1 Q283	1853-0357	0	1	XSTR PNP SI	02037	
A1 Q300	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A1 Q301	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A1 Q302	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A1 Q303	1853-0354	7	1	XSTR PNP SI	02037	
A1 Q304	1853-0354	7	1	XSTR PNP SI	02037	
A1 Q305	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q306	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q307	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q308	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q309	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q310	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A1 Q311	1853-0569	6	1	XSTR PNP SI	02037	
A1 Q312	1853-0569	6	1	XSTR PNP SI	02037	
A1 Q313	1853-0569	6	1	XSTR PNP SI	02037	
A1 Q314	1853-0569	6	1	XSTR PNP SI	02037	
A1 Q315	1853-0569	6	1	XSTR PNP SI	02037	
A1 Q400	1853-0589	0	1	XSTR-DUAL PNP	02037	MD4260
A1 Q402	1853-0218	2	1	XSTR PNP SI	03406	NS65098
A1 Q403	1855-0386	9	1	J-FET 2N4392	02037	2N4392
A1 Q404	1853-0569	6	1	XSTR PNP SI	02037	
A1 Q501	1854-0809	9	1	XSTR NPN 2N2369A	02037	2N2369A
A1 Q502	1853-0405	9	1	XSTR PNP SI	02037	2N4209
A1 Q503	1854-0354	9	1	XSTR NPN SI	02037	
A1 Q504	1853-0357	0	1	XSTR PNP SI	02037	

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 Q505	1853-0312	7	1	XSTR PNP SI	02037	
A1 Q506	1854-0597	2	1	XSTR NPN 2N5943	02037	2N5943
A1 Q507	1854-0477	7	1	XSTR NPN 2N2222A	02037	2N2222A
A1 Q508	1854-0597	2	1	XSTR NPN 2N5943	02037	2N5943
A1 Q509	1853-0312	7	1	XSTR PNP SI	02037	
A1 Q510	1854-0597	2	1	XSTR NPN 2N5943	02037	2N5943
A1 Q511	1853-0312	7	1	XSTR PNP SI	02037	
A1 Q512	1854-0597	2	1	XSTR NPN 2N5943	02037	2N5943
A1 Q513	1853-0312	7	1	XSTR PNP SI	02037	
A1 Q514	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A1 Q515	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q516	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q517	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A1 Q518	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 Q519	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A1 R1	0764-0013	5	1	RES 56 5% 2W MO	02499	GS-3
A1 R2	0812-0111	7	1	RES .05 3% 3W	05524	RS-2B
A1 R3	0698-4508	0	1	RES 78.7K 1%	05524	CMF-55-1
A1 R4	0698-0085	0	1	RES 2.61K 1%	05524	CMF-55-1
A1 R5	0812-0045	6	1	RES .15 5% 3W	05524	CW-2B-39
A1 R6	0757-0460	1	1	RES 61.9K 1%	05524	CMF-55-1
A1 R7	0698-0085	0	1	RES 2.61K 1%	05524	CMF-55-1
A1 R8	0698-0085	0	1	RES 2.61K 1%	05524	CMF-55-1
A1 R9	0757-0464	5	1	RES 90.9K 1%	05524	CMF-55-1
A1 R10	0812-0111	7	1	RES .05 3% 3W	05524	RS-2B
A1 R11	0698-4460	3	1	RES 649 1% .125W	05524	CMF-55-1
A1 R12	2100-3211	7	1	RES-TRMR 1K 10%	03744	3386P-Y46-102
A1 R13	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R14	0698-6320	8	1	RES 5K .1% .125W	05524	CMF-55-1, T-9
A1 R15	0698-6320	8	1	RES 5K .1% .125W	05524	CMF-55-1, T-9

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R16	0698-3442	9	1	RES 237 1% .125W	05524	CMF-55-1
A1 R17	0757-0434	9	1	RES 3.65K 1%	05524	CMF-55-1
A1 R18	2100-3211	7	1	RES-TRMR 1K 10%	03744	3386P-Y46-102
A1 R19	2100-3211	7	1	RES-TRMR 1K 10%	03744	3386P-Y46-102
A1 R20	0757-0434	9	1	RES 3.65K 1%	05524	CMF-55-1
A1 R21	0698-3442	9	1	RES 237 1% .125W	05524	CMF-55-1
A1 R22	0698-4421	6	1	RES 249 1% .125W	05524	CMF-55-1
A1 R23	0698-4435	2	1	RES 2.49K 1%	05524	CMF-55-1
A1 R24	2100-0554	5	1	RES-TRMR 500 10%	03744	3386P-Y46-501

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R130	0757-0438	3	1	RES 5.11K 1%	05524	CMF-55-1
A1 R131	0757-0289	2	1	RES 13.3K 1%	05524	CMF-55-1
A1 R132	0757-0441	8	1	RES 8.25K 1%	05524	CMF-55-1
A1 R134	0698-0085	0	1	RES 2.61K 1%	05524	CMF-55-1
A1 R135	0698-3268	7	1	RES 11.5K 1%	05524	CMF-55-1
A1 R136	0698-0084	9	1	RES 2.15K 1%	05524	CMF-55-1
A1 R137	0757-0460	1	1	RES 61.9K 1%	05524	CMF-55-1
A1 R138	0757-0289	2	1	RES 13.3K 1%	05524	CMF-55-1
A1 R139	0698-7258	3	1	RES 8.25K 1%	05524	CMF-50-2
A1 R140	0698-7268	5	1	RES 21.5K 1%	05524	CMF-50-2
A1 R141	1810-0037	3	1	NETWORK-RES DIP	02483	761-3-R1K
A1 R200	0698-4486	3	1	RES 24.9K 1%	05524	CMF-55-1
A1 R201	0757-0460	1	1	RES 61.9K 1%	05524	CMF-55-1
A1 R202	0698-7205	0	1	RES 51.1 1% .05W	05524	CMF-50-2
A1 R203	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R204	0757-0416	7	1	RES 511 1% .125W	05524	CMF-55-1
A1 R205	0757-0394	0	1	RES 51.1 1%	05524	CMF-55-1
A1 R206	0698-6324	2	1	RES 187 1% .125W	05524	CMF-55-1
A1 R207	0757-0410	1	1	RES 301 1% .125W	05524	CMF-55-1
A1 R208	0698-3700	2	1	RES 715 1% .125W	05524	CMF-55-1
A1 R209	0757-0403	2	1	RES 121 1% .125W	05524	CMF-55-1
A1 R210	0698-3446	3	1	RES 383 1% .125W	05524	CMF-55-1
A1 R211	0698-3441	8	1	RES 215 1% .125W	05524	CMF-55-1
A1 R212	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R214	0698-3160	8	1	RES 31.6K 1%	05524	CMF-55-1
A1 R220	0698-4486	3	1	RES 24.9K 1%	05524	CMF-55-1
A1 R221	0757-0460	1	1	RES 61.9K 1%	05524	CMF-55-1
A1 R222	0698-7205	0	1	RES 51.1 1% .05W	05524	CMF-50-2
A1 R223	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R224	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R225	0698-3441	8	1	RES 215 1% .125W	05524	CMF-55-1
A1 R226	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R229	0698-3160	8	1	RES 31.6K 1%	05524	CMF-55-1
A1 R240	0698-4486	3	1	RES 24.9K 1%	05524	CMF-55-1
A1 R241	0757-0460	1	1	RES 61.9K 1%	05524	CMF-55-1
A1 R242	0698-7205	0	1	RES 51.1 1% .05W	05524	CMF-50-2
A1 R243	0757-0394	0		RES 51.1 1%	05524	CMF-55-1
A1 R244	0698-3441	8	1	RES 215 1% .125W	05524	CMF-55-1
A1 R245	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R249	0698-3160	8	1	RES 31.6K 1%	05524	CMF-55-1
A1 R280	0698-3442	9	1	RES 237 1% .125W	05524	CMF-55-1
A1 R281	0698-4404	5	1	RES 105 1% .125W	05524	CMF-55-1
A1 R282	0757-1094	9	1	RES 1.47K 1%	05524	CMF-55-1
A1 R283	0698-4460	3	1	RES 649 1% .125W	05524	CMF-55-1
A1 R284	0757-0394	0	1	RES 51.1 1%	05524	CMF-55-1
A1 R285	0698-4014	3	1	RES 787 1% .125W	05524	CMF-55-1
A1 R286	0757-0803	6	1	RES 182 1% .5W	05524	CMF-65-2
A1 R287	0757-0803	6	1	RES 182 1% .5W	05524	CMF-65-2
A1 R288	0757-0394	0	1	RES 51.1 1%	05524	CMF-55-1
A1 R289	0757-0499	6	1	RES 27.4 1% .25W	05524	CMF-60-1, T-1
A1 R290	0757-1000	7	1	RES 51.1 1% .5W	05524	CMF-65-2
A1 R300	0757-0428	1	1	RES 1.62K 1%	05524	CMF-55-1
A1 R301	0757-0428	1	1	RES 1.62K 1%	05524	CMF-55-1
A1 R302	1810-1091	1	1	NETWORK-RES SIP	05524	MSP08A01
A1 R304	0698-7227	6	1	RES 422 1% .05W	05524	CMF-50-2
A1 R305	0698-7219	6	1	RES 196 1% .05W	05524	CMF-50-2
A1 R306	0698-7212	9	1	RES 100 1% .05W	05524	CMF-50-2
A1 R307	1810-0371	8	1	NETWORK-RES SIP	02483	750-81
A1 R308	1810-1091	1	1	NETWORK-RES SIP	05524	MSP08A01
A1 R309	1810-0205	7	1	NETWORK-RES SIP	02483	750-81

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R310	0698-7188	8	1	RES 10 1% .05W	05524	CMF-50-2
A1 R311	0698-3427	0	1	RES 13.3 1%	05524	CMF-55-1
A1 R312	0698-7212	9	1	RES 100 1% .05W	05524	CMF-50-2

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R414	0698-3226	7	1	RES 6.49K 1%	05524	CMF-55-1
A1 R415	0698-7200	5	1	RES 31.6 1% .05W	05524	CMF-50-2
A1 R416	2100-3659	7	1	RES-TRMR 20K 10%	04568	67WR
A1 R418	2100-0558	9	1	RES-TRMR 20K 10%	03744	3386P-Y46-203
A1 R419	0698-3428	1	1	RES 14.7 1%	05524	CMF-55-1
A1 R420	0698-3428	1	1	RES 14.7 1%	05524	CMF-55-1
A1 R421	0698-7221	0		RES 237 1% .05W	05524	CMF-50-2
A1 R422	0757-0438	3	1	RES 5.11K 1%	05524	CMF-55-1
A1 R423	0698-4467	0		RES 1.05K 1%	05524	CMF-55-1
A1 R424	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A1 R425	2100-3091	1	1	RES-TRMR 2K 10%	04568	67WR
A1 R426	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A1 R427	0698-4467	0		RES 1.05K 1%	05524	CMF-55-1
A1 R429	0698-7202	7	1	RES 38.3 1% .05W	05524	CMF-50-2

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R506	2100-3253	7	1	RES-TRMR 50K 10%	03744	3386P-Y46-503
A1 R507	0698-3452	1	1	RES 147K 1%	05524	CMF-55-1
A1 R508	0699-0644	9	1	RES 7.87 1%	01074	H8
A1 R509	0698-4421	6	1	RES 249 1% .125W	05524	CMF-55-1
A1 R510	0698-4488	5	1	RES 26.7K 1%	05524	CMF-55-1
A1 R511	0698-3359	7	1	RES 12.7K 1%	05524	CMF-55-1
A1 R512	0698-3359	7	1	RES 12.7K 1%	05524	CMF-55-1
A1 R513	0698-3498	5	1	RES 8.66K 1%	05524	CMF-55-1
A1 R514	0698-4460	3	1	RES 649 1% .125W	05524	CMF-55-1
A1 R515	2100-0568	1	1	RES-TRMR 100 10%	03744	3386P-Y46-101
A1 R516	0757-0443	0	1	RES 11K 1% .125W	05524	CMF-55-1
A1 R517	0757-0443	0	1	RES 11K 1% .125W	05524	CMF-55-1
A1 R518	0698-4386	2	1	RES 59 1% .125W	05524	CMF-55-1
A1 R519	0698-4386	2	1	RES 59 1% .125W	05524	CMF-55-1
A1 R520	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A1 R521	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A1 R522	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A1 R523	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A1 R524	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R525	0757-0283	6	1	RES 2K 1% .125W	05524	CMF-55-1
A1 R526	0757-0283	6	1	RES 2K 1% .125W	05524	CMF-55-1
A1 R527	0757-0401	0	1	RES 100 1% .125W	05524	CMF-55-1
A1 R528	0698-3495	2	1	RES 866 1% .125W	05524	CMF-55-1
A1 R529	0698-3495	2	1	RES 866 1% .125W	05524	CMF-55-1
A1 R530	0757-1022	3	1	RES 1.78K 1%	05524	CMF-60-1, T-1
A1 R531	0757-1022	3	1	RES 1.78K 1%	05524	CMF-60-1, T-1
A1 R532	0757-0751	3	1	RES 7.5K 1% .25W	05524	CMF-60-1, T-1
A1 R533	0698-3429	2	1	RES 19.6 1%	05524	CMF-55-1
A1 R534	0698-4358	8	1	RES 14 1% .125W	05524	CMF-55-1
A1 R535	2100-3211	7	1	RES-TRMR 1K 10%	03744	3386P-Y46-102

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 R536	0698-7220	9	1	RES 215 1% .05W	05524	CMF-50-2
A1 R537	0698-4358	8	1	RES 14 1% .125W	05524	CMF-55-1
A1 R538	0698-3429	2	1	RES 19.6 1%	05524	CMF-55-1
A1 R539	0698-8819	4	1	RES 3.83 1%	05524	CMF-55-1
A1 R540	0698-8819	4	1	RES 3.83 1%	05524	CMF-55-1
A1 R541	0698-3495	2	1	RES 866 1% .125W	05524	CMF-55-1
A1 R542	0698-3495	2	1	RES 866 1% .125W	05524	CMF-55-1
A1 R543	0757-0346	2	1	RES 10 1% .125W	05524	CMF-55-1
A1 R544	0757-0346	2	1	RES 10 1% .125W	05524	CMF-55-1
A1 R545	0757-0346	2	1	RES 10 1% .125W	05524	CMF-55-1
A1 R546	0757-0346	2	1	RES 10 1% .125W	05524	CMF-55-1
A1 R547	0766-0025	3	1	RES 101 2% 3W MO	12482	FP-3
A1 R548	0766-0025	3	1	RES 101 2% 3W MO	12482	FP-3
A1 R549	0757-0818	3	1	RES 825 1% .5W	05524	CMF-65-2
A1 R550	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A1 R551	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A1 R552	0757-0346	2	1	RES 10 1% .125W	05524	CMF-55-1
A1 R553	0757-0346	2	1	RES 10 1% .125W	05524	CMF-55-1
A1 R554	0757-0460	1	1	RES 61.9K 1%	05524	CMF-55-1
A1 R555	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A1 R556	0757-0290	5	1	RES 6.19K 1%	05524	CMF-55-1
A1 R557	1810-0279	5	1	NETWORK-RES SIP	05524	MSP10A01
A1 R560	0757-0384	8	1	RES 20 1% .125W	05524	CMF-55-1
A1 R562	0757-0399	5	1	RES 82.5 1%	05524	CMF-55-1
A1 R563	0757-0399	5	1	RES 82.5 1%	05524	CMF-55-1
A1 S1	3101-2956	8	1	SW-PB DPDT	05912	104-02-01003
A1 TP1	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP2	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP3	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP4	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 TP5	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP6	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP9	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP10	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP11	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 TP12	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A1 U1	1826-0315	3	1	IC 348	03406	LM348N
A1 U2	1826-0315	3	1	IC 348	03406	LM348N
A1 U3	1826-0393	7	1	IC LM317T	03406	LM317T
A1 U4	1826-0527	9	1	IC LM337T	03406	LM337T
A1 U5	1826-0393	7	1	IC LM317T	03406	LM317T
A1 U6	1826-0527	9	1	IC LM337T	03406	LM337T
A1 U100	1820-1216	3	1	IC-SN74LS138N	01698	SN74LS138N
A1 U101	1820-1997	7	1	IC-SN74LS374N	03406	DM74LS374N
A1 U102	1826-0501	9	1	ANLG MUXR	02037	MC14053BCP
A1 U110	1826-0111	7	1	IC 1458	03799	CA1458T
A1 U130	1820-1546	2	1	ANLG MUXR	02037	MC14052BCL
A1 U131	1826-0476	7	1	ANLG SW TL601CP	01698	TL601CP
A1 U132	1826-0111	7	1	IC 1458	03799	CA1458T
A1 U140	1820-1112	8	1	IC-SN74LS74AN	01698	SN74LS74AN
A1 U141	1820-1112	8	1	IC-SN74LS74AN	01698	SN74LS74AN
A1 U142	1820-1491	6	1	IC-SN74LS367AN	01698	SN74LS367AN
A1 U200	1DD6-0002	5	1		28480	1DD6-0002
A1 U201	1820-2849	0	1	IC-MC10H131P	02037	MC10H131P
A1 U220	1DD6-0002	5	1		28480	1DD6-0002
A1 U240	1DD6-0002	5	1		28480	1DD6-0002
A1 U300	1820-1997	7	1	IC-SN74LS374N	03406	DM74LS374N
A1 U301	1826-0955	7	1	IC 1DB6	01876	1DB6
A1 U302	1826-0600	9	1	IC 074A	01698	TL074ACN
A1 U320	1826-0111	7	1	IC 1458	03799	CA1458T

Table A-3. Main Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A1 U400	1820-1546	2	1	ANLG MUXR	02037	MC14052BCL
A1 U401	1826-0923	9	1	IC 1DC7	01876	
A1 U500	1820-1997	7	1	IC-SN74LS374N	03406	DM74LS374N
A1 U501	1826-0635	0	1	IC OP-07C	02180	OP-07CP
A1 U502	1826-0635	0	1	IC OP-07C	02180	OP-07CP
A1 U503	1820-1198	0	1	IC-SN74LS03N	01698	SN74LS03N
A1 VR1	1902-0680	7	1	DIO-ZNR 1N827	02037	1N827
A1 VR320	1902-0680	7	1	DIO-ZNR 1N827	02037	1N827
A1 VR501	1902-0960	6	1	DIO-ZNR 12V 5%	02037	SZ30035-18RL
A1 VR502	1902-0960	6	1	DIO-ZNR 12V 5%	02037	SZ30035-18RL
A1 W2	8159-0005	0	1	RES 0 CWM	01339	L-2007-1
A1 W3	8159-0005	0	1	RES 0 CWM	01339	L-2007-1
A1 W4	8159-0005	0	1	RES 0 CWM	01339	L-2007-1
A1 W5	8159-0005	0	1	RES 0 CWM	01339	L-2007-1
A1 W8	08116-61605	0	1		28480	08116-61605
A1 W9	08116-61607	2	1		28480	08116-61607
A1 W10	08112-61608	9	1		28480	08112-61608
A1 W11	08112-61609	0	1		28480	08112-61609
A1 W12	8159-0005	0	1	RES 0 CWM	01339	L-2007-1
A1 W13	8159-0005	0	1	RES 0 CWM	01339	L-2007-1

Control Board

Table A-4. Control Board Parts List

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2	08112-66502	2	1	BD AY-CONTROL	28480	08112-66502
A2 C1	0160-6596	1	1	CAP 0.47uF 50 V	02010	SA305E474MAAH
A2 C2	0180-0116	1	1	CAP 6.8uF 35 V	04200	150D685X9035B2-DYS
A2 C3	0180-0116	1	1	CAP 6.8uF 35 V	04200	150D685X9035B2-DYS
A2 C4	0180-0374	3	1	CAP 10uF 20 V	04200	150D106X9020B2-DYS
A2 C5	0180-0374	3	1	CAP 10uF 20 V	04200	150D106X9020B2-DYS
A2 C6	0180-4129	4	1	CAP 1uF 35 V	04200	173D105X9035V
A2 C7	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C10	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C11	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C14	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C15	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C16	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C17	0180-4129	4	1	CAP 1uF 35 V	04200	173D105X9035V
A2 C20	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C21	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C24	0180-0376	5	1	CAP 0.47uF 35 V	04200	150D474X9035A2-DYS
A2 C25	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C26	0160-3718	3	1	CAP 0.047uF 250	05992	23547350
A2 C27	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C28	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C29	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C30	0160-3879	7	1	CAP 0.01uF 100 V	02010	SR201C103MAAH
A2 C31	0180-4129	4	1	CAP 1uF 35 V	04200	173D105X9035V
A2 C32	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C33	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C101	0160-4386	3	1	CAP 33pF 200 V	09939	RPE121-105C0G330J200V
A2 C102	0160-4389	6	1	CAP 100pF 200 V	02010	SR202A101JAAH
A2 C103	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C104	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11

Table A-4. Control Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2 C105	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C106	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C107	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C108	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C109	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C110	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 C111	0160-5746	1	1	CAP 0.1uF 50 V	06121	B37987-T5104-M11
A2 CR1	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR2	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR3	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR4	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR5	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR6	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR7	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 CR8	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A2 J4	1251-3119	2	1	CONN-POST-TP-HDR	04726	3428-2002
A2 J5	1251-3119	2	1	CONN-POST-TP-HDR	04726	3428-2002
A2 L100	9170-0029	3	1	CORE-SHLD BEAD	04822	57-3452
A2 P1	1258-0124	7	1	SHUNT-PROGRAMMAB	05518	8136-475G1
A2 Q1	1853-0569	6	1	XSTR PNP SI	02037	
A2 Q2	1854-0472	2	1	XSTR NPN SI DARL	02037	MPS-A14
A2 Q3	1854-0472	2	1	XSTR NPN SI DARL	02037	MPS-A14
A2 Q100	1853-0563	0	1	XSTR PNP SI	02037	2N3906(SEL)
A2 Q101	1854-1028	6	1	XSTR NPN SI	02037	2N3904
A2 R1	1810-0277	3	1	NETWORK-RES SIP	05524	MSP10A01
A2 R2	0698-3153	9	1	RES 3.83K 1%	05524	CCF-55-1, T-1
A2 R3	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R4	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R5	0757-0462	3	1	RES 75K 1% .125W	05524	CCF-55-1, T-1
A2 R6	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104

Table A-4. Control Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2 R7	0698-3153	9	1	RES 3.83K 1%	05524	CCF-55-1, T-1
A2 R8	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R9	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R10	0757-0462	3	1	RES 75K 1% .125W	05524	CCF-55-1, T-1
A2 R11	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R12	0698-3153	9	1	RES 3.83K 1%	05524	CCF-55-1, T-1
A2 R13	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R14	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R15	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R16	0698-4014	3	1	RES 787 1% .125W	05524	CCF-55-1, T-1
A2 R17	0757-0280	3	1	RES 1K 1% .125W	05524	CCF-55-1, T-1
A2 R18	0757-0280	3	1	RES 1K 1% .125W	05524	CCF-55-1, T-1
A2 R19	0698-4473	8	1	RES 8.06K 1%	05524	CCF-55-1, T-1
A2 R21	0698-4428	3	1	RES 1.69K 1%	05524	CCF-55-1, T-1
A2 R22	0698-4428	3	1	RES 1.69K 1%	05524	CCF-55-1, T-1
A2 R23	0757-1094	9	1	RES 1.47K 1%	05524	CCF-55-1, T-1
A2 R24	0757-1094	9	1	RES 1.47K 1%	05524	CCF-55-1, T-1
A2 R26	2100-3252	6	1	RES-TRMR 5K 10%	03744	3386P-Y46-502
A2 R27	2100-0554	5	1	RES-TRMR 500 10%	03744	3386P-Y46-501
A2 R28	2100-0554	5	1	RES-TRMR 500 10%	03744	3386P-Y46-501
A2 R29	0757-0440	7	1	RES 7.5K 1%	05524	CCF-55-1, T-1
A2 R30	0757-0441	8	1	RES 8.25K 1%	05524	CCF-55-1, T-1
A2 R31	0698-4422	7	1	RES 1.27K 1%	05524	CCF-55-1, T-1
A2 R32	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R33	0698-4514	8	1	RES 105K 1%	05524	CCF-55-1, T-1
A2 R34	1810-0470	8	1	NETWORK-RES DIP	02483	761-3-R2.2K
A2 R35	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R36	0698-4514	8	1	RES 105K 1%	05524	CCF-55-1, T-1
A2 R37	2100-0554	5	1	RES-TRMR 500 10%	03744	3386P-Y46-501
A2 R38	2100-0554	5	1	RES-TRMR 500 10%	03744	3386P-Y46-501

Table A-4. Control Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2 R39	0757-0462	3	1	RES 75K 1% .125W	05524	CCF-55-1, T-1
A2 R40	0698-6360	6	1	RES 10K .1%	05524	CMF-55-1, T-9
A2 R41	0698-6360	6	1	RES 10K .1%	05524	CMF-55-1, T-9
A2 R42	2100-3252	6	1	RES-TRMR 5K 10%	03744	3386P-Y46-502
A2 R43	0698-4481	8	1	RES 16.5K 1%	05524	CCF-55-1, T-1
A2 R44	0698-4433	0	1	RES 2.26K 1%	05524	CCF-55-1, T-1
A2 R45	0757-0442	9	1	RES 10K 1% .125W	05524	CCF-55-1, T-1
A2 R46	2100-0567	0	1	RES-TRMR 2K 10%	03744	3386P-Y46-202
A2 R47	0757-0277	8	1	RES 49.9 1%	05524	CCF-55-1, T-1
A2 R48	0757-0280	3	1	RES 1K 1% .125W	05524	CCF-55-1, T-1
A2 R49	0698-3452	1	1	RES 147K 1%	05524	CCF-55-1, T-1
A2 R50	2100-0554	5	1	RES-TRMR 500 10%	03744	3386P-Y46-501
A2 R51	0698-6324	2	1	RES 187 1% .125W	05524	CCF-55-1, T-1
A2 R52	0698-3444	1	1	RES 316 1% .125W	05524	CCF-55-1, T-1
A2 R53	0698-3153	9	1	RES 3.83K 1%	05524	CCF-55-1, T-1
A2 R55	0698-3153	9	1	RES 3.83K 1%	05524	CCF-55-1, T-1
A2 R56	0757-0462	3	1	RES 75K 1% .125W	05524	CCF-55-1, T-1
A2 R57	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R58	0757-0462	3	1	RES 75K 1% .125W	05524	CCF-55-1, T-1
A2 R59	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R60	0757-0462	3	1	RES 75K 1% .125W	05524	CCF-55-1, T-1
A2 R61	2100-3214	0	1	RES-TRMR 100K	03744	3386P-Y46-104
A2 R62	0757-0458	7	1	RES 51.1K 1%	05524	CCF-55-1, T-1
A2 R63	0757-0458	7	1	RES 51.1K 1%	05524	CCF-55-1, T-1
A2 R64	0757-0458	7	1	RES 51.1K 1%	05524	CCF-55-1, T-1
A2 R101	1810-0243	3	1	NETWORK-RES DIP	02483	761-3-R6.8K
A2 R102	1810-0205	7	1	NETWORK-RES SIP	02483	750-81
A2 R103	1810-0206	8	1	NETWORK-RES SIP	02483	750-81
A2 R104	1810-0203	5	1	NETWORK-RES SIP	02483	750-81
A2 R105	1810-0203	5	1	NETWORK-RES SIP	02483	750-81

Table A-4. Control Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2 R106	1810-0203	5	1	NETWORK-RES SIP	02483	750-81
A2 R107	0698-4425	0	1	RES 1.54K 1%	05524	CCF-55-1, T-1
A2 R108	0698-4425	0	1	RES 1.54K 1%	05524	CCF-55-1, T-1
A2 R109	0757-0280	3	1	RES 1K 1% .125W	05524	CCF-55-1, T-1
A2 R110	0698-3441	8	1	RES 215 1% .125W	05524	CCF-55-1, T-1
A2 R111	0757-0280	3	1	RES 1K 1% .125W	05524	CCF-55-1, T-1
A2 TP1	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP2	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP3	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP4	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP5	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP6	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP7	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP8	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP9	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP10	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP11	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP12	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 TP13	0360-2264	6	1	TERMINAL-TEST PO	10358	1095D
A2 U1	1820-1216	3	1	IC-SN74LS138N	01698	SN74LS138N
A2 U2	1820-1730	6	1	IC-SN74LS273N	01698	SN74LS273N
A2 U3	1826-0821	6	1	ANLG SW	03285	AD7512DIJN
A2 U4	1826-0857	8	1	D/A 10-BIT	03285	AD7522LN
A2 U5	1826-0857	8	1	D/A 10-BIT	03285	AD7522LN
A2 U6	1826-0857	8	1	D/A 10-BIT	03285	AD7522LN
A2 U7	1826-0547	3	1	IC 072A	01698	TL072ACP
A2 U8	1826-0547	3	1	IC 072A	01698	TL072ACP
A2 U9	1826-0276	5	1	IC MC78L05ACP	02037	MC78L05ACP
A2 U10	1826-0111	7	1	IC 1458	03799	CA1458T
A2 U11	1820-1546	2	1	ANLG MUXR	02037	MC14052BCL

Table A-4. Control Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2 U12	1826-0857	8	1	D/A 10-BIT	03285	AD7522LN
[illegible]	1826-0857	8	1	D/A 10-BIT	03285	AD7522LN

Table A-4. Control Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A2 VR1	1902-0786	4	1	DIO-ZNR 1N937	02688	

Microprocessor Board

Table A-5. Microprocessor Board Parts List

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A3	08116-66535	0	1	BD AY MICROPRCR	28480	08116-66535
A3 BT1	1420-0273	2	1	BAT 3V	08709	BR-2/3AT2P
A3 C1	0160-4493	3	1	CAP 27pF 200 V	06352	FD12C0G2D270J
A3 C2	0160-4493	3	1	CAP 27pF 200 V	06352	FD12C0G2D270J
A3 C3	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH
A3 C4	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C5	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C6	0180-0229	7	1	CAP 33uF 10 V	04200	510D336X9010R2-DYS
A3 C7	0180-2207	5	1	CAP 100uF 10 V	04200	150D107X9010R2-DYS
A3 C8	0180-0229	7	1	CAP 33uF 10 V	04200	510D336X9010R2-DYS
A3 C9	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C10	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C11	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C12	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C13	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C14	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C15	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C16	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C17	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C18	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C19	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C20	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C21	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C22	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C23	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C24	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C25	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C26	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C27	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C28	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C29	0160-3877	5	1	CAP 100pF 200 V	02010	SR202C101MAAH
A3 C30	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121

Table A-5. Microprocessor Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A3 C31	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C32	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C33	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C34	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C35	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C36	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 C37	0160-6623	5	1	CAP 0.1uF 50 V	02010	SA115C104MAAH06121
A3 CR1	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A3 CR2	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A3 CR3	1901-1098	1	1	DIO-1N4150	04486	
A3 CR4	1901-1098	1	1	DIO-1N4150	04486	
A3 CR5	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A3 CR6	1901-0535	9	1	DIO- SCHOTTKY SM	02062	50825511
A3 J1	1251-8980	5	1	CONN-POST-TP-HDR	04726	3432-5202
A3 J2	1252-1979	0	1	CONN-POST-TP-HDR	04726	3627-5202
A3 J3	1251-3167	0	1	CONN-POST-TP-BDY	03418	09-50-3041
A3 J4	1251-4670	2	1	CONN-POST-TP-HDR	02946	68000-603
A3 J5	1251-4672	4	1	CONN-POST-TP-HDR	02946	68000-610
A3 MP1	1400-0824	7	1	STRAP-CABLE	04225	TY-23M
A3 Q1	1853-0281	9	1	XSTR PNP 2N2907A	02037	2N2907A
A3 R1	1810-0280	8	1	NETWORK-RES SIP	05524	MSP10A01
A3 R2	0698-8812	7	1	RES 1 1% .125W	05524	CMF-55-1
A3 R3	1810-0277	3	1	NETWORK-RES SIP	05524	MSP10A01
A3 R4	1810-0338	7	1	NETWORK-RES DIP	02483	761-3-R100
A3 R6	0698-3446	3	1	RES 383 1% .125W	05524	CMF-55-1
A3 R9	0757-0465	6	1	RES 100K 1%	05524	CMF-55-1
A3 R10	1810-0037	3	1	NETWORK-RES DIP	02483	761-3-R1K
A3 R11	1810-0503	8	1	NETWORK-RES DIP	02483	761-3-R3.3K
A3 R12	0757-0449	6	1	RES 20K 1% .125W	05524	CMF-55-1
A3 R13	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A3 R14	1810-0330	9	1	NETWORK-RES DIP	02483	761-3-R470 OHMS
A3 R15	1810-0280	8	1	NETWORK-RES SIP	05524	MSP10A01
A3 R16	1810-0280	8	1	NETWORK-RES SIP	05524	MSP10A01

Table A-5. Microprocessor Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A3 R17	0698-8812	7	1	RES 1 1% .125W	05524	CMF-55-1
A3 R19	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A3 R20	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A3 R21	0698-3162	0	1	RES 46.4K 1%	05524	CMF-55-1
A3 R22	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A3 R24	0757-0280	3	1	RES 1K 1% .125W	05524	CMF-55-1
A3 R25	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A3 R26	0757-0442	9	1	RES 10K 1% .125W	05524	CMF-55-1
A3 R27	0757-0279	0	1	RES 3.16K 1%	05524	CMF-55-1
A3 U1	1820-2099	2	1	IC-6802	02037	MC6802P
A3 U2	1820-2075	4	1	IC-SN74LS245N	01698	SN74LS245N
A3 U3	1820-2024	3	1	IC-SN74LS244N	01698	SN74LS244N
A3 U4	1820-2024	3	1	IC-SN74LS244N	01698	SN74LS244N
A3 U10	1LJ6-0001	7	1		28480	1LJ6-0001
A3 U12	1820-1216	3	1	IC-SN74LS138N	01698	SN74LS138N
A3 U13	1820-1216	3	1	IC-SN74LS138N	01698	SN74LS138N
A3 U14	1820-1216	3	1	IC-SN74LS138N	01698	SN74LS138N
A3 U15	1820-1414	3	1	IC-SN74LS12N	01698	SN74LS12N
A3 U16	1820-1997	7	1	IC-SN74LS374N	03406	DM74LS374N
A3 U17	1820-1216	3	1	IC-SN74LS138N	01698	SN74LS138N
A3 U19	1820-1298	1	1	IC-SN74LS251N	01698	SN74LS251N
A3 U20	1820-1426	7	1	IC-SN74LS145N	01698	SN74LS145N
A3 U21	1820-2024	3	1	IC-SN74LS244N	01698	SN74LS244N
A3 U22	1820-2132	4	1	IC-INTERFACE	03799	ICM7218A
A3 U23	1820-1997	7	1	IC-SN74LS374N	03406	DM74LS374N
A3 U25	1820-2075	4	1	IC-SN74LS245N	01698	SN74LS245N
A3 U26	1820-2024	3	1	IC-SN74LS244N	01698	SN74LS244N
A3 U27	1826-0161	7	1	IC 324	03406	LM324N
A3 U29	1858-0053	3	1	XSTR ARY 14P-DIP	02037	
A3 U30	1820-2219	8	1	IC-68488	02037	MC68488P
A3 U31	1820-2058	3	1	IC-INTERFACE	02037	MC3448AL

Table A-5. Microprocessor Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A3 U32	1820-2058	3	1	IC-INTERFACE	02037	MC3448AL
A3 U33	1820-2058	3	1	IC-INTERFACE	02037	MC3448AL
A3 U34	1820-2058	3	1	IC-INTERFACE	02037	MC3448AL
A3 U35	1820-1416	5	1	IC-SN74LS14N	01698	SN74LS14N
A3 U36	1820-1640	7	1	IC-SN74LS366AN	01698	SN74LS366AN
A3 U37	1820-1195	7	1	IC-SN74LS175N	01698	SN74LS175N
A3 U39	1820-1197	9	1	IC-SN74LS00N	01698	SN74LS00N
A3 U40	08112-13728	2	1		28480	08112-13728
A3 W3	8159-0005	0	1	RES 0 CWM	01339	L-2007-1
A3 W4	5180-2469	0	1	CABLE RBN	28480	5180-2469
A3 Y1	0410-0762	2	1	XTAL 4.000 MHZ	07492	

Keyboard

Table A-6. Keyboard Parts List

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A4	08112-66504	4	1	BD AY-KEY	28480	08112-66504
A4 DS1	1990-0665	3	1	LED-LMP	01542	
A4 DS2	1990-0665	3	1	LED-LMP	01542	
A4 DS3	1990-0665	3	1	LED-LMP	01542	
A4 DS4	1990-0665	3	1	LED-LMP	01542	
A4 DS5	1990-0665	3	1	LED-LMP	01542	
A4 DS6	1990-0665	3	1	LED-LMP	01542	
A4 DS7	1990-0665	3	1	LED-LMP	01542	
A4 DS8	1990-0665	3	1	LED-LMP	01542	
A4 DS9	1990-0665	3	1	LED-LMP	01542	
A4 DS10	1990-0665	3	1	LED-LMP	01542	
A4 DS11	1990-0665	3	1	LED-LMP	01542	
A4 DS12	1990-0665	3	1	LED-LMP	01542	
A4 DS13	1990-0665	3	1	LED-LMP	01542	
A4 DS14	1990-0665	3	1	LED-LMP	01542	
A4 DS15	1990-0665	3	1	LED-LMP	01542	
A4 DS16	1990-0665	3	1	LED-LMP	01542	
A4 J1	1251-7409	1	1	CONN-POST-TP-SKT	03418	22-14-2124
A4 J2	1251-6255	3	1	CONN-POST-TP-SKT	03418	22-14-2204
A4 MP1	5041-0309	5	1		28480	5041-0309
A4 MP2	5041-0309	5	1		28480	5041-0309
A4 MP3	5041-0309	5	1		28480	5041-0309
A4 MP4	5041-0351	7	1		28480	5041-0351
A4 MP5	5041-0351	7	1		28480	5041-0351
A4 MP6	5041-0351	7	1		28480	5041-0351
A4 MP7	5041-0726	0	1		28480	5041-0726
A4 MP8	5041-0285	6	1		28480	5041-0285
A4 MP9	5041-0285	6	1		28480	5041-0285
A4 MP10	5041-0276	5	1		28480	5041-0276
A4 MP11	5041-0276	5	1		28480	5041-0276

Table A-6. Keyboard Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A4 MP12	5041-0351	7	1		28480	5041-0351
A4 MP13	5041-0351	7	1		28480	5041-0351
A4 MP14	5041-0516	6	1		28480	5041-0516
A4 MP15	5041-0285	6	1		28480	5041-0285
A4 MP16	5041-0285	6	1		28480	5041-0285
A4 MP17	5041-0351	7	1		28480	5041-0351
A4 MP18	5041-0351	7	1		28480	5041-0351
A4 MP19	5041-0342	6	1		28480	5041-0342
A4 MP20	5041-0285	6	1		28480	5041-0285
A4 MP21	5041-0285	6	1		28480	5041-0285
A4 MP22	5041-0285	6	1		28480	5041-0285
A4 MP23	5041-0285	6	1		28480	5041-0285
A4 S1	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S2	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S3	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S4	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S5	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S6	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436

Table A-6. Keyboard Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A4 S19	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S20	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S21	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S22	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 S23	5060-9436	7	1	SW-PB SPST NO	04486	5560-9436
A4 W1	5180-2402	7	1		28480	5180-2402

Display Board

Table A-7. Display Board Parts List

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A5	08112-66505	5	1	BD AY-DISPLAY	28480	08112-66505
A5 DS1	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS2	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS3	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS4	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS5	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS6	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS7	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS8	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS9	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS10	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS11	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS12	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS13	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS14	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS15	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS16	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS17	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS18	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS19	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS20	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS21	1990-0806	4	1	LED-LT BAR	01542	HLMP-2300(SELECTED)
A5 DS22	1990-0805	3	1	LED-LT BAR	01542	HLMP-2350(SELECTED)
A5 DS23	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS24	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS25	1990-0486	6	1	LED-LMP	01542	HLMP-1301
A5 DS26	1990-0846	2	1	DISPLAY-NUM-SEG	01542	
A5 DS27	1990-0846	2		DISPLAY-NUM-SEG	01542	
A5 DS28	1990-0846	2		DISPLAY-NUM-SEG	01542	
A5 DS29	1990-0846	2		DISPLAY-NUM-SEG	01542	

Table A-7. Display Board Parts List (continued)

Reference	HP Part #	CD	Qty	Description	Manuf'r	Part #
A5 J1	1251-7430	8	1	CONN-POST-TP-HDR	08839	5912575
A5 J2	1251-7431	9	1	CONN-POST-TP-HDR	08839	5920575
A5 S1	3101-2529	1	1	SW-RKR DPDT	08360	326.2-01
A5 S2	3101-2529	1	1	SW-RKR DPDT	08360	326.2-01
A5 S3	3101-2529	1	1	SW-RKR DPDT	08360	326.2-01

B

Backdating

Backdating information is only required for instruments with a serial number *lower* than that shown on the front page of this manual i.e. When you have an older instrument than those covered in this manual.

Introduction

This appendix contains backdating information to adapt this manual for instruments with a serial number *lower* than that shown on the title page. Only the digits following the letter are important when deciding which changes apply to your instrument. If your instrument has a higher serial number than that shown on the title page, refer to Appendix C *Updating* for any possible changes instead.

To adapt this manual for an earlier instrument, look up your serial number in Table B-1 and implement the changes from the **latest** back to the earliest change which applies to your instrument. For example, if the serial number of your instrument is 2633G04470, implement changes in order from Change 57 to 36. Change 35 and earlier would have been incorporated during manufacture.

Where changes to components occur, modify the appropriate schematic and component layout accordingly.

Note

- Some components may have been changed more than once during production of the HP 8112A. Therefore Hewlett-Packard suggests you make the modifications to the manual in pencil as you work through the changes for your instrument.
- Some components may have been changed individually, or as part of an associated group, to improve performance etc. In these cases Hewlett-Packard suggests you note the difference between the build standard of your instrument and current models, but do not implement what would in effect, be a retrograde change.

Table B-1. Backdating Changes

Instrument Serial No.	Implement Changes From 58 to:
G00xxx to G00119	1
G00120 to G00159	2
G00160 to G00189	3
G00190 to G00219	4
G00220 to G00354	5
G00355 to G00373	6
G00374 to G00404	7
G00405 to G00554	8
G00555 to G00579	9
G00580 to G00604	10
G00605 to G00704	11
G00705 to G00729	12
G00730 to G01180	13
G01181 to G01580	14
G01581 to G01630	15
G01631 to G01855	16
G01856 to G01930	17
G01931 to G02105	18
G02106 to G02180	19
G02181 to G02255	20
G02256 to G02330	21
G02331 to G02380	22
G02381 to G02555	23
G02556 to G02630	24
G02631 to G02655	25
G02656 to G03005	26
G03006 to G03055	27
G03056 to G03230	28
G03231 to G03255	29
G03256 to G03480	30
G03481 to G04105	31
G04106 to G04230	32
G04231 to G04280	33
G04281 to G04460	34
G04461 to G04530	35
G04531 to G04605	36
G04606 to G04730	37
G04731 to G04830	38
G04831 to G04880	39
G04881 to G05780	40
G05781 to G05830	41
G05831 to G06180	42
G06181 to G06580	43
G06581 to G06930	44
G06931 to G07230	45
G07231 to G07280	46
G07281 to G07380	47
G07381 to G07680	48
G07681 to G07780	49
G07781 to G07980	50
G07981 to G08630	51
G08631 to G08780	52
G08781 to G08949	53
G08950 to G09030	54
G09031 to G09130	55
G09131 to G09505	56
G09506 to G09530	57
G09531 to G10005	58

Change 1

Component value change to improve vernier adjustment.

For instruments with serial numbers 2136G00120 and lower, make the following change to the parts-list for the Main Board assembly A1 in Appendix B, Table A-3.

	Reference	Description	HP Part #
A1 08112-66501	R438	RESISTOR	0698-4425

Change 2

For instruments with serial numbers 2136G00160 and lower, make the following changes to the appropriate parts-lists:

Instrument case

In Appendix A, Table A-2 *modify*:

	Reference	Description	HP Part #
A0 08112	MP2	SHAFT, POWER SW	08112-43701
	MP8	FRAME REAR	5020-8814
	MP9	PANEL REAR	08112-60253

Display Board

In Appendix A, Table A-7 *modify*:

	Reference	Description	HP Part #
A5 08112-66505	DS26	DISPLAY NUM	1990-0649
	DS27	DISPLAY NUM	1990-0531
	DS28	DISPLAY NUM	1990-0531
	DS29	DISPLAY NUM	1990-0531

HP-IB Board

In Appendix A, Table A-8 *modify*:

	Reference	Description	HP Part #
A6 08116-66506	S1	SW AY-SL	3101-2097

Change 3

Minor mechanical improvements were made.

For instruments with serial numbers 2136G00190 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	MP200	HT-SINK	1205-0018

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66523	MP1	CLAMP CABLE	1400-0304
		RIVET 0.125	0361-0140

Change 4

Several component changes were made to improve pulse response in Linear and Fixed Transition Mode.

For instruments with serial numbers 2136G00219 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	C532	CAP 1 pF 200 V	0160-4380
	C534	CAP 27 pF	0160-4393
	Q504	XSTR SI 2N4209	1853-0405
	R534	RES 16.9Ω 1%	0698-4363
	R537	RES 12.7Ω 1%	0698-4356
	R559	RES 30.1Ω 1%	0757-0388

Change 5

A faster IC was substituted to improve reset after power interruption.

For instruments with serial numbers 2136G00354 and lower, make the following changes to the appropriate parts-list:

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66523	U35	IC SN74LS04	1820-1199

Change 6

Component changes were made to improve slope stability.

For instruments with serial numbers 2136G00374 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	R437	RES 16.2Ω 1% .5	0698-7265

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	R325 to R329		

Change 7

This change was to clarify incorrect labelling on the ROM ICs. No change action is required, however do not order replacement ICs as detailed in the first table below. Use the correct numbers given in the second table.

Microprocessor Board

In Appendix A, Table A-5:

Faulty labels to disregard

	Reference	Description	HP Part #
A3 08116-66523	U5	ROM	08112-10001
	U6	ROM	08112-10002
	U7	ROM	08112-10003
	U8	ROM	08112-10004
	U9	ROM	08112-10005

In Appendix A, Table A-5:

Correct Part Numbers

	Reference	Description	HP Part #
A3 08116-66523	U5	ROM	08112-13701
	U6	ROM	08112-13702
	U7	ROM	08112-13703
	U8	ROM	08112-13704
	U9	ROM	08112-13705

Main Board

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	CR513	DIODE	
	CR514	DIODE	

Change 8

An extra test point and an isolator link were added to the microprocessor board to improve test facility.

For instruments with serial numbers 2136G00405 and lower, make the following changes to the appropriate parts-list:

Microprocessor Board

In Appendix A, Table A-5 *delete*:

	Reference	Description	HP Part #
A3 08116-66523	TP8	Test point	0360-0535
	W2	Wire jumper	8159-0005

Change 9

Two bus termination resistor networks were changed to reduce crosstalk.

For instruments with serial number 2136G00579 and lower, make the following changes to the appropriate parts-list:

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66523	R15	R-NETWORK 47 k	1810-0378
	R16	R-NETWORK 47 k	1810-0378

Change 10

Component value change to provide greater adjustment range on Width generator.

For instruments with serial number 2136G00605 and lower, make the following changes to the appropriate parts-list:

Control Board

In Appendix A, Table A-4 *modify*:

	Reference	Description	HP Part #
A2 08112-66502	R7	R-F 4.64 k| 0698-3155	

Change 11

For instruments with serial number 2136G00705 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	R317	R-F 2k	0757-0283

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	C541	C-F 0.01 μF	

Change 12

The performance of the rate ICs was improved. With introduction of new version, components and values were changed.

For instruments with serial number 2136G00730 and lower, make the following changes to the appropriate parts lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	R211	R-F 1k 1% .125W	0757-0280
	R225	R-F 1k 1% .125W	0757-0280
	R244	R-F 1k 1% .125W	0757-0280
	U200	IC TIMING SEL 2%	5180-2410
	U220	IC TIMING SEL 2%	5180-2410
	U240	IC TIMING SEL 2%	5180-2410

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	C204,205,224,225,244,246	C-F 0.47 μF	0160-0575
	CR200,201,220,221,240,241	DIODE	1901-1068
	R214,R229,R249	R-F 31.6 k 1%	0698-3160

In Appendix A, Table A-3 *add*:

	Reference	Description	HP Part #
A1 08112-66501	C203,223,243	C-F 0.1 μF	0160-0576
	R213,	R-F 10 k 1%	0757-0442
	R227,228,246,247	R-F 2.21 k	0757-0430

Control Board

In Appendix A, Table A-4 *modify*:

	Reference	Description	HP Part #
A2 08112-66502	R62*	R-F 51.1 k| 0757-0458	
	R64*	R-F 51.1 k| 0757-0458	
	VR2*	DIODE ZENER 4.3 V 1%	1902-0949
	VR4*	DIODE ZENER 4.3 V 1%	1902-0949

Microprocessor Board

In Appendix A, Table A-5 *add*:

	Reference	Description	HP Part #
A3 08116-66523	W1	Jumper	8159-0005

Change 13

Component changes to improve slope accuracy and prevent erroneous error message "E31"

For instruments with serial number 2136G00780 and lower, make the following changes to the appropriate parts lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	C305	C-F 1000 pf 2%	0140-0178
	R15	R-F 5.2 k 1% .125W	0698-8863

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	R30	R-F 200 Ω	0757-0407

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66523	U17	IC-SN74LS138	1820-1216

Change 14

Component changes were introduced to improve overshoot. New firmware was introduced with a new set of ROMS. If you have the old firmware installed, signature analysis readings for the ROM test (see *Trouble shooting* in Chapter 10.7) will be as detailed in Table B-2:

For instruments with serial number 2343G01130 and lower make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	C541	Capacitor 0.01 μF 100 V	0160-3879

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66501	C414	Capacitor	15 pF	0160-4385
	R100	Resistor network	7×10 k	1810-0206
	R556	Resistor	13.3 k 1%	0757-0289
	R557	Resistor network	9×10 k	1810-0280

Control Board

In Appendix A, Table A-4 *modify*:

	Reference	Description		HP Part #
A2 08112-66502	R7	Resistor	5.62 k	0757-2000
	R55		4.42 k	0698-4442

Microprocessor Board In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66523	U5	ROM 6	8112-13711
	U6	ROM 5	8112-13712
	U7	ROM 4	8112-13713
	U8	ROM 3	8112-13714
	U9	ROM 2	8112-13715

Table B-2.

Pin	U9 ROM2	U8 ROM3	U7 ROM4	U6 ROM5	U5 ROM6
9	U3H3	5U37	F90P	98HH	6855
10	274F	A0AH	U397	6AH5	UAC1
11	89CC	5U76	6U6P	99AU	9C5F
13	U630	P4A1	U1A3	OP4H	A375
14	4P70	9U82	7512	H4F6	0064
15	11UF	HOF4	C3AU	8FC2	22A3
16	A3CP	28P7	89P4	7HU1	F55F
17	4C7P	AH62	99C1	1P86	668A

Change 15

A ferrite bead was introduced around the base connector of Q400A, and the value of C535 altered, to improve pulse performance when ringing and fall times are excessive, as shown in Figure B-1.

For instruments with serial number 2343G01580 and lower make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3*delete*:

	Reference	Description		HP Part #
A1 08112-66501	C535	Capacitor	47 pF	0160-4387
	*C535	Capacitor	68 pF	0160-5737
	L513	Ferrite bead	Green	9170-0029

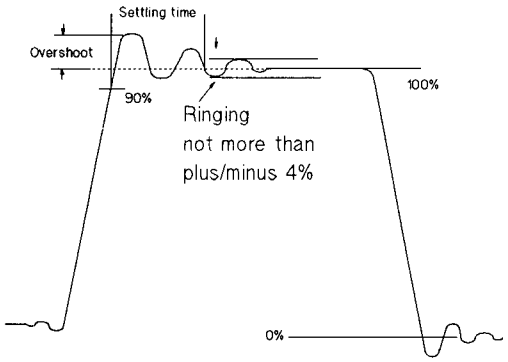


Figure B-1. Example output pulse

Change 16

Capacitor C415 was added between Pin 20 of connector J2 and ground to provide a cleaner signal at low period times. Other component value changes were to compensate for slight variations in dual transistor performance.

For instruments with serial number 2343G01630 and lower make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66501	R406	Resistor	1.62 k	0757-0428
	R408	Resistor	249Ω	0698-4421
	R421	Resistor	237Ω	0698-7221

In Appendix A, Table A-3 *add*:

	Reference	Description		HP Part #
A1 08112-66501	*R421	Resistor	147	0698-7216

In Appendix A, Table A-3 *delete*:

	Reference	Description		HP Part #
A1 08112-66501	C415	Capacitor	220 pF	0160-5731

Change 17

Component value changes were introduced to improve linearity.

For instruments with serial number 2343G01855 and lower make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66501	C240	Capacitor	10 pF	0160-3874
	R7	Resistor	4.87 k	0698-4444

In Appendix A, Table A-3 *delete*:

	Reference	Description		HP Part #
A1 08112-66501	*R7	Resistor	4.42 k	0698-4442

Change 18

Component value changes were introduced with a change in dual [illegible]

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66501	C535	Capacitor	68 pF	0160-5737
	Q400	Transistor	Dual PNP	1853-0075

In Appendix A, Table A-3 *add*:

	Reference	Description	HP Part #
A1 08112-66501	L513	Ferrite Bead	9170-0029

Change 19

There was a board revision involving component changes and substitution, caused by a changeover from 1k×4 RAM chips to 2k×8.

For instruments with serial number 2343G02105 and lower,

1. Make the following changes to the appropriate parts-lists:

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66523	U10	IC RAM 444C	1818-1330

In Appendix A, Table A-5 *delete*:

	Reference	Description	HP Part #
A3 08116-66523	R21		
	U38		

In Appendix A, Table A-5 *add*:

	Reference	Description	HP Part #
A3 08116-66523	U11	IC RAM 444C	1818-1330

2. Figure B-2 shows the location of the RAMs U10 and U11 on the microprocessor board 08116-65503. Modify Chapter 10.7, Figure 10.7-9 accordingly.

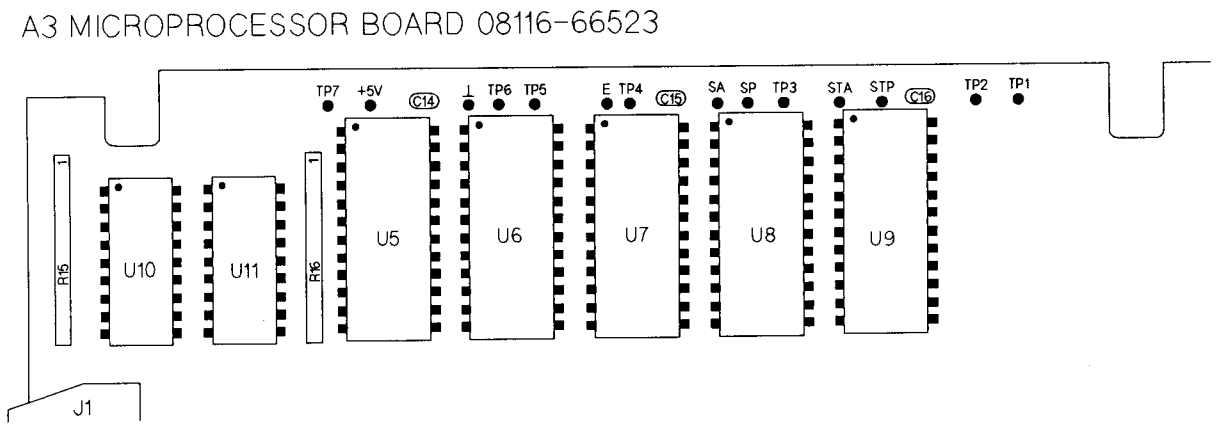


Figure B-2. 08116-66523: U10, U11 layout

3. Figure B-3 shows the RAM circuit on the microprocessor board 08116-65523. Modify Chapter 10.7, Figure 10.7-5 accordingly.

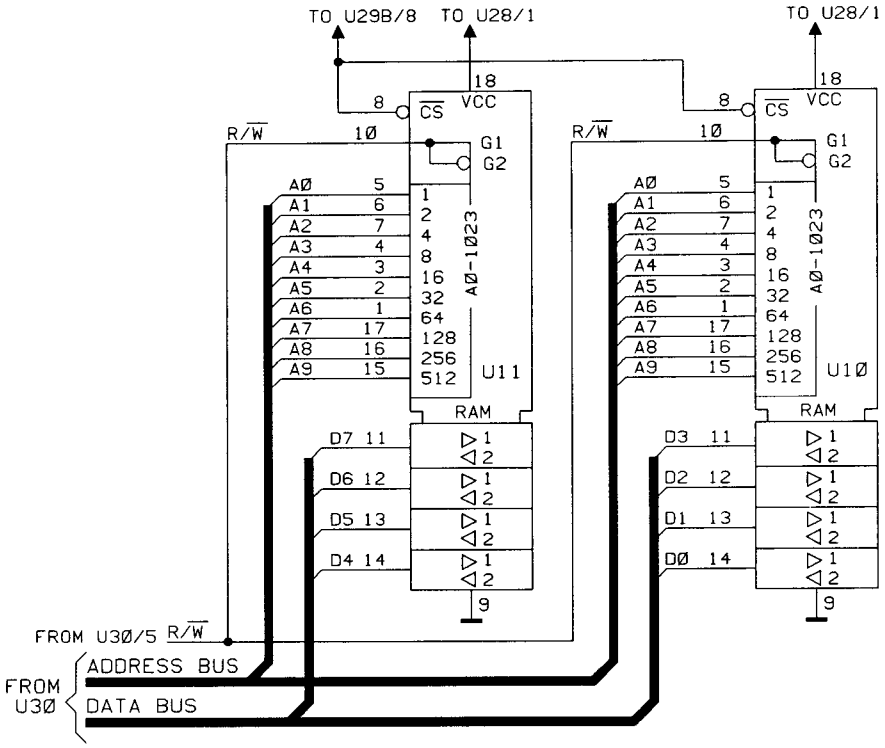


Figure B-3. 08116-66523: U10, U11 schematic

Change 20

Component value change to increase adjustment range and improve compatibility.

For instruments with serial number 2343G02180 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	R400	RES 15.4K 1%	0698-3540

Change 21

New part numbers were allocated to case components, caused by standardisation on metric screw threads.

Caution

If you are replacing any of the parts identified below, you should take care before ordering a replacement from the parts list in Appendix A of this manual. Any part containing a screw thread will require new **compatible** screws and the instrument case will then contain a mix of screw types!.

For instruments with serial number 2343G02255 and lower, make the following changes to the appropriate parts-lists:

Instrument

In Appendix A, Table A-2 *modify*:

	Reference	Description	HP Part #
A0 08112	MP4	PANEL SUB	08112-00202
	MP7	FRAME FRONT	5020-8813
	MP8	FRAME REAR	08112-21103
	MP12	SIDE STRUT 17 IN	5020-8831
	MP13	SIDE STRUT 17 IN	5020-8831
	MP17	COVER BOTTOM	08112-04158
	MP18	COVER TOP 31/2#M	08112-04101

Change 22

For instruments with serial number 2343G02330 and lower.

Changes in component sourcing required several changes to the parts lists. Because the changes did not affect the manual or the performance of the instrument, they are not detailed here.

Change 23

For instruments with serial number 2343G02380 and lower.

Changes in component sourcing required several changes to the parts lists. Because the changes did not affect the manual or the performance of the instrument, they are not detailed here.

Change 24

For instruments with serial number 2343G02555 and lower.

This change introduced ferrite beads (L514 and L515) on the base of Q400 and the collector of Q402 respectively. The change is associated with change 18 and was found to ensure more stable performance when the dual transistor type was changed.

Change 25

For instruments with serial number 2507G02630 and lower:

A new microprocessor board (08116-66533) was introduced which gave improved jitter and standard setting characteristics. See change 41 for more information.

Make the following changes to the appropriate parts-lists:

Instrument

In Appendix A, Table A-2 *modify*:

	Reference	Description	HP Part #
A0 08112	A3	BD AY-MICROPROCESSOR	08116-66523

Microprocessor Board

In Appendix A, Table A-5 *delete*:

	Reference	Description	HP Part #
A3 08116-66533	W5	Resistor zero Ω	8159-0005

Change 26

For instruments with serial number 2522G02655 and lower.

This change was a change in part number for fuse F1 caused by component obsolescence.

Change 27

Changed the value of C246 on the main board to suppress an intermittent and unwanted pulse in one of the width ranges.

For instruments with serial number 2522G03005 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	C246	Capacitor 0.047 μF	0160-0575

Change 28

Made R53 value selectable during manufacture and thus added an alternative (*) value to the parts list.

For instruments with serial number 2522G03055 and lower make the following changes to the appropriate parts-lists:

Control Board

In Appendix A, Table A-4 *delete*:

	Reference	Description	HP Part #
A2 08112-66502	*R53	Resistor 4.42 k	0698-4442

Change 29

Component value change improved LOL variation about HIL.

For instruments with serial number 2522G03230 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	R507	Resistor 178 k	0698-3243

Change 30

For instruments with serial number 2522G03269 and lower.

Introduced a new main board with changed board layout. This was caused by substitution for relay type that was no longer available.

Note

Board A1 08112-66501 rev E changed to rev F. Newer board type can be recognized by fuses F1 and F2 which are mounted in clips.

Change 31

Alternative component value selection, improved linearity of Period, Delay and Width adjustment.

For instruments with serial number 2522G03480 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66501	C200	Capacitor 12 pF	0160-4521

Change 32

New heat sink introduced by metrication. Components added to improve switch-on reset conditions.

For instruments with serial number 2522G04130 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66501	MP505,506, and MP508 to 513	HT-SINK SGL	1205-0329

For instruments with serial number 2522G04105 and lower, make the following changes to the appropriate parts-list:

Microprocessor Board

In Appendix A, Table A-5 *delete*:

	Reference	Description	HP Part #
A3 08116-66533	CR5		8159-0005
	Q2		
	R22,23		

Change 33

Board edge connectors were changed for improved type with ejector latches. These provided more secure fastening for the ribbon cable ends into the board connectors.

Instruments with serial number 2522G04230 and lower will have older type of connector fitted.

Change 34

For instruments with serial number 2522G04280 and lower, make the following changes to the appropriate parts-lists:

Instrument

Standardisation of rear frame assembly introduced new part number. Old part in Appendix A, Table A-2 was:

	Reference	Description	HP Part #
A0 08112	MP8	FRAME REAR	5021-5814

Note

This change was reversed by change 37 to provide improved screening. This means if your instrument pre-dates this change, implement Change 34 and ignore Change 37.

Main Board

Components on the main board and control board were allocated alternative values to improve pulse specification.

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66501	C200*	Capacitor	12 pF	0160-4521
	C220*	Capacitor	12 pF	0160-4521
	C240*	Capacitor	12 pF	0160-4521

Control Board

In Appendix A, Table A-4 *modify*:

	Reference	Description		HP Part #
A2 08112-66502	R53	Resistor	4.22 k	0698-3158
	R54	Resistor	4.42 k	0698-4442

In Appendix A, Table A-4 *delete*:

	Reference	Description		HP Part #
A2 08112-66502	R55	Resistor	4.02 k	0698-3558

Change 35

Introduction of new Main board assembly (08112-66511).

For instruments with serial number 2633G04460 and lower, make the following change to the appropriate parts-list:

Instrument

In Appendix A, Table A-2 *modify:*

	Reference	Description	HP Part #
A0 08112	A1	Board Ay Main	8112-66501

Change 36

Component value and/or type changes, made to improve adustment range.

For instruments with serial number 2633G04505 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	R302,R308	Resistor Network 680 Ω	1810-0332

For instruments with serial number 2633G04530 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	R317	Resistor 1.87 k	0698-4429

Change 37

For instruments with serial number 2633G04605 and lower, make the following changes to the appropriate parts-lists:

Instrument

Note

This change reverses change 34!. **Do not** reverse-implement this change. **Ignore it.** Information here is for the sake of completeness only.

Reversion to previous frame assembly. In Appendix A, Table A-2 *modify:*

	Reference	Description	HP Part #
A0 08112	MP8	FRAME REAR	5021-0512

Change 38

This change applied only to a special version of the HP 8112A, and therefore is not detailed here.

Change 39

Changes to part numbers on introduction of improved D/A converter chips.

For instruments with serial number 2633G04830 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	R411	Resistor 2.37 k	0698-7245

Control Board

In Appendix A, Table A-4 *modify*:

	Reference	Description	HP Part #
A2 08112-66502	U4,5,6 and U12,13,23	D/A Converter 10 bit	1826-0729

Change 40

This change introduced the HP 8116A sub-panel which has better RFI characteristics. No backdating action for earlier instruments is required.

Change 41

New microprocessor board A3 (08112-66534) was introduced with one 32k EPROM replacing old ROMs. Changes to circuit diagrams and trouble shooting signature analysis table(s) were involved in this change. Details of appropriate parts, drawings etc. for older style microprocessor boards are given here.

For instruments with serial number 2633G05780 and lower:

1. Make the following changes to the appropriate parts-lists and trouble shooting information:

Instrument

In Appendix A, Table A-3 and Table A-5: *modify*

	Reference	Description	HP Part #
A0 08112	A3	BD AY-MICROPRCR	08112-66533

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08116-66533	BT1	BAT NI-CAD	1420-0251
	U10	RAM	1818-1768

In Appendix A, Table A-5 *delete*:

	Reference	Description	HP Part #
A3 08116-66533	CR6		
	R24		
	U40		
	W3		

In Appendix A, Table A-5 *add*:

	Reference	Description		HP Part #
A3 08116-66533	C14	CAP .1 μF CER	20%	0160-5746
	Q2	XSTR NPN 2N3904		1854-1028
	R7	RES 200 Ω .125 W	1%	0757-0407
	R8	RES 100K .125 W	1%	0757-0465
	R18	RES 1K .125 W	1%	0757-0280
	RT1	THMS 1K DIS		0837-0050
	U5	ROM 6		08112-13721
	U6	ROM 5		08112-13722
	U7	ROM 4		08112-13723
	U8	ROM 3		08112-13724
	U9	ROM 2		08112-13725
	U28	XSTR QUAD PNP		1858-0058
	W5	RES-ZERO OHMS		8159-0005
	U10	RAM		1818-1768
		SOCKET 24 PIN		1200-0541
		TEST POINT		0360-2264

2. Figure B-4 shows the location of the ROMs on microprocessor board 66533, modify Figure 10.7-9.

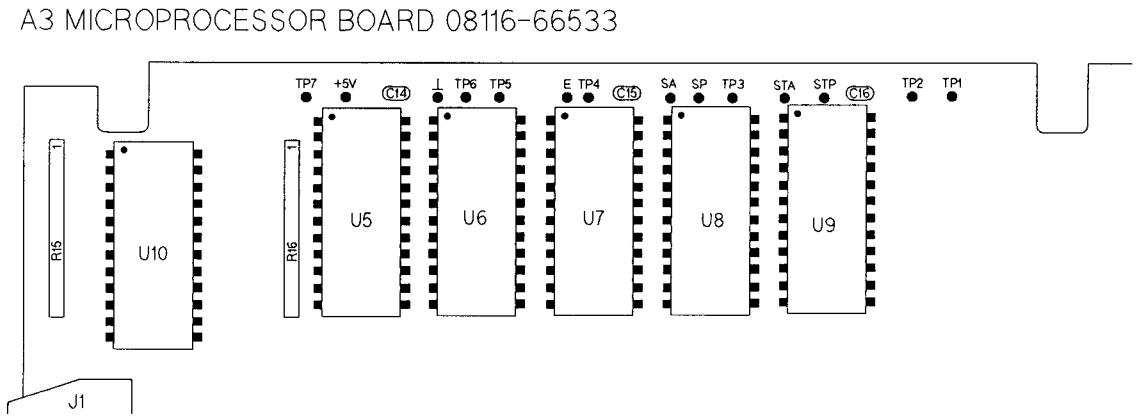


Figure B-4. 08116-66533: ROM layout

3. Figure B-5 shows the change to Figure 10.7-5 for enabling five individual ROMS.

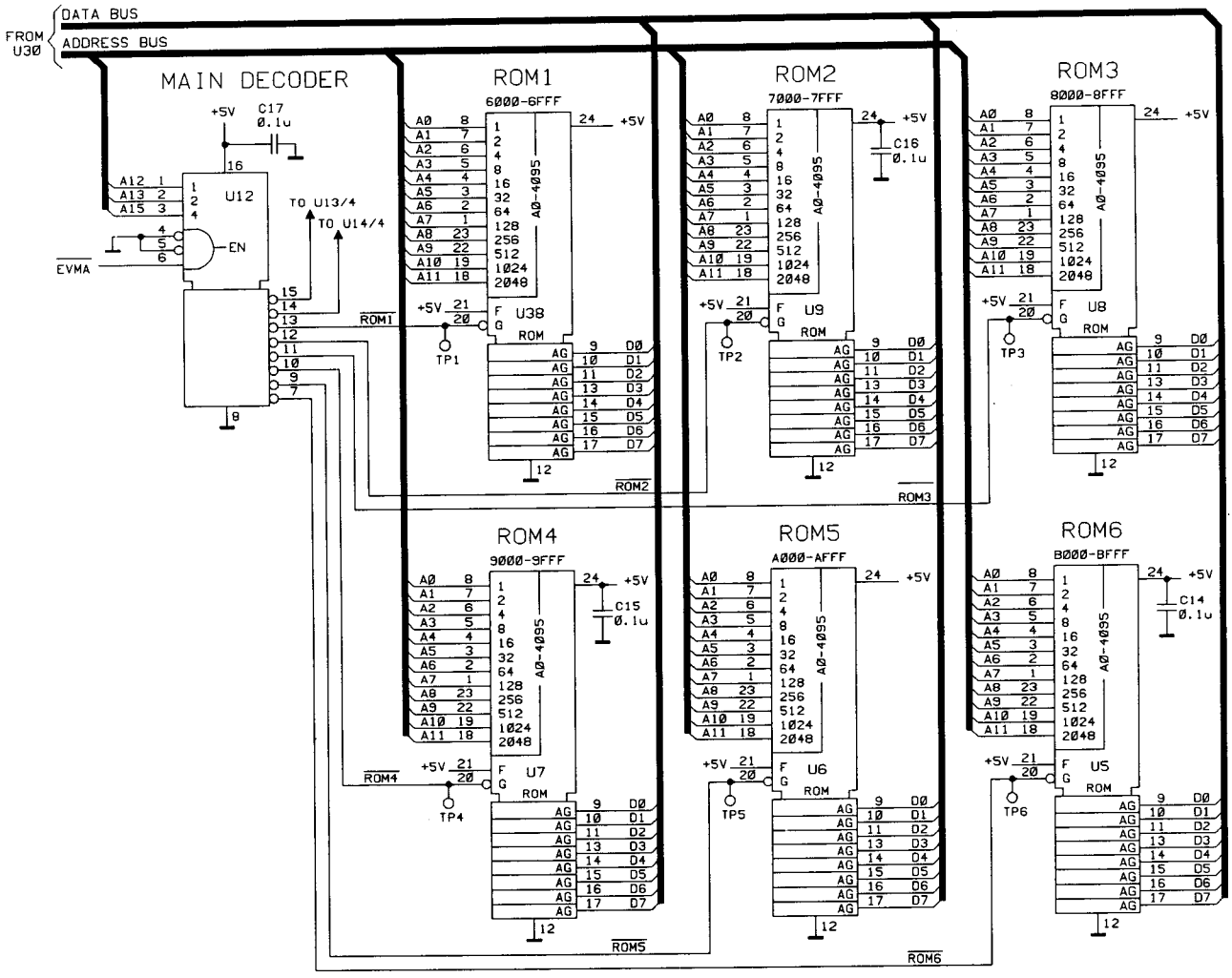


Figure B-5. 08116-66533: ROM schematic

4. Figure B-6 shows the location of U28 and other additional components, modify Figure 10.7-9 accordingly.

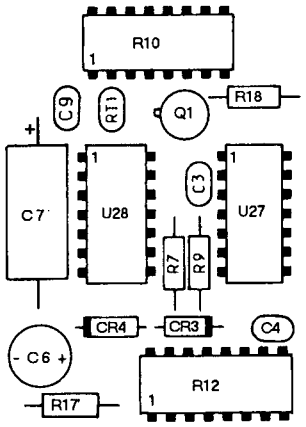


Figure B-6. 08116-66533: U28 layout

5. Figure B-7 shows the RAM battery supply circuit on microprocessor board 66533, modify Figure 10.7-5 accordingly.

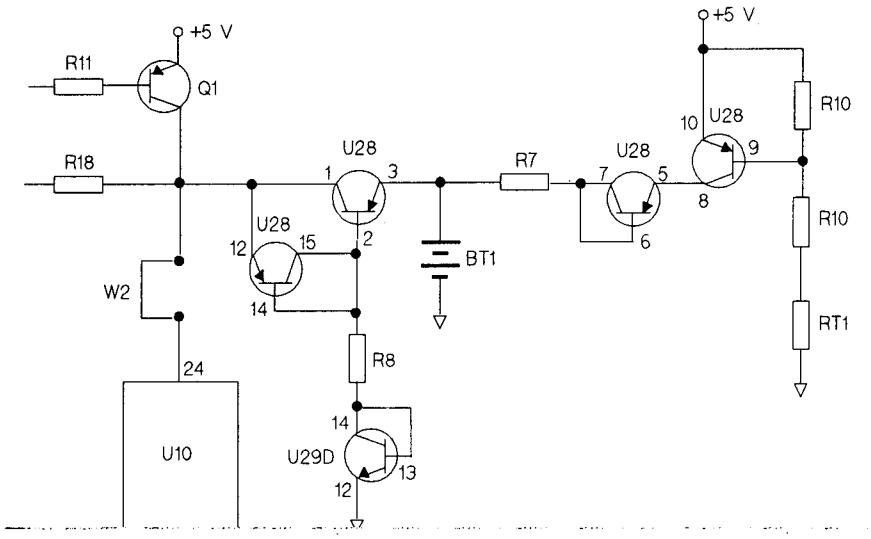


Figure B-7. 08116-66533: U28 schematic

6. Modify the schematic Figure 10.7-4 as shown in Figure B-8.

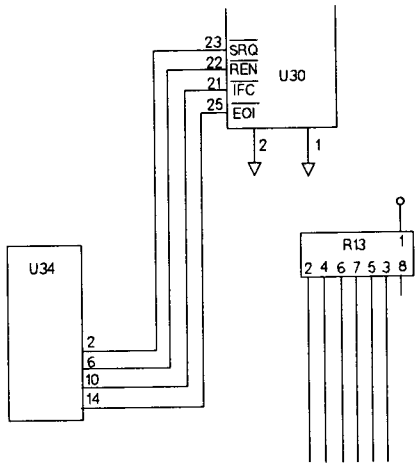


Figure B-8. 08116-66533: Deletion of W3

7. Figure B-9 shows the microprocessor reset circuit on microprocessor board 66533, modify the schematic Figure 10.7-5 accordingly.

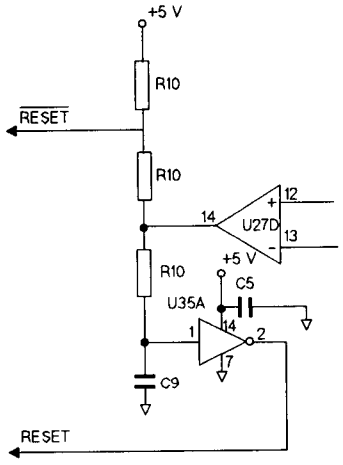


Figure B-9. 08116-66533: Reset circuit

8. In Chapter 10.7 substitute Table B-3, Table B-4, and Table B-5 for Table 10.7-3, *Signatures for address drivers and decoders*

Table B-3. Address bus Signature Analysis

Address Bus	Free Run S.A.	U1 Pin	U3 Pin	U4 Pin
A0	UUUU	9	2 18	
A1	FFFF	10	4 16	
A2	8484	11	6 14	
A3	P763	12	8 12	
A4	1U5P	13	11 9	
A5	0356	14	13 7	
A6	U759	15	15 5	
A7	6F9A	16	17 3	
A8	7791	17		2 18
A9	6321	18		4 16
A10	37C5	19		6 14
A11	6U28	20		8 12
A12	4FCA	22		11 9
A13	4868	23		13 7
A14	9UP1	24		15 5
A15	0002	25		17 3

Table B-4. Main Decoder Signature Analysis

Main Decoder	Free Run S.A.	U12 Pin	U13 Pin	U14 Pin	U9 Pin	U8 Pin	U7 Pin	U6 Pin	U5 Pin	TP
	2340	15	4							
	1C66	14		4						
$\overline{\text{ROM2}}$	20U0	12			20					2
$\overline{\text{ROM3}}$	4685	11				20				3
$\overline{\text{ROM4}}$	36F8	10					20			4
$\overline{\text{ROM5}}$	31AC	9						20		5
$\overline{\text{ROM6}}$	41P4	12							20	6

Table B-5. Sub Decoder Signature Analysis

Sub Decoder	Free Run S.A.	U10 Pin	U11 Pin	U13 Pin	U14 Pin	U15 Pin	U16 Pin	U18 Pin	U19 Pin	U23 Pin	U26 Pin	U30 Pin	U37 Pin
GPIA $\overline{CS}$	748C			7								3	
$\overline{Keyboard}$	U638			10					7				
$\overline{LB}$	89C7				14		11						
$\overline{ADD}$	C898				12			11					
$\overline{READ}$	6P25				11						1/19		
$\overline{LATCH1}$	HC8A				10					11			
$\overline{HP\text{-}IB}$	PHCC				7								9
$\overline{RAM\text{-}SEL}$	8UP9	8	8										
	5HP5			15		9							
	0A8U			14		10							
	H883			13		11							

9. In Chapter 10.7 modify the section on trouble-shooting the ROM as follows:

ROM The ROMs can be checked using signature analysis:

1. Set the microprocessor to free-run as described in Chapter 10.7 and connect the signature analyzer probes as instructed.

Signature Analyzer Probe connections for ROM Test

Probe	Trigger	Connect to
Start	↘	See Table B-6
Stop	ƒ	See Table B-6
Clock	↘	TP "E"
Ground		Ground

2. Connect the data probe to the +5 V supply and check that the signature is P254. If not, the microprocessor is not free-running.

3. For each ROM in Table B-6 connect the start and stop probes to the indicated test point and use the data probe to check the signature at the listed pins:

Table B-6. ROM signatures

ROM:	U9 ROM2	U8 ROM3	U7 ROM4	U6 ROM5	U5 ROM6
Start/Stop: Pin	TP2	TP3	TP4	TP5	TP6
9	0A6P	U88F	5808	3HA1	P191
10	UP1C	70CU	60F5	3HFH	61A8
11	95FH	6PC3	452P	03A9	01UP
13	4102	3C35	7733	34PH	H862
14	AHUA	U623	41PU	C3F0	61C1
15	06AF	A4HF	3H0H	73UF	F8H8
16	7000	2C09	P912	FP6U	5U29
17	4C7P	2125	8PF7	A795	P3F3

Changing the ROM

If the ROMs are changed, the data saved in the RAM has to be made compatible with the new ROMs. This can be done by setting the HP 8112A to RCL 0 and turning the instrument off and on again.

If the instrument becomes totally inoperable switch it off and disconnect the RAM back-up battery for at least 30 seconds. This will destroy the stored RAM data. Re-connect the RAM back-up battery and switch the instrument on. The Standard Parameter Set is now loaded into the RAM.

Change 42

A change in manufacturing method introduced a part number change for a widely used 0.47 μF capacitor.

Change 43

This change introduced a standardisation of switch part numbers, no backdating action is required.

Change 44

For instruments with serial number 2739G06580 and lower.

This change introduced a standardisation of switch part numbers, no backdating action is required.

Main Board

In Appendix A Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	MP2, MP3	Insulator	08112-05401

Change 45

For instruments with serial number 2739G06930 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	C523,524	CAP 270 μF 40 V	0180-2455

In Appendix A Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66511	W12,13		

In Appendix A Table A-3 *add*:

	Reference	Description	HP Part #
A1 08112-66511	F1,2	FUSE 5 A 125 V	2110-0297

Note

F1 replaces W12 and F2 replaces W13 in Figure 10.2-3 and 10.2-6

Change 46

This change introduced a component value change to provide increased slope adjustment range.

For instruments with serial number 2739G07230 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	Q282, Q283	XSTR PNP	1853-0218

Note

This change duplicates change 55

Control Board

In Appendix A Table A-4 *modify*:

	Reference	Description		HP Part #
A2 08112-66502	R37, R38	Resistor	200 Ω	2100-3212

Change 47

Changed component value to provide greater adjustment range and eliminate select on test value.

For instruments with serial number 2739G07280 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66511	R317	Resistor	2.15 k	0698-0084
	R318	Resistor	500 Ω	2100-0554

Change 48

Standardisation of case colors.

Note

Old case parts as detailed below can only be obtained as long as stocks last at the Hewlett-Packard manufacturing plant.

For instruments with serial number 22739G07380 and lower:

1. Make the following changes to the appropriate parts-lists:

Instrument

In In Appendix A, Table A-2 *modify*:

	Reference	Description	HP Part #
A0 08112	MP7	FRAME FRONT	5021-5813
	MP8	FRAME REAR	5021-0512
	MP17	COVER-BOTTOM	5001-1227
	MP18	COVER-TOP	08112-04160
	MP20	TRIM STRIP	5001-0438
	MP21	TRIM STRIP	5040-7203
	MP22	FOOT	5040-7201
	MP23	PNL REAR STD	5040-7221
	MP24	FOOT-REAR N-SKI	5040-7222
	B1	FAN-TBAX	3160-0266

In Appendix A, Table A-2 *add*:

	Reference	Description	HP Part #
A0 08112	B2	MOD MOTOR CON	3160-0310

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08112-66534	U40	ROM 6	08112-13726

Change 49

Changed component value to improve overshoot adjustment, and introduction of fast fuse.

For instruments with serial number 2851G07680 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	C529	Capacitor 1.0 pF	0160-4380

Instrument

In Appendix A, Table A-2 *modify*:

	Reference	Description	HP Part #
A0 08112	F1	Fuse 750 mA	2110-360

Change 50

IC changed to LS type

For instruments with serial number 2851G07780 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	R422	Resistor 4.64 k	0698-3155

Microprocessor Board

In Appendix A, Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08112-66534	U17	IC SN74I138	1820-2861

Change 51

Capacitor added on back of board from U100 Pin 12 to +5 V rail, to suppress spikes.

For instruments with serial number 2851G07980 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *delete*:

	Reference	Description		HP Part #
A1 08112-66511	C141	Capacitor	3.3 pF	0160-4382

Change 52

Changed component values to increase adjustment range.

For instruments with serial number 2851G08630 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66511	R410	Resistor	500 Ω	2100-0554
	R411	Resistor	2.61 k	0698-7246

Change 53

Heatsink added to Q282.

For instruments with serial number 2851G08780 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *delete*:

	Reference	Description	HP Part #
A1 08112-66511	MP201	Heatsink	1205-0235

Change 54

Heatsink changed Q505 and Q506 a capacitor added between Q282 collector and ground to improve trigger output.

For instruments with serial number 2851G08949 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	MP500	Heatsink	08116-04151

Main Board

In Appendix A, Table A-3 *delete*:

Reference	Description	HP Part #

Change 55

For instruments with serial number 2851G08699 and lower, make the following changes to the appropriate parts-lists:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112-66511	Q282, Q283	XSTR PNP	1853-0218

Note This change is repeated by change 46

Change 57

Component values changed to improve instrument performance at low operating temperatures required by changeover to new style Rate ICs.

For instruments with serial number 2851G09506 and lower, make the following changes to the appropriate parts-list:

Main Board

In Appendix A, Table A-3 *modify*:

	Reference	Description		HP Part #
A1 08112-66511	C200, C220	Capacitor	15 pF	0160-4385
	C240	Capacitor	18 pF	0160-4492
	R30	Resistor	200 Ω	0757-0407

Change 58

For instruments with serial number 3205G10006 and lower:

1. Make the following changes to the appropriate parts-lists:

Instrument

In Table A-2 *modify*:

	Reference	Description	HP Part #
A0 08112	A1	BD AY-MAIN	08112-66511
	A3	BD AY-MICROPRCR	08112-66534
	MP8	FRAME REAR 2	5021-5814
	MP11	HEATSINK POWER	08112-21105
	MP14	KEEPER	08112-04154
	MP25	FUSEHOLDER BODY	2110-0564

In Table A-2 *add*:

	Reference	Description	HP Part #
A0 08112	A6	BD AY-HPIB	08116-66506
	MP5	BRACKET FAN	08112-04156
	MP6	BRACKET XFMR	08112-04153
	MP9	PANEL REAR	5061-2116
	MP10	HEATSINK REAR	08112-21101
	MP12	SIDE STRUT 1/2M	5021-5831
	MP13	SIDE STRUT 1/2M	5021-5831
	MP17	COVER BOTTOM	5001-1233
	MP18	COVER TOP	08112-04170
	MP23	FOOT REAR	5041-8821
	MP29	FUHLR-CMPNT	1400-0090
	MP31	CLMP-CA	1400-0024
	MP32	STDF-HEX .327-IN	0380-0644
	MP34	WSHR-LK HLCL	2190-0074
	MP41	WSHR-LK INTL T	2190-0016

In Table A-2 *delete*:

	Reference	Description	HP Part #
A0 08112	C1	CAP 0.047uF 0 V	0160-4323
	MP50	CHASSIS	08116-60101
	MP51	BRACKET-XFMR	08116-01203
	MP52	BRACKET-XFMR	08116-01201
	MP54	SCR-TPG 8-16	0624-0413
	MP55	COVER	08116-04123

Main Board

In Table A-3 *modify*:

	Reference	Description	HP Part #
A1 08112		BD-AY MAIN	08112-66511
	MP1	HEATSINK	08112-21104
	R1	RES 47 5% 2W MO	0698-3615

Microprocessor Board In Table A-5 *modify*:

	Reference	Description	HP Part #
A3 08112		08112-66534	BD AY MICROPRCR
	C3	0160-5746	CAP 0.1uF 50 V
	C4	0160-5746	CAP 0.1uF 50 V
	C5	0160-5746	CAP 0.1uF 50 V
	C6	0180-2856	CAP 47uF 25 V
	C8	0180-2856	CAP 47uF 25 V
	C9	0160-5746	CAP 0.1uF 50 V
	C11	0160-5746	CAP 0.1uF 50 V
	C12	0160-5746	CAP 0.1uF 50 V
	C13	0160-5746	CAP 0.1uF 50 V
	C15	0160-5746	CAP 0.1uF 50 V
	C16	0160-5746	CAP 0.1uF 50 V
	C17	0160-5746	CAP 0.1uF 50 V
	C18	0160-5746	CAP 0.1uF 50 V
	C19	0160-5746	CAP 0.1uF 50 V
	C20	0160-5746	CAP 0.1uF 50 V
	C21	0160-5746	CAP 0.1uF 50 V
	C22	0160-5746	CAP 0.1uF 50 V
	C23	0160-5746	CAP 0.1uF 50 V
	C24	0160-5746	CAP 0.1uF 50 V
	C25	0160-5746	CAP 0.1uF 50 V
	C26	0160-5746	CAP 0.1uF 50 V
	C27	0160-5746	CAP 0.1uF 50 V
	C28	0160-5746	CAP 0.1uF 50 V
	C30	0160-5746	CAP 0.1uF 50 V
	C31	0160-5746	CAP 0.1uF 50 V
	C32	0160-5746	CAP 0.1uF 50 V
	C33	0160-5746	CAP 0.1uF 50 V
	C34	0160-5746	CAP 0.1uF 50 V
	C36	0160-5746	CAP 0.1uF 50 V
	J2	1251-8930	CONN-POST-TP-HDR
	R6	0757-0412	RES 365 1% .125W
	R12	1810-0316	NETWORK-RES DIP
	R13	1810-0206	NETWORK-RES SIP
	R22	0757-0442	RES 10K 1% .125W
	R24	0757-0283	RES 2K 1% .125W
	U40	08112-13727	ROM 1
	W4	5180-2405	CBL RBN 350 MM

In Table A-5 *delete*:

	Reference	Description	HP Part #
A3 08112	C10	CAP 0.1uF 50 V	0160-6623
	C14	CAP 0.1uF 50 V	0160-6623
	C35	CAP 0.1uF 50 V	0160-6623
	C37	CAP 0.1uF 50 V	0160-6623
	J4	CONN-POST-TP-HDR	1251-4670
	J5	CONN-POST-TP-HDR	1251-4672
	R25	RES 10K 1% .125W	0757-0442
	R26	RES 10K 1% .125W	0757-0442
	R27	RES 3.16K 1%	0757-0279

In Table A-5 *add*:

	Reference	Description	HP Part #
A3 08112	P1	SHUNT-PROGRAMMAB	1258-0124
	R23	RES 10K 1% .125W	0757-0442
	U18	IC-SN74LS273N	1820-1730
	W2	RES-ZERO OHMS	8159-0005

2. In the section "Rear Panel" in Chapter 4, delete Figure 4-12 and add the following figure and text:

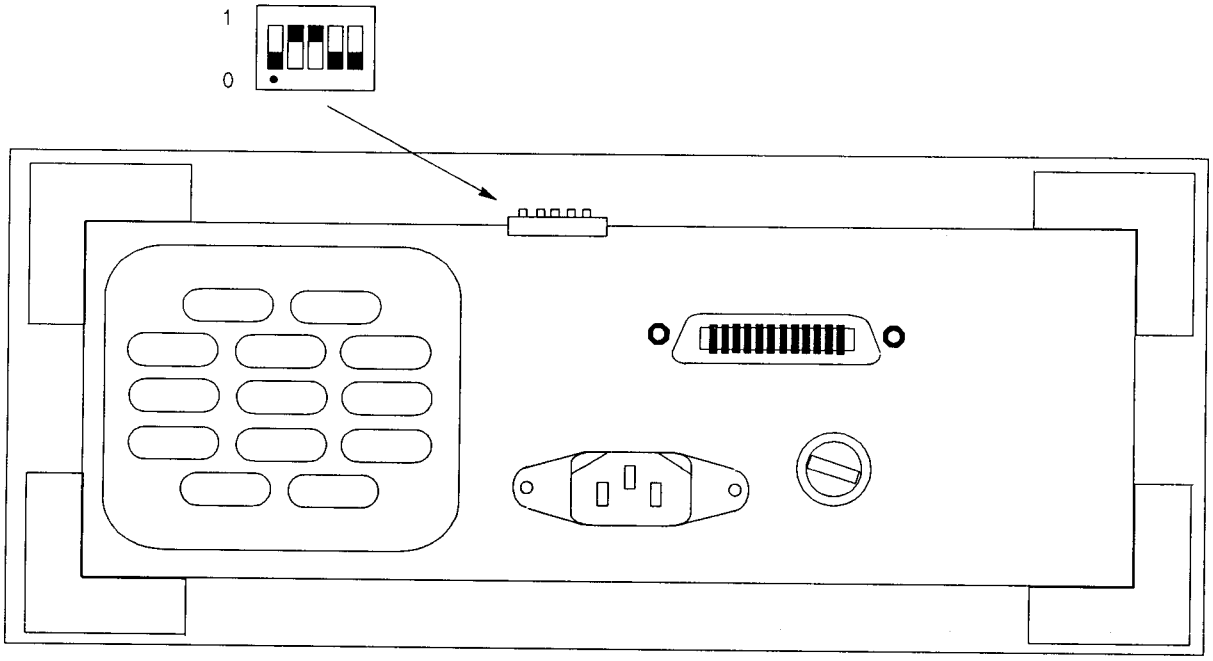


Figure B-10. Rear Panel

HP-IB Address

When the instrument is switched on it determines its HP-IB address from the address switches on the rear panel. The address switches are preset at the factory to 12 decimal:

To change the address, change the bit settings on the rear panel switch, then either press the [LCL] key, or switch the instrument off and on again.

Pressing the [LCL] key will display the current HP-IB address in decimal on the front panel digital display.

3. Delete the text in the section "Setting the HP-IB Address" in Chapter 6, and replace it with the following:

   The HP 8112A HP-IB address is read from the address switch on the rear panel when the instrument is switched on. The address switch is set at the factory to 12 decimal.

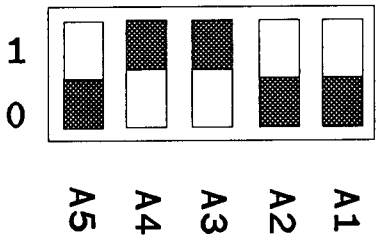


Figure B-11. HP-IB Address Switch (Factory setting)

Note

- Pressing the [LCL] key displays the current address while the key is depressed.
- When allocating addresses ensure that no two instruments on the bus have the same address.

To change the instrument address:

1. Change the address on the rear-panel address-switch.
2. Press the [LCL] key or switch the instrument off and on again.

4. In the section "General" in Chapter 10, correct the last sentence to read:

   The **six** board assemblies contained in the HP 8116A are listed in Table 10-1 which lists the servicing chapters applicable to each board.

5. Add the following line to Table 10-1 in Chapter 10:

HP-IB Connector Board	A6	10.7

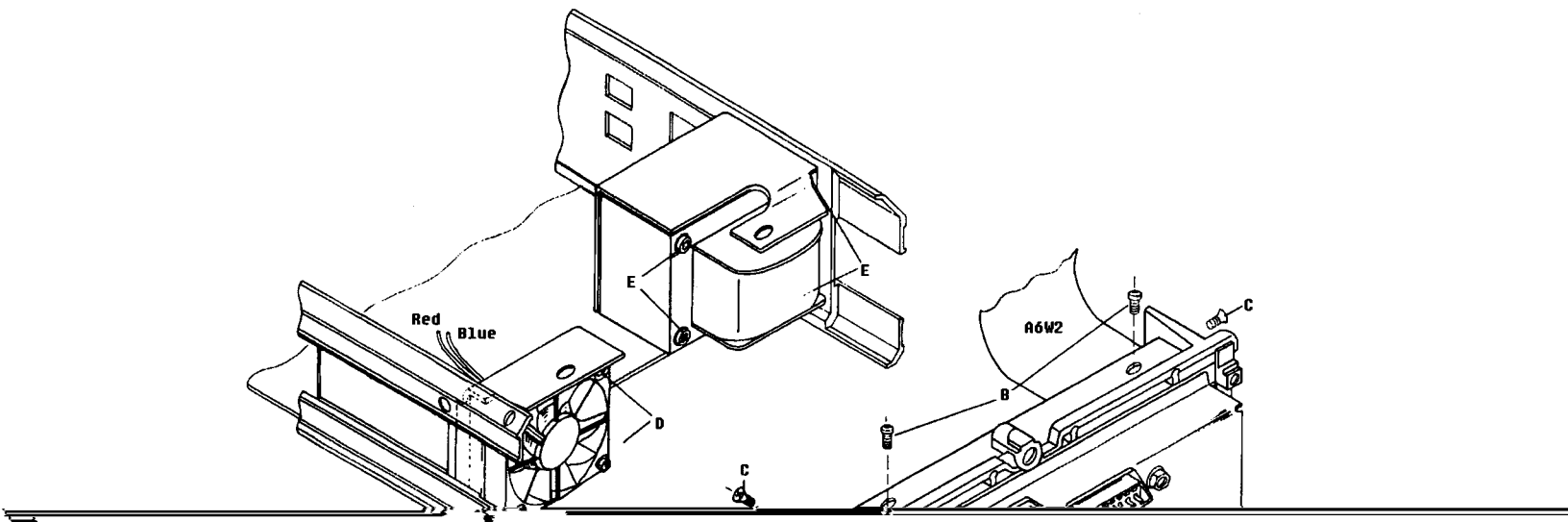
6. In the section "Preparing the HP 8112A for servicing" in Chapter 10.1, replace the procedure with the following text:

   1. Remove all four feet at the rear of the instrument by [illegible]

   2. Remove the single screw holding the instrument top cover to the rear panel.
   3. Remove the cover by sliding it backwards.
   4. Remove the four screws securing the microprocessor board.
   5. Lift the microprocessor board and stand it vertically by placing the cut-outs on the edge of the board over the locating lugs on the inside of the right-hand side-panel (as seen from the front of the instrument).
   6. Remove the screen covering the control board.
   7. Lift the control board and stand it vertically by placing the cut-outs on the edge of the board over the locating lugs on the inside of the left-hand side-panel (as seen from the front of the instrument).

7. In the section "Troubleshooting the Power Supply" in Chapter 10.2 delete the sub-sections "Removing the Fan", and "Re-fitting the Fan". Replace these sections with the following:

   Starting with the instrument in its servicing position (as described in Chapter 10.1 and referring to Figure B-12:


Red
Blue
E
E
D
C
A6W2
B
C

8. In Chapter 10.2 make the following change to the schematic diagram for the Main Board A1, Figure 10.2-2 as follows:

   Delete the capacitor C1 (0.047 μF) from the outputs of the line filter.

9. In Chapter 10.7 replace the component location diagram for the Microprocessor Board, Figure 10.7-8, with the following:

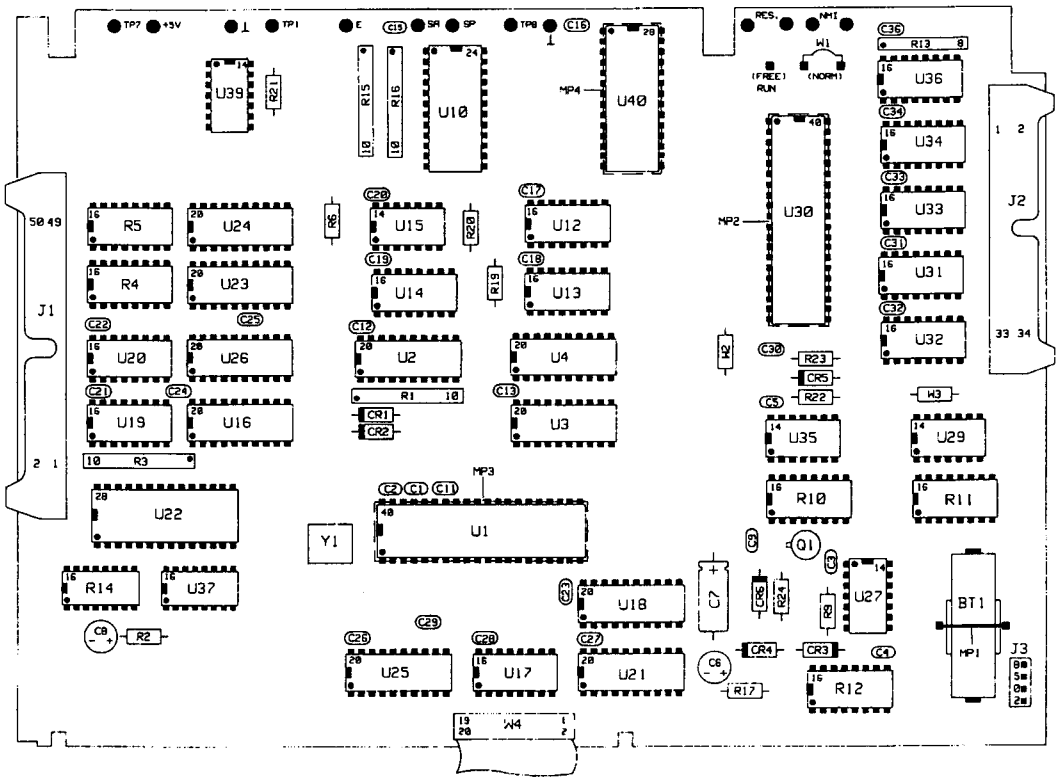
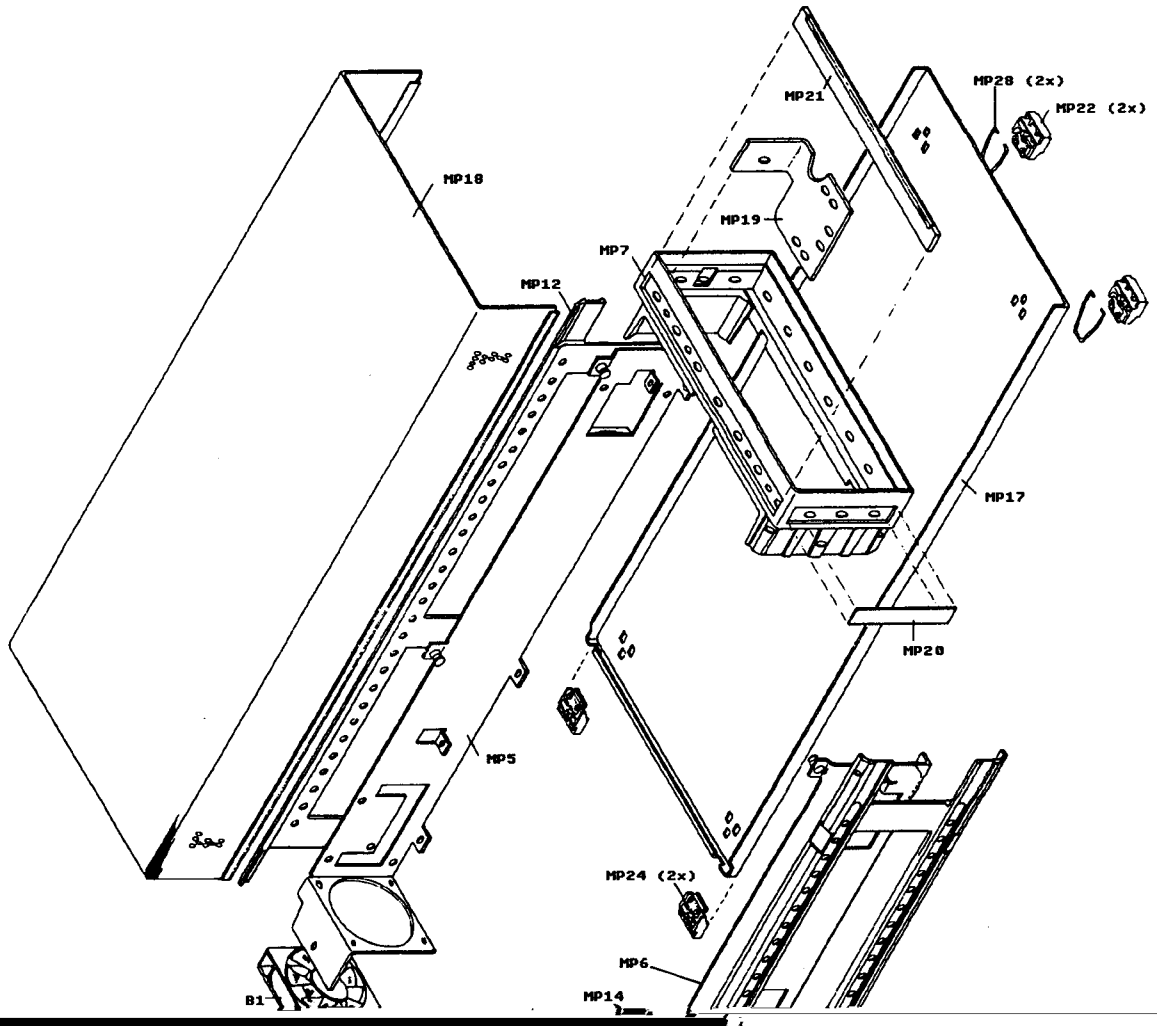


Figure B-13. Microprocessor Board A3 Component Layout and Locator

10. In Appendix A delete Figure A-1 and Figure A-2 and add the following two figures:


MP28 (2x)
MP21
MP22 (2x)
MP18
MP19
MP7
MP12
MP17
MP20
MP5
MP24 (2x)
MP6
MP14
B1

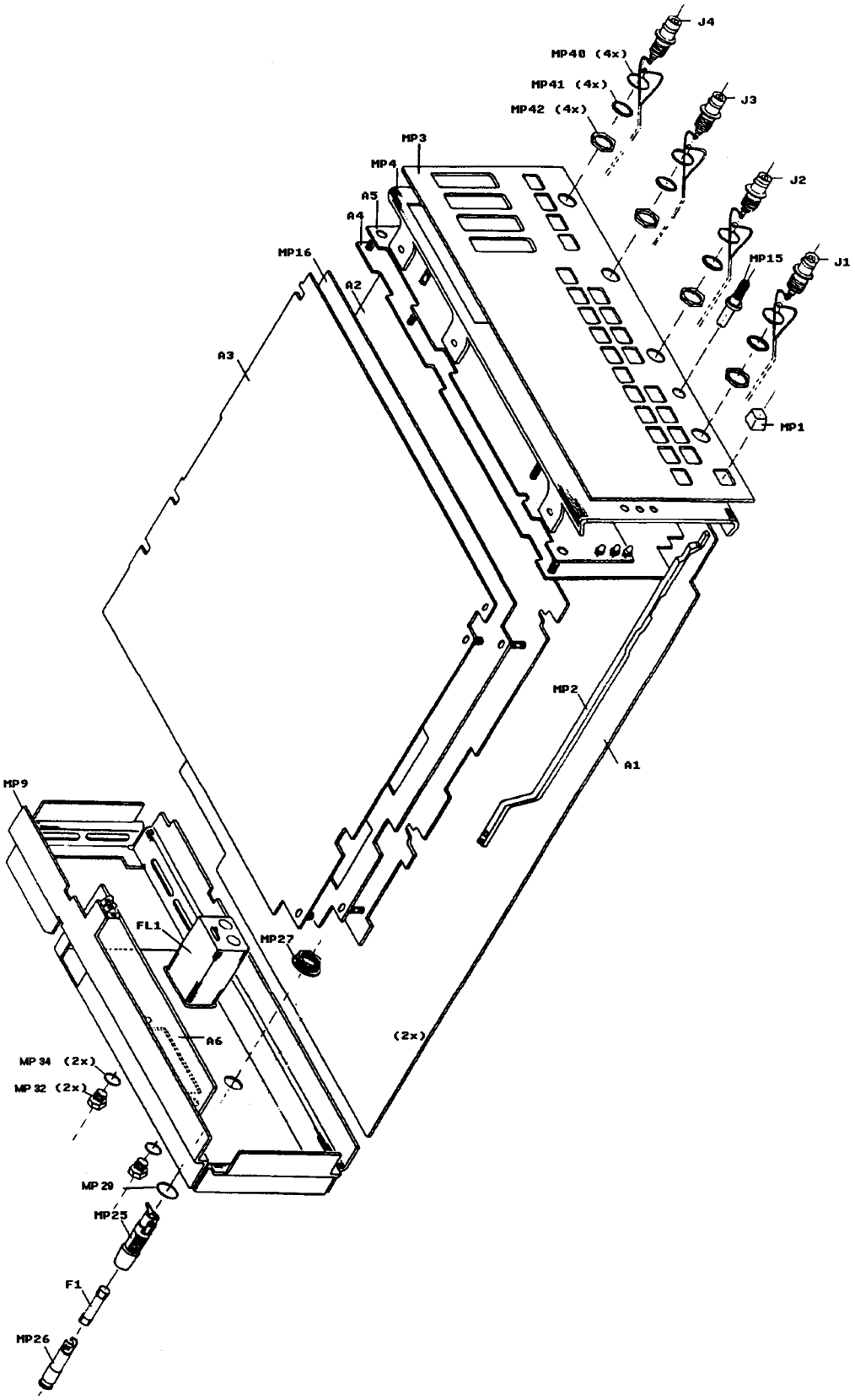


Figure B-15. Mechanical Parts - 2

C

Updating

Introduction

This appendix contains information to correct errors in the manual, and to update the manual for instruments with a serial number *higher* than that shown on the title page of this manual.

Please file all update information behind this page. If any text or drawings are affected, it is useful to indicate whether that update information has been incorporated in the manual.

You should ensure that you request update information for this manual at regular intervals from Hewlett-Packard.

app V

HEWLETT PACKARD

MANUAL CHANGES

July, 1996

Manual for Model Number	8112A
Manual printed on	January 1992
Manual Part Number	08112-90004

Make all ERRATA corrections.

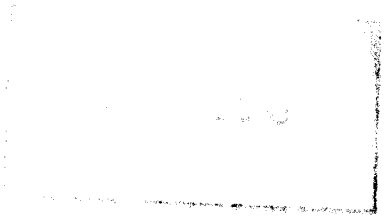
Check the following table for your instrument serial prefix/serial number/EDC and make the listed changes to your manual

New Item

Serial Prefix or Serial Number	Manual Changes
ERRATA	
3205G10181	1
3205G10381	2
3205G10706	3
3205G10986	4
3205G11016	5
3205G11616	6
3205G11841	7

INDEX OF MANUAL CHANGE

MANUAL CHANGE	FRAME	A1	A2	A3	A5
ERRATA					
1		C18,19,281 C310,312, C314,405, C507,508, C519,520, C521,522	C1		
2				J3,W3	
3		U301,401			
4				U10	
5		U301			
6					DS21
7		U401			



ERRATA

On Page A-7, change the Table of Repl.Parts to read:

MP58	5180-2471	CABLE HP IB
MP60	0380-0643	SCREW HP IB

On Page A-36, change the Table of Repl.Parts to read:

A3	U40	08112-13729	ROM1

On Page 9-2, Adjustment Procedure, change to read:

A1	C541	0.01uF (was pF)

On Page 9-3, Adjustment Procedure, change to read:

A1(was A2)	R243	46.4k_ endash; 51.1K_
A1(was A2)	R248	1.96k_

On Page 9-3, Adjustment Procedure add:

A1	C245	47pF

On Page a-36, change the Table of Repl.Parts List add:

A3	W2	8159-0005	RES O CWM

ERRATA (Cont.)

page 1-3, Introduction

Accessories

Change to read:

Item		HP Part Number	Description
Carrying handle		5062-4001	Bail Handle Kit
Rack mounting a single unit		5062-3972	Rack Mounting Flange and Filler Panel Kit
Rack mounting a single unit on a shelf		5062-3996	Support Shelf
	+	5062-4022	Filler Panel
	+	08116-68703	Special Mounting Kit
Rack slide mounting of a single unit		5062-3996	Support Shelf
	+	5062-4022	Filler Panel
	+	1494-0015	Rack Slide Kit
	+	08116-68703	Special Mounting Kit
Rack mounting of two units side by side		5062-3974	Rack Flange Kit
	+	5061-9694	Lock Link Kit
Rack mounting of two units side by side on a shelf		5062-3996	Support Shelf
	+ 2x	08116-68703	Special Mounting Kit
Rack slide mounting of two units side by side		5062-3996	Support Shelf
	+	1494-0015	Rack Slide Kit
	+ 2x	08116-68703	SpecialMounting Kit
Linking with an HP 8112A, s/n 3127G10005 and lower, a special linking kit is required		08116-68704	Special Linking Kit

ERRATA (Cont.)

page 1-4, Introduction

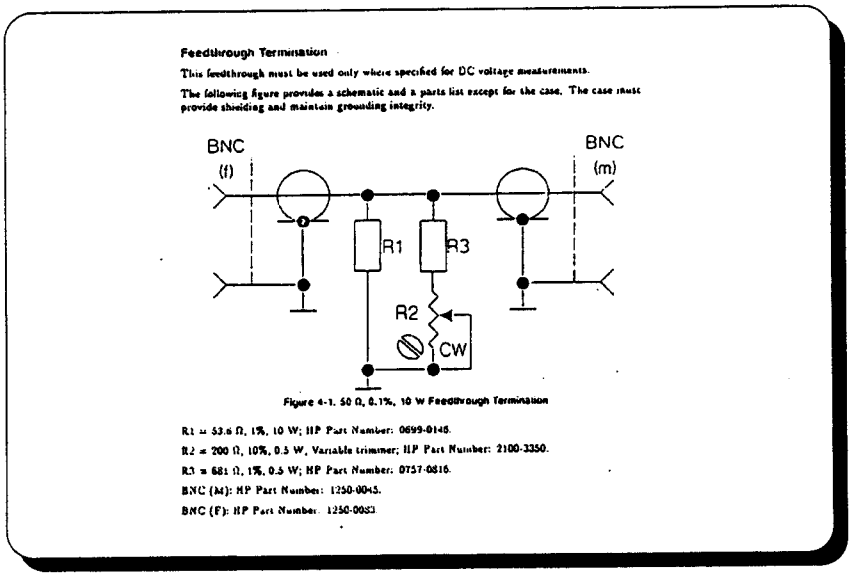
and
page 8-2, Testing Performance

Test Equipment Required

Add or change to read:

Instrument	Recom. Model	Characteristics	Alternative	Use
Counter	HP 5335A HP 5370B	50 MHz TI A to B	HP 5334A/B HP 5370A	P, A P, A
Digitizing	HP 54121T HP 54503A	..... 500 MHz Bandwidth	.....	...
Adaptor	HP 1250-1200	SMA (m) to BNC (f)		P
Feedthrough	HP 10100C see Figure: Feedthrou Termination	50 ohms, 2 W 50 ohms, 10 W		P, A P

Add: Figure: Feedthrough Termination



ERRATA (Cont.)

page 2-3, Specifications

Output parameters change to read:

Settling Time: 100 ns

page 8-16, Testing Performance

Pulse Performance Test change to read:

Settling Time: 100 ns

page 8-17, Testing Performance

Pulse Performance Test

First table: change to read:

Settling Time <= 100 ns (third line in the first table)

Second table:

Delete settling time test with linear transitions!

Delete:

Settling Time <= 107 ns (third line in the second table)

page 8-38, Testing Performance

Test Record page of Pulse Performance

First table: Change to read:

Settling time <= 100 ns

Second table:

Delete:

Settling time <= 107 ns

ERRATA (Cont.)

page 8-12, Testing Performance

Output Levels Performance Test change to read:

step 3. Set up the DVM as follows

Function DCV

Add or
Change: Measurement Peak Voltage

HP 3458A setup for peak-voltage measurement:

Function DCV

MENU -> Trig EXT
(press Trig button, select EXT, terminate
with ENTER key)

MENU -> NPLC 0.1
(press NPLC button, press period ".",
then "1" keys, terminate with ENTER key)

HP 3456A setup for peak-voltage measurement:

Function ⎓ V

TRIGGER EXT

N CYC INT 0.1
(press period ".", then "1" keys,
press STORE button,
press CHS (N CYC INT) key)

page 9-2, Adjustment Procedures

Table 9-1, Adjustment Procedures - Changeable Components change to read:

Procedure	Reference	Range	Description
Overshoot/Transition Times	A1 C532	0 pF (open) to 33 pF	Increasing V532 dereases transition times and increases overshoot in FIXED and LINEA mode

ERRATA (Cont.)

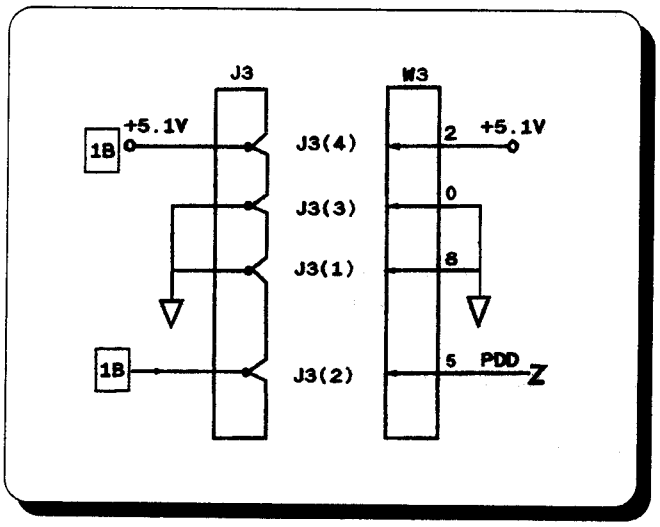
page 10.1-5, Troubleshooting Guide

RAM Test change to read:

The microprocessor is unable to load a test pattern into the RAM U10 and verify it.....

page 10.7-9, Servicing the Microprocessor

Schematic 2 (3B), Figure 10.7-5



page A-2, Replaceable Parts

Add as a title:

MASTER PARTS:

page A-3, Replaceable Parts

Add as a title to the upper two figures:

MASTER PARTS (continued):

Add as a title to the third figure:

KEYBOARD PARTS:

ERRATA (Cont.)

page A-6, Replaceable Parts

Table A-2

Add descriptions:

Reference	...	Description	...	...
A0 MP1	...	KEY	...	...
A0 MP2	...	SHAFT-POWER-SW	...	...
A0 MP4	...	PNL SUB	...	...
A0 MP7	...	FRAME FRONT	...	...
A0 MP15	...	KNOB, LONG	...	...
A0 MP16	...	SHIELD	...	...
A0 MP19	...	HEATSINK OUTPUT	...	...
A0 MP20	...	TRIM STRIP	...	...
A0 MP21	...	TRIM STRIP	...	...
A0 MP22	...	FOOT	...	...
A0 MP24	...	FOOT REAR, N-SKI	...	...
A0 MP33	...	COVER-PLASTIC	...	...
A0 T1	...	TRANSFORMER, PWR	...	...

page A-14, Replaceable Parts

Table A-3

Add the descriptions:

Reference	...	Description	...	...
A1 MP1	...	PLATE TRANSISTOR	...	...
A1 MP2	...	PLATE INSULATOR	...	...
A1 MP3	...	PLATE INSULATOR	...	...
A1 MP4 to A1 MP20		>>> see next Page 10 <<<		
A1 MP100	...	BRACKET	...	...
A1 MP500		TRANSISTOR - HEATSINK		

ERRATA (Cont.)

Add to Page A-14, Table A-3

REFERENCE DESIGNATOR	C D	H-P PART NUMBER	DESRCIPTION
A1 MP4	5	1200-0181	INSUL-XSTR NYLO
A1 MP5	7	1400-0824	STRAP-CABLE
A1 MP6	0	1251-0600	CONN-SGL CONT
A1 MP7	1	0515-0652	SCR-MACHINE
A1 MP8	8	0610-0003	NUT-HEX-DBL-CHA
A1 MP9	7	0520-0128	SCR-MACH 2-56
A1 MP10	9	3050-0017	WSHR-FL MTLC
A1 MP11	3	2950-0072	NUT-HEX-DBL-CHA
A1 MP12	4	2190-0067	WSHR-LK INTL T
A1 MP13	0	2190-0584	WASHER-LK HLCL
A1 MP14	7	3050-0891	WASHER-FL MTLC
A1 MP15	4	3050-1101	WASHER-SHLDR 3
A1 MP16	9	0515-1111	SCR-MACH M3X0.5
A1 MP17	4	0535-0025	NUT-HEX DBL-CHA
A1 MP18	7	0515-1755	SCR-MACHINE
A1 MP19	0	2190-0112	WSHR-LK HLCL
A1 MP20	8	4330-0467	INSUL-BEAD GLAS

page A-24, Replaceable Parts

Table A-3

Add the descriptions:

Reference	...	Description	...	...
A1 U200	...	TIMING IC, PERIOD	...	...
A1 U220	...	TIMING IC, DELAY	...	...
A1 U240	...	TIMING IC, WIDTH	...	...

ERRATA (Cont.)

page A-25, Replaceable Parts

Table A-3

Add the descriptions:

Refernce	...	Description	...	...
A1 W8	...	CABLE AY SIG OUT	...	...
A1 W9	...	CABLE AY TRG OUT	...	...
A1 W10	...	CABLE AY CTL IN	...	...
A1 W11	...	CABLE AY EXT/TRG IN	...	...

page A-37, Replaceable Parts Table A-6

Add the descriptions:

Reference	...	Description	...	...
A4 MP1	...	KEY CAP QUARTER	...	...
A4 MP2	...	KEY CAP QUARTER	...	...
A4 MP3	...	KEY CAP QUARTER	...	...
A4 MP4	...	KEY CAP SRF-G-L	...	...
A4 MP5	...	KEY CAP SRF-G-L	...	...
A4 MP6	...	KEY CAP SRF-G-L	...	...
A4 MP7	...	KEY CAP LCL	...	...
A4 MP8	...	KEY CAP PRL-G L	...	...
A4 MP9	...	KEY CAP PRL-G L	...	...
A4 MP10	...	KEY CAP PRL-GRA	...	...
A4 MP11	...	KEY CAP PRL-GRA	...	...

ERRATA (Cont.)

page A-38, Replaceable Parts

Table A-6

Add the descriptions:

Reference	...	Description	...	...
A4 MP12	...	KEY CAP SRF-G L	...	...
A4 MP13	...	KEY CAP SRF-G L	...	...
A4 MP14	...	KEY CAP GRN LT	...	...
A4 MP15	...	KEY CAP PRL-G L	...	...
A4 MP16	...	KEY CAP PRL-G L	...	...
A4 MP17	...	KEY CAP SRF-G L	...	...
A4 MP18	...	KEY CAP SRF-G L	...	...
A4 MP19	...	KEY CAP SRF-GRA	...	...
A4 MP20	...	KEY CAP PRL-G L	...	...
A4 MP21	...	KEY CAP PRL-G L	...	...
A4 MP22	...	KEY CAP PRL-G L	...	...
A4 MP23	...	KEY CAP PRL-G L	...	...

page A-39, Replaceable Parts

Table A-6

Add the description:

Reference	...	Description	...	...
A4 W1	...	CABLE AY RBN 260 MM	...	...

ERRATA (CONT.)

On page 10.1-5, Instrument Overview and Troubleshooting Guide

RAM Test

E01

delete: U11

Timing Tests

E 12

change to read:

...Possible failure of Delay control circuit U5, U7, Error feedback U140, level shifter Q200 or Period IC U200. ...

E 13

change to read:

...Possible failure of Width control circuit U6, U8, Error feedback U141, level shifter Q220, Period IC U200 or DelayIC U220. ...

E 14

change to read:

...Possible failure of Slope control circuit U12, U13, U14 or U302, Slope range switching circuit Q305 to Q309, U300, reference circuit U320, Period IC U200, Delay IC U220 or Width IC U240. ...

ERRATA (Cont.)

page 2-7, Specifications add:

General Characteristics
Capitel 2

DECLARATION OF CONFORMITY

similar to ISO/IEC Guide 22)

Manufacturer: Hewlett-Packard GmbH
Boeblingen Instruments Division
Herrenberger Str.130
D-71034 Boeblingen
Germany

We declare that the product

HP 8112A Pulse Generator

conforms to the following standards:

Safety: IEC 348 (1978)

EMC: EN 55011 (1991) / CISPR 11 Group 1, Class A
EN 50082-1 (1991)
IEC 801-2 ESD: 4kV cd, 8kv ad
IEC 801-3 Radiated Immunity: 3V/m
IEC 801-4 Fast transients: 0.5kV, 1kV

Supplementary Information:

During the measurements against EN 55011, the I/O ports were terminated with their nominal impedance, the HP-IB connection was terminated with the cable HP 10833B. When the product is connected to other devices, the user must ensure that the connecting cables and the other devices are adequately shielded to prevent radiation.

Boeblingen, 25th August 1993
Hans Baisch
Product Regulations Consultant

MANUAL CHANGE 1

On Page A-8/9/10/11, Repl.Parts List,change to read:

A1	C18,19,281, C310,312,314 C405,507,508 C519,520,521 C522	,0160-3097	CAP 0.47uF 50V

On Page A-26, Repl.Parts List,change to read:

A2	C1	0160-3097	CAP 0.47uF 50V

MANUAL CHANGE 2

On Page A-34, Repl.Parts List, delete:

A3	J3	1251-3167	CONN-POST-TB

On Page A-36, Repl.Parts List, add:

A3	W3	08116-61693	CBL BD AY'S

On 8112A Manual Page 10.7-9 middle left side correct schematic as follows:

From Main Board A1 J3 pin W3 (J3) color Signal
ground V--.< 1 <--------V gray ground
page 1B ---.< 2 <--------- green PDD
ground V--.< 3 <--------V black ground
+5.1V O--.< 4 <--------- red +5.1V

NOTE: EDC-LBL:ENGINEERING DATE CODE
LABEL = BOARD REVISION
+ DATE CODE

MANUAL CHANGE 3

On Page A-24/25, Repl.Parts List, change to read:

EDC-LBL				
A-3310	A1	U301	1DB6-0001	IC SNAKE
		U401	1DC7-0001	IC BOOSTER

MANUAL CHANGE 4

On Page a-6, Repl.Parts List, change to read:

A-3401	A3	U10	1818-1768	IC HM6116LP-3

MANUAL CHANGE 5

On Page A-24, Repl.Parts List, change to read:

A-3408	A1	U301	1826-0955	IC 1DB6

MANUAL CHANGE 6

On Page A-40, Repl.Parts List, change to read:

B-3550	A5	DS21	1990-1840	LED-LT BAR

MANUAL CHANGE 7

On Page A-25 Repl.Parts, Table A-3 Parts List change to read:

A-3624	A1	U401	1826-0923	IC BOOSTER

D

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