Diplomarbeit

Design of Monolithic Integrated Lumped Transformers in Silicon-based Technologies up to 20 GHz

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Abstract

Monolithic integrated lumped planar transformers have several advantages when using them in power amplifiers, mixers, oscillators and other radio frequency circuits. But, up to now there was no way to get an accurate prediction and model of the electrical characteristic of on-chip transformers.

For the first time this work presents the modeling and model verification of integrated lumped planar transformers in silicon which have excellent performance characteristics in the 1-20 GHz frequency range. A new method for characterization of monolithic lumped planar transformers is proposed in this work.

The metallization of a semiconductor process defines the possibilities for transformer design. Planar and layer construction of common monolithic lumped transformers and its optimization techniques are considered in detail. A lumped low-order equivalent circuit is presented which results from the transformer geometries.

The aim of precise and fast transient analysis of RF circuits using monolithic transformers was reached with the compact lumped low order model which consists of 24 elements. The model gives accurate prediction of the electrical behavior and ensures fast transient analysis. An excellent prediction accuracy is achieved.

Background details about extraction of all elements used in the equivalent circuit are given. The inductance of transformers built up from straight conductors is derived. Skin effect and current crowding cause losses in the conductors. The conductive substrate causes additional losses. Some thesis about the parasitic capacitive coupling between the windings and the substrate are presented.

The parameter extraction for the equivalent circuit is based on a tool developed by the author which uses a new expression for the substrate loss and two finite element method cores.

The modeling and parameter extraction of monolithic transformers has been verified by multiple transformers. In this work the measurement of two types of transformers is presented as example. The first type offers a high coupling performance up to 4 GHz. The second type of transformer offers a high self resonance frequency of 20 GHz. Measurement and simulation of the two transformers show excellent agreement.

List of Abbreviations

Al	Aluminum
CAD	Computer Aided Design
δ	Depth of Current Penetration in [m]
DECT	Digital Enhanced Cordless Telecommunication
DC	Direct Current
DUT	Device Under Test
ε_r	Relative Permittivity in [1]
FEM	Finite Element Method
f_{Op}	Operation Frequency in [Hz]
$GaAs$	Gallium-Arsenide
GMD	Geometric Mean Distance in [m]
IC	Integrated Circuit
k	Coupling Coefficient in [1]
L	Inductance in [H]
λ_g	Guided Wavelength in [m]
n	Turn Ratio in [1]
N	Number of Turns in [1]
M	Mutual Inductance in [H]
μ	Permeability in [Vs/Am]
Q	Quality Factor in [1]
RF	Radio Frequency
ρ	Specific Resistivity in [Ωm]
σ	Conductivity in [S/m]
Si	Silicon
Si_3N_4	Siliconnitride
SiO_2	Silicondioxide
VLSI	Very Large Scale Integration

Chapter 1

Introduction

Transformers have been used in radio frequency circuits since the early days of telegraphy. Normally transformers are relatively large and expensive components in a circuit or system. But there are several outstanding advantages using transformers in circuit design:

- DC isolation between primary and secondary winding
- BALUN function
- Impedance transformation and matching
- No power consumption

The requirements of nowadays telecommunication systems needs a high degree of monolithic integration. Today it is possible to integrate lumped planar transformers in Si- and GaAs-based IC technologies which have excellent performance characteristics in the 1-20 GHz frequency range. The outer dimensions are in the range of about 500 μm down to 60 μm diameter depending on the frequency of operation and the IC technology.

Monolithic integrated lumped planar transformers are introduced by [Rabjohn 89]. A review of the electrical performance of passive planar transformers in IC technology was presented by [Long 00]. Amplifiers and mixers using monolithic transformers are presented in [McRory 99], [Long 99]. A monolithic 2 GHz Meissner-type voltage controlled oscilallator is realised in [Wohlmuth 99]. The transformer coupled push-pull type amplifier was invented in the early days of tubes. Recent designs in monolithic integration of this concept shows a high performance [Simbürger 99],[Simbürger 00],[Heinz 00].

Figure 1.1(a) shows the schematic diagram of a monolithic transformer coupled RF power Amplifier for 2 GHZ in SI-bipolar [Simbürger 00].The circuit consists of a transformer X1 as input-balun, a driver stage T1 and T2, a transformer

X2 as interstage matching network and a power output stage T3 and T4. The transformers X1 and X2 are of the same kind.

Figure 1.1b shows the chip micrograph of the power amplifier. The key elements of this circuit are two high performance on-chip transformers of the same kind, which work as input balun and for interstage matching.

A detailed micrograph of the on-chip transformer is shown in Figure 1.2. A more detailed description of this transformer is given in Sect. 4.1.

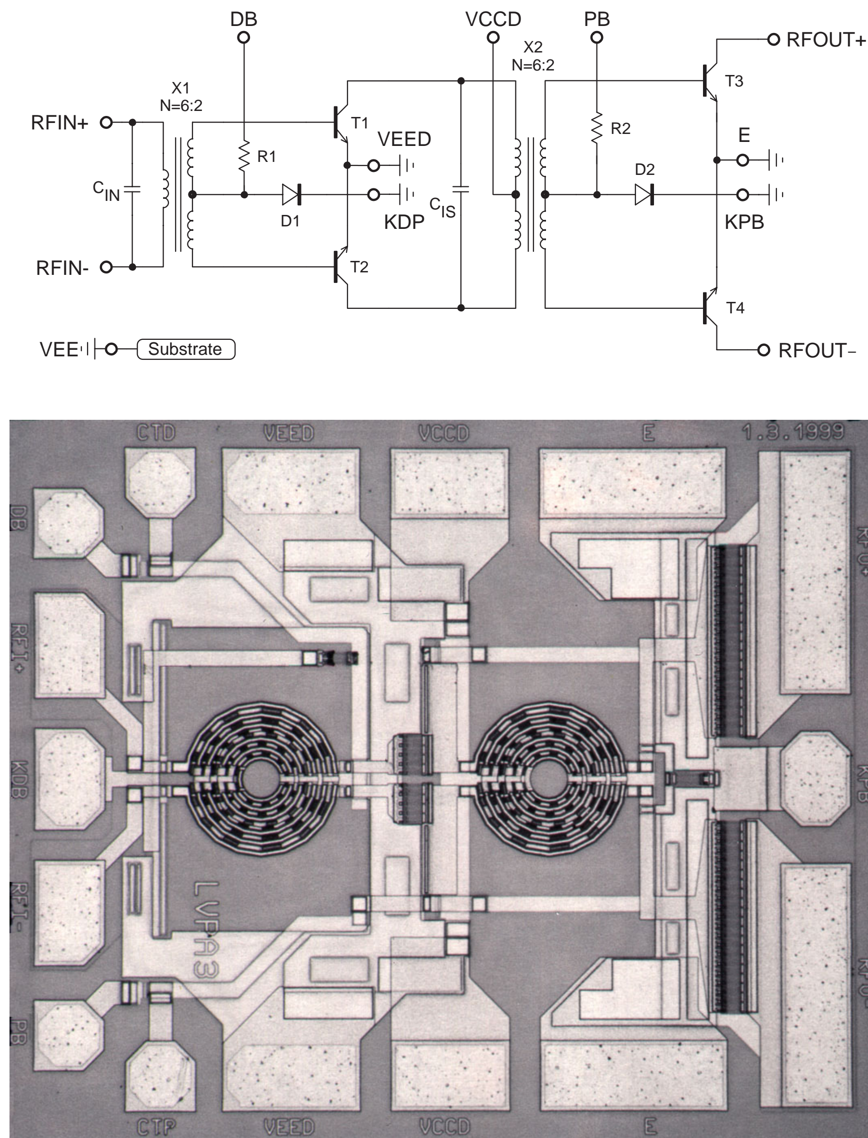

Figure 1.1: (a) Schematic diagram of a power amplifier using integrated lumped planar transformers (b) Micrograph of the 2 GHz RF power amplifier [Simbürger 00]

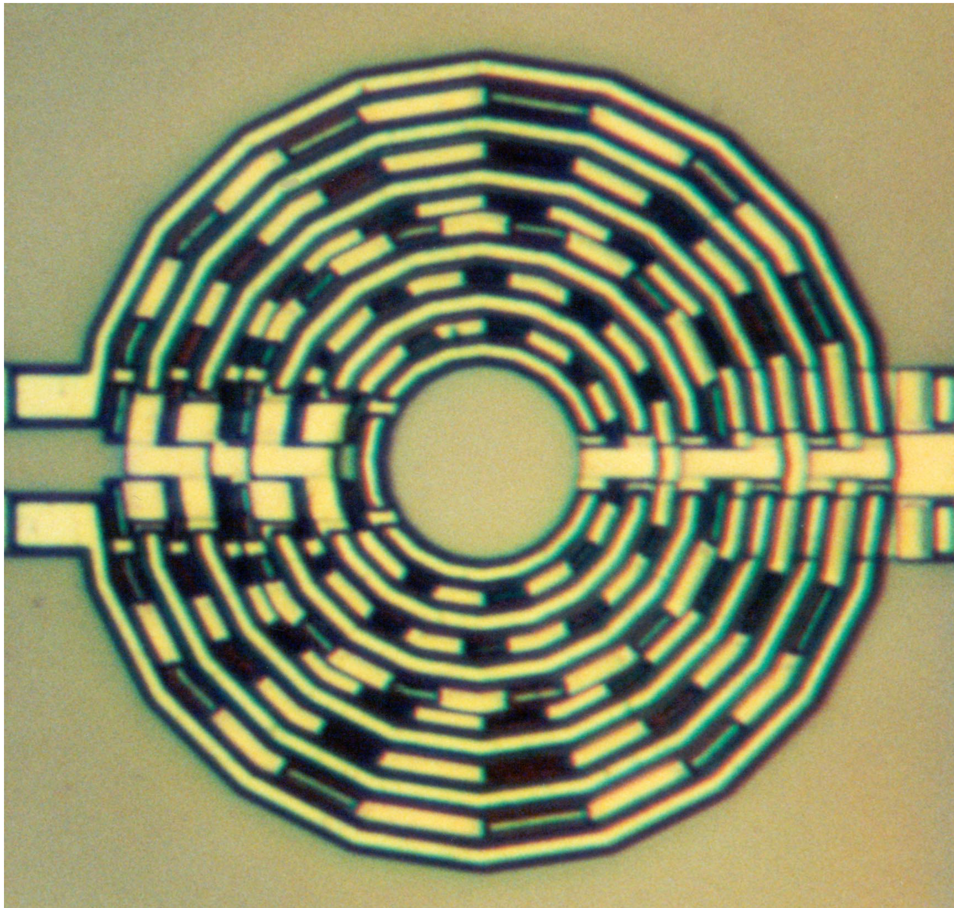

Figure 1.2: Micrograph of an on-chip transformer. Size: 205 μm diameter

The operation of a lumped transformer is based upon the mutual inductance between two or more conductors or windings.

In contrast to an ideal transformer, monolithic integrated transformers have parasitic effects and imperfect coupling between the windings which results in a coupling coefficient less than one. However, monolithic integrated lumped transformers have not the characteristics of an ideal component. To create a successful design including a integrated transformer it is not enough to know the transformers turn ratio. A sufficient specification includes at least the main electrical parameters, which are inductance and coupling coefficients of multiple coupled inductors of the windings, ohmic loss in the conductor material of the windings due to skin effect and current crowding, parasitic capacitive coupling between the windings and parasitic capacitive coupling into the substrate and finally substrate loss.

The limitations of monolithic integrated transformers on silicon must be clearly understood by the circuit designer in order to get an overall successful circuit design. Up to now there was no way to get an accurate prediction and models of

the electrical characteristic of the on-chip transformers.

For the first time this work presents the modeling and model verification of integrated lumped planar transformers in silicon. A lumped low order model which consists of 24 elements is presented. The model gives accurate prediction of the electrical behavior and ensures fast transient analysis, because of the low complexity. This work presents a method of parameter extraction for the equivalent circuit. The method is based on a tool developed by the author. The tool, called *FastTrafo*, uses a new expression for the substrate loss and two finite element method (FEM) cores available from Massachusetts Institute of Technology called *FastHenry* [MIT 96] and *FastCap* [MIT 92].

FastTrafo consists of three program modules. The first module computes the self inductances and mutual inductances of the primary and secondary winding and the ohmic loss due to the resistivity of the conductor material, skin effect and current crowding. The substrate loss is calculated by a formula which follows from characteristic impedances [Hilberg 81] and simulations using the FEM-solver *Maxwell-Field* by [Ansoft 93]. The second module computes the parasitic capacitance between primary winding, secondary winding and the substrate. The third program module creates a SPICE netlist of the equivalent model which is then compared to measurement data of the transformer (if available).

Chapter 2 presents the design and construction of monolithic planar transformers. The metallization of a semiconductor process defines the possibilities for transformer design. Design rules and optimization techniques are presented. A lumped low-order equivalent circuit results from the transformer geometries. Chapter 3 derives basic relations of an ideal transformer. Background details about extraction of all elements used in the equivalent-circuit are given. Chapter 4 shows several design examples. Simulation results are compared to measurement results. An excellent prediction accuracy is achieved.

Chapter 2

Design of Integrated Transformers

The design of monolithic lumped planar transformers is a demanding task. First the metallization of a semiconductor process, which defines the possibilities for transformer design, is considered. Planar and layer construction of common monolithic lumped transformers and its optimization techniques are presented in Sect. 2.2. A lumped low-order equivalent circuit, resulting from the transformer geometries, is derived in Sect. 2.3.

2.1 Silicon-based Technology and Metallization

The Metallization of a wafer is known as the wiring-layers, which are placed on the surface of the wafer. They are used to get a connection between the components of the circuit. The connection should have less resistance. In the case of a monolithic transformer, the winding construction consists of the metallization-layers. The metallization defines restrictions and possibilities. It is the working-area for monolithic transformer design.

The most common material for metal-layers is Aluminum (Al). It is a cheap material, inexpensive in production and has excellent characteristics against diffusion in silicon.

Nowadays some semiconductor-manufacturer are using copper as material for the metallization. Nearly the half resistance of aluminum stands in the opposite of a complex and costly semiconductor-process. INFINEON decided to use a Al-metallization for the standard process B6HFC.

The metallization forms the design environment for monolithic transformers. The layer construction fixes the design rules for transformer design. It sets the restrictions and affects the transformers characteristics. In order to get a good transformer design it is necessary to take advantage of all available possibilities of the metallization.

A simplified cross-section of the B6HFC-metallization is shown in Fig. 2.1. The B6HFC-Process consists of three metal layers, Alu1, Alu2 and Alu3. The conductor material is aluminum and has a conductivity of $\sigma = 33\,\mathrm{S}/\mu\mathrm{m}$. Every metal layer has a different height and a different minimal spacing between two conductors. The minimal spacing increases with each metal-layer and is a physical result of the semiconductor process. The metal layers are embedded in Silicondioxide SiO_2, which has a relative permittivity of $\varepsilon_r = 3.9$. The passivation is a airproof protection coat against dust, dirt and oxidation. It consists of Siliconnitride Si_3N_4 and has an $\varepsilon_r = 7.5$. The substrate is a p^--doted Silicon and is a mixture of conductor and dielectric. The thickness of the substrate-layer is about $200\,\mu$m. The high conductivity of $\sigma = 12.5\,\mathrm{S/m}$ is significant for the substrate loss, discussed in Section 3.3. The relative permittivity of the substrate is $\varepsilon_r = 11.9$.

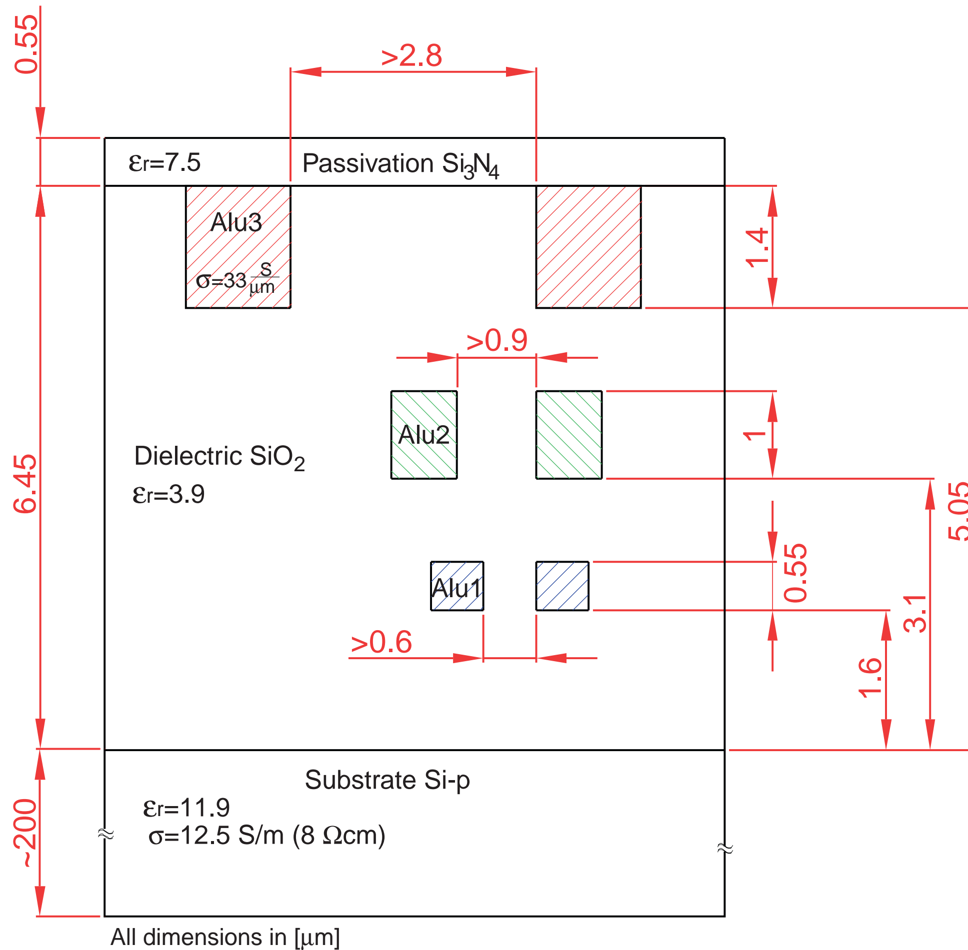

Figure 2.1: Schematic cross section of the B6HFC-metallization.

2.2 Transformer Construction

The goal of a design procedure for monolithic integrated transformers is to attain the desired frequency range with the lowest possible losses. Because of the complexities in modeling and analysis of these components, any change of the design should involve a simulation of the structure.

2.2.1 Basic Electrical Characteristics

Now some basic relations about transformers are explained. This relations will be needed to understand the design of monolithic integrated lumped planar transformers. Fig. 2.2 shows the schematic symbol of an ideal transformer with two coupled windings. In this work all variables shown in Fig. 2.2 are related to this figure if not noted differently.

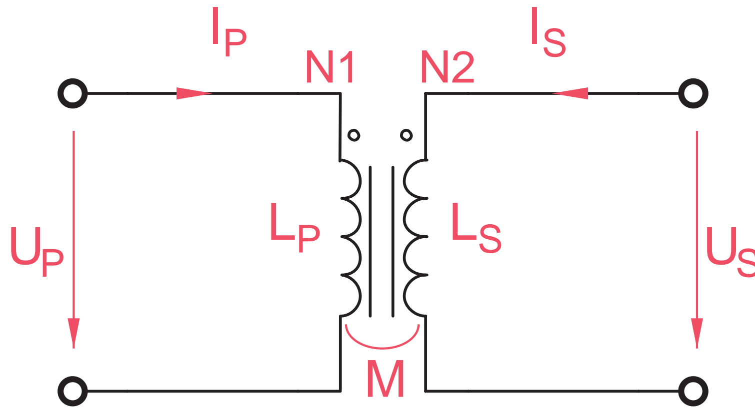

Figure 2.2: Schematic symbol of an ideal transformer with two windings.

A monolithic integrated planar transformer comprises two windings. Each winding consists of an integer number of turns $N1 \geq 1, N2 \geq 1$ where $N1$ is the number of primary turns and $N2$ is the number of secondary turns. The two windings are arranged in a single plane with conductors crossing one another.

The turn ratio n of a transformer is one of the main electrical parameters of interest and is defined as

$$n = \frac{N1}{N2} \tag{2.1}$$

In the case of an ideal transformer, the turn ratio n is also equivalent to

$$n = \frac{U_P}{U_S} = \frac{I_S}{I_P} \tag{2.2}$$

where U_P is the voltage between the primary ports, U_S is the voltage between the secondary ports. I_P and I_S is the current-flow into the related ports.

Each winding, the primary and the secondary, has a self-inductance L_P and L_S and they are inductively coupled denoted by the mutual-inductance M.

The strength of the magnetic coupling between the primary and secondary winding is indicated by the coupling coefficient k (k-factor) as

$$k = \frac{M}{\sqrt{L_P \, L_S}} \tag{2.3}$$

A typical range for the k-factor achieved in monolithic transformer designs is $0.6 \leq k \leq 0.95$.

A lumped transformer means that the maximum outer dimensions are smaller than the guided wavelength λ_g at the operation frequency f_{op}. This is expressed in the following unequation:

$$d_O \ll \lambda_g(f_{op}) \tag{2.4}$$

where d_O is the maximum outer dimension of the transformer.

Transformer Tuning

In many applications (i.e Input matching and interstage matching of a power amplifiers) a high current transfer ratio of the on-chip transformer is desired. In contrast to an ideal transformer the current transfer ratio of a lossy transformer is not equal to the value of the turn ratio. In this subsection a basic relation of the current transfer ratio of a lossy tuned transformer is derived.

Fig. 2.3 shows a secondary short-circuit transformer. It consists of a primary winding L_P and a secondary winding L_S. L_P and L_S are mutually coupled, denoted by the k-factor. In most cases the input impedance of the driver stage and the output stage is very low. Therefore, the secondary winding of the transformer in Fig. 2.3 is short-circuit, but without loss of generality. The ohmic loss of the primary winding L_P, ohmic loss the secondary winding L_S and the input impedance of the transistors (assumed real valued) are considered by the admittance G. The transformer is connected as a parallel resonant device using the capacitor C.

Then the resonant frequency ω_{res} of the tuned transformer can be derived as

$$\omega_{res} = \frac{1}{\sqrt{(1-k^2) \cdot C \cdot L_P}} \tag{2.5}$$

The quality factor Q of the resonant circuit is

$$Q = \frac{\omega_{res} \cdot C}{G} = \frac{1}{G} \cdot \sqrt{\frac{C}{(1-k^2) \cdot L_P}} \tag{2.6}$$

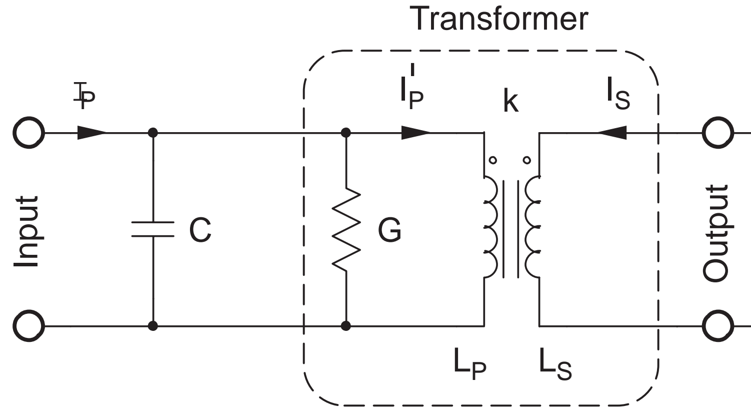

Figure 2.3: Tuned ideal transformer equivalent circuit [Simbürger 99].

The inner current transfer ratio of the ideal transformer is

$$\frac{I_S}{I'_P} = -k \cdot \sqrt{\frac{L_P}{L_S}} \tag{2.7}$$

Now the total current transfer ratio I_S/I_P of the parallel resonant transformer can be expressed by

$$\left|\frac{I_S}{I_P}\right| = k \cdot Q \cdot \sqrt{\frac{L_P}{L_S}} \tag{2.8}$$

This relation shows that in contrast to the untuned transformer, the total current transfer ratio can be increased by a quality factor of $Q > 1$.

2.2.2 Planar Winding Scheme

Monolithic transformers have been presented in various geometric designs and many different kinds have been realized. Some planar winding schemes for monolithic transformers are discussed in this section. The schemes are presented in simple example transformers.

Fig. 2.4(a) shows the winding scheme of a monolithic transformer with a turn ratio $n = 2 : 2$. Fig. 2.4(b) illustrates the physical layout of the circular-shaped planar transformer. The primary ports are located on the left side, the secondary ports are located on the right side. The two windings are separated from each other. The secondary winding starts at the radius r_{IS}, which is equal to the inner radius r_I of the transformer, and ends at the radius r_{OS}. The primary winding starts at the radius r_{IP} and ends at the radius r_{OP} which is equal to the outer radius r_O of the transformer. The winding scheme includes two cross-overs, one in the primary winding between the turns P1 and P2 and another one in the secondary winding between the turns S1 and S2. The transformer is completely symmetrical about a line. This design can be improved by several ways.

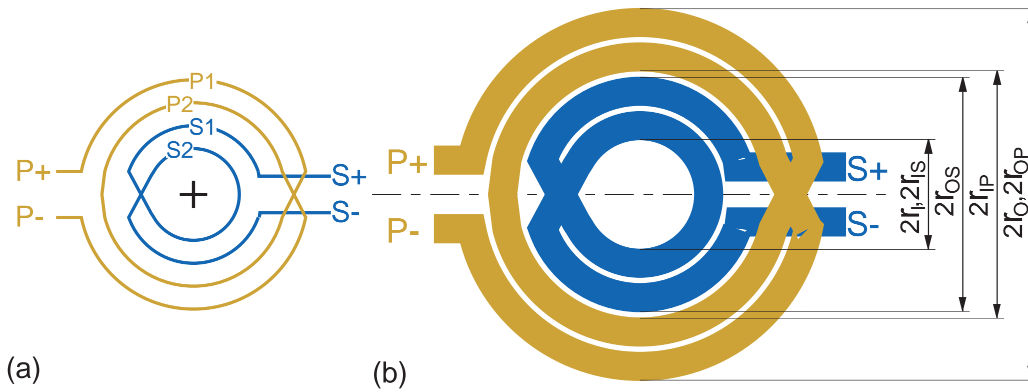

Figure 2.4: Circular-shaped monolithic lumped planar transformer with a turn ratio $n = 2:2$, (a)Winding Scheme (b) Physical layout

Adjacent Conductors

To maximize magnetic coupling between windings, adjacent conductors should belong to different windings. The mutual magnetic coupling between adjacent conductors that belong to the same winding increases self-inductance but not mutual inductance. It is clear from (2.3) that the k-factor is significantly lowered.

The circular-shaped transformer in Fig. 2.4 has not been optimized. Two primary turns are followed by two secondary turns which lowers the k-factor as mentioned before. In this case a interleaved winding scheme would help to increase magnetic coupling.

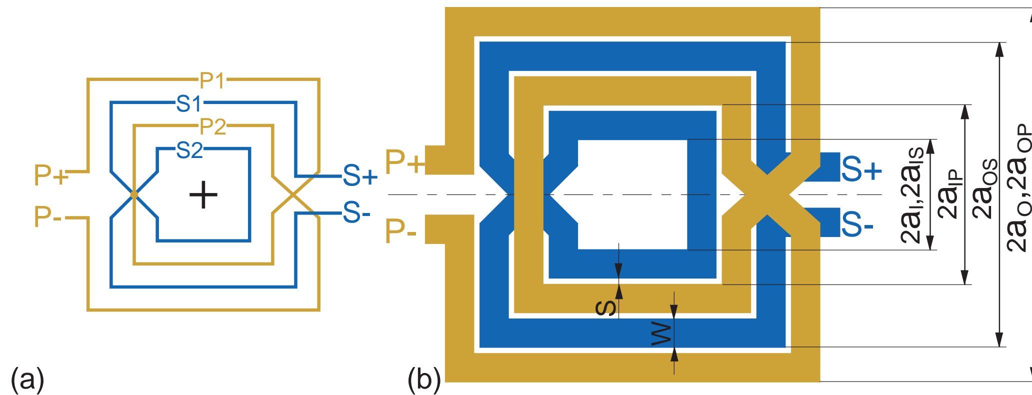

Figure 2.5: Square-shaped monolithic transformer with a turn ratio $n = 2:2$ and an interleaved scheme: (a)Winding Scheme (b) Physical layout

The square-shaped transformer in Fig. 2.5 has the same number of windings on primary and secondary side ($n = 2:2$) as the transformer shown in Fig. 2.4. The major difference between these two designs is the winding scheme. The

transformer is constructed with a interleaved winding scheme, which means primary turns are followed by secondary turns. This increases magnetic coupling between the windings and the coupling coefficient k. The winding scheme shown in Fig. 2.5(a) consists of two turns on each side and without loss of generality the scheme can be expanded with a number of more than two turns.

Interlaced Winding Scheme

To realize other values of the turn ratio than 1 different numbers of primary and secondary turns are used. This implements that some adjacent conductors belong to the same winding which results in a lower k-factor. A solution for this problem is to use a interlaced winding-scheme. One winding (e.g. the secondary) is sectioned into a number of individual turns rather than one continuous winding.

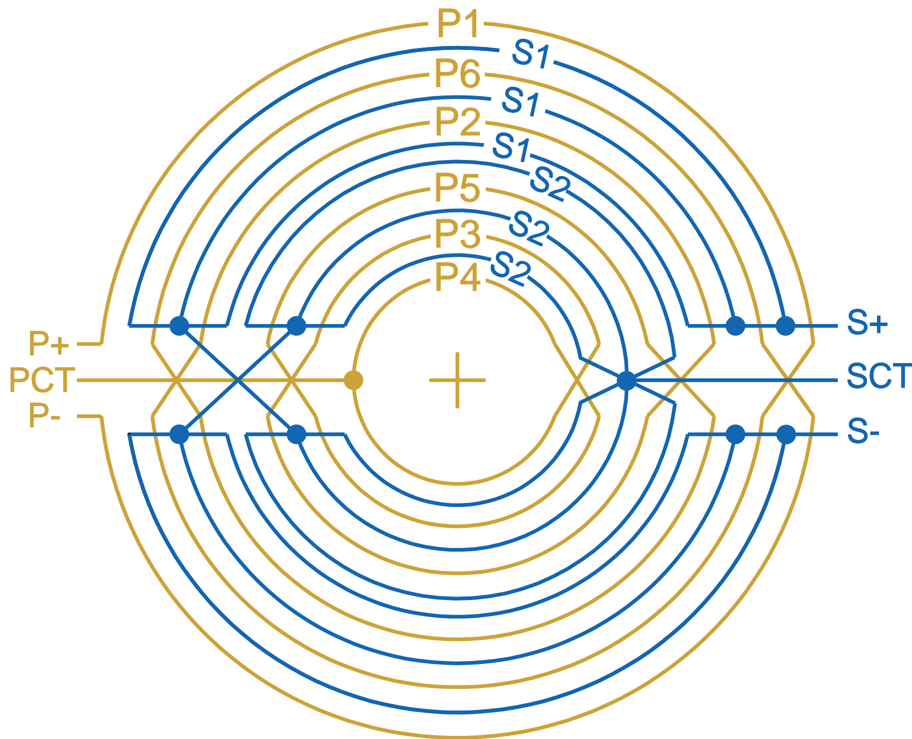

Figure 2.6: Interlaced winding scheme of a planar transformer with a turn ratio of $n = 6 : 2$.

Fig. 2.6 illustrates a interlaced winding scheme with a turn ratio of $n = 6 : 2$. The six primary turns (P1-P6) are connected in series. On the secondary side the three outer and the three inner turns are connected in parallel to form two groups (S1 and S2). The groups are connected in series to form two secondary turns. Six primary turns and two secondary turns result in a turn ratio of $n = 6 : 2$. Centertaps on the primary side PCT and on the secondary side SCT are available.

Ports Position

In many applications of monolithic integrated transformers it is desired to connect the primary ports at the left side and the secondary ports on the right side. The winding schemes presented before (Fig. 2.4, Fig. 2.5, Fig. 2.6) enable this demands. The groups of conductors are interconnected in a way which brings all terminals to the outside edge of the transformer layout.

In applications it is commonly required to use such transformers in balanced circuits, for which at least at one of the transformer winding a center tap exists. The midpoint (center tap) between the ports on each winding, can be located precisely at the inside edge. Because of the symmetric design, the center tap is optimally positioned, and the two halves of the winding are inductively and capacitively balanced for frequencies in a very broad range. All winding schemes presented before provides this symmetric design.

Square- and Circular-Shaped Transformers

Planar transformers can be constructed in square-shape or in circular shape. These two shapes of the planar transformer geometry are illustrated in Fig. 2.4(b) and Fig. 2.5(b). The main difference between these two shapes is the needed chip area.

Now a single circular-loop and square-loop shown in Fig. 2.7 is used as example to derive the relation between these two shapes. We want to assume the same perimeter, l_{Rect} and l_{Circle}, for each shape which is expressed in the following equation.

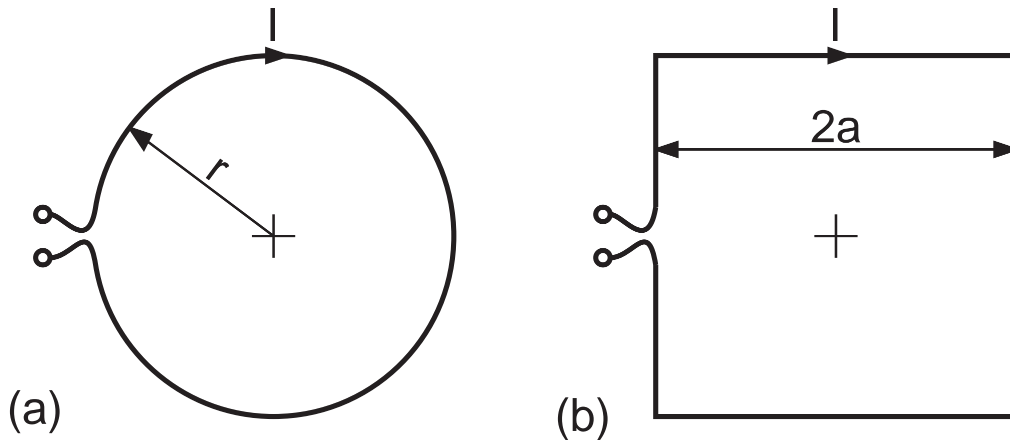

Figure 2.7: Single current-loop: (a) circular-shaped loop (b) square-shaped loop.

$$l_{Rect} = 8a \quad = \quad 2\pi r = l_{Circle}$$

$$a = \frac{\pi}{4} r \tag{2.9}$$

where a is the half side length of the square-shaped loop and r is the radius of the circular-shaped loop. In the case of a transformer all length are scaled with the factor $\pi/4$. The needed chip area of a square shaped transformer follows from (2.9) to

$$A_{Rect} = 4\,a_O^2 = 4\frac{r_O^2\pi^2}{16} = r_O^2\pi\frac{\pi}{4} = A_{Circle}\frac{\pi}{4} \tag{2.10}$$

where a_O is the half side length of a square-shaped transformer (Fig. 2.5) and r_O is the outer radius of a circular-shaped transformer (Fig. 2.4). (2.10) shows that the needed chip area for a square shape is only $\pi/4$ of the area of a circular shape with the assumption that $l_{Rect} = l_{Circle}$.

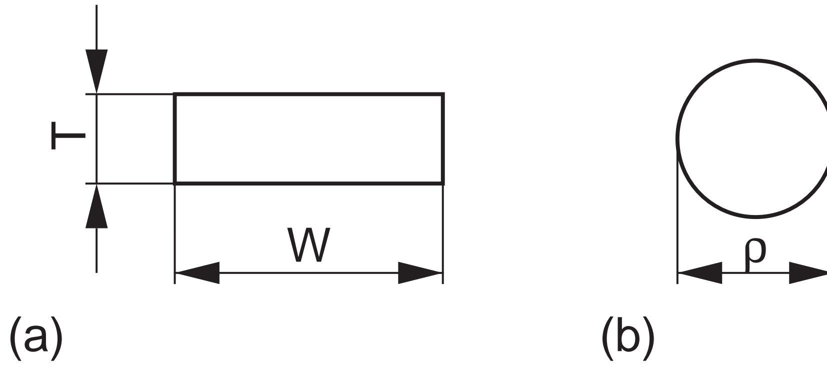

Figure 2.8: Conductor-Cross-Section: (a) Rectangular cross-section (b) Circular cross-section.

Now a basic relation of the self-inductance for a plane circular- and a square-loop is derived. The inductance-formulas [Grover 46] of any plane closed figure with perimeter l and radius ρ of the conductor's cross section have the general form

$$L = \frac{\mu_o}{2\pi} l \left[\ln\left(\frac{2l}{\rho}\right) - \alpha + \frac{\rho}{l} \right] \tag{2.11}$$

The constant α is characteristic for the figure and its shape. The value of α for square- and circular-shape was noted by [Grover 46] and is valid for a infinite thin wire. For a finite conductor cross section α have to be corrected with the geometric mean distance GMD of the conductor's cross section (Sect. 3.1). In the case of a rectangular conductor cross section the constant α for a circular- and square-shaped loop can be noted as

$$\begin{aligned} \alpha_{Rect} &= 2.854 + \ln 0.2235 = 1.356, \\ \alpha_{Circle} &= 2.452 + \ln 0.2235 = 0.954 \end{aligned} \tag{2.12}$$

Equation (2.11) is valid for conductors with negligible conductor height T which is not the case at monolithic transformers. So instead of the general inductance-formula for plane shapes a approximation based on (2.11) is used for the inductance calculation. The approximation was noted by [Wohlmuth 00].

$$L_{Rect} = \frac{\mu_o}{2\pi}8a\left[\ln\left(\frac{2}{W+T}\right)+\ln(8a)-1.356+\frac{W+T}{8a}\right] \quad (2.13)$$

$$L_{Circle} = \frac{\mu_o}{2\pi}2\pi r\left[\ln\left(\frac{2}{W+T}\right)+\ln(2\pi r)-0.954+\frac{W+T}{2\pi r}\right] \quad (2.14)$$

where T is the conductor height and W the conductor width, a is the half side length of the square-shaped loop and r is the radius of circular-shaped loop. In the case that $W+T \ll r$ and $W+T \ll a$ the last term in brackets is negligible. With this simplification and the assumption $l_{Rect} = l_{Circle}$ the ratio of the inductances can be written as

$$L_{Rect}/L_{Circle} = \frac{\ln\left(\frac{2l}{W+T}\right)-1.356}{\ln\left(\frac{2l}{W+T}\right)-0.954} \quad (2.15)$$

For a square and a circular shaped loop with the same length (2.15) shows a lower inductance for the square shape in a range of 5-15% for typical geometries. To get the same inductance of both shapes the rectangular loop must have a greater length.

In Fig. 2.9 a comparison of the needed chip area between circular-shaped and square-shaped loop is illustrated. The data plotted in Fig. 2.9 is valid for a single current loop in the two mentioned shapes and is a result of the numerical solution of (2.13) and (2.14) under the condition $L_{Rect} = L_{Circle}$. A circular loop with radius r, track width W and conductor height T needs a chip area of A_{Circle} to reach a certain inductance. A square loop with the same track width and conductor height needs a chip area of A_{Rect} to achieve the same inductance as the circular loop.

In the case of a transformer with a number of turns it is not possible to make a simple comparison. The simulation of the transformer design in both shapes is the best way to find the optimum. In fact the chip-area consumption of the square-shaped transformer in opposite to the circular shaped transformer is not that small as mentioned in (2.10). The ratio of the needed chip-area is always smaller than $\pi/4$ for reaching the same inductance. In some cases the required chip area of a circular-shaped transformer can be lower than a square shaped transformer.

Another disadvantage of the square shaped transformer are unsteady places in the geometries. The corners of the square represent a narrow place for the current. Additional losses are the consequences. In some cases a rectangular shape can be placed better on the chip than a circular shape.

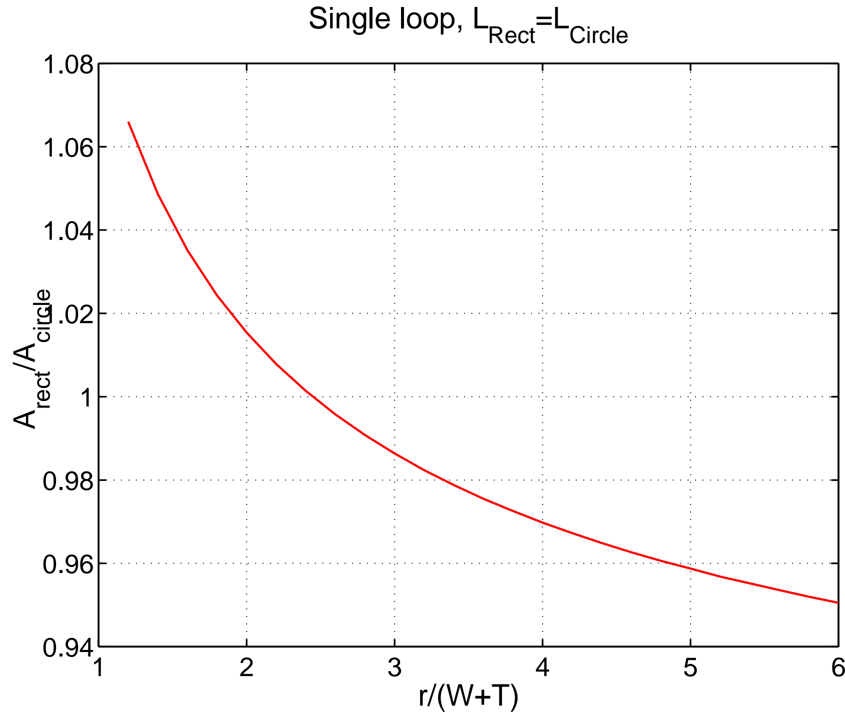

Figure 2.9: Comparison of needed chip area between circular- and square-loop with the same inductance.

Spacing between Conductors

The following steps are explained with the help of the simple example transformer shown in Fig. 2.5. To keep it simple, no center taps and only two turns for each winding are used. The top view shows the geometry parameters W which is the conductor-width of each turn, lateral spacing S between the turns, the inner and outer side length $2\,a_I$ and $2\,a_O$. The primary ports are located on the left side, the secondary ports on the right side.

Narrowly spaced conductors improve the magnetic and electric coupling between windings. The plot in Fig. 2.10 illustrates the k-factor of the example transformer as a function of the conductor-width W and different lateral spacings S. It shows that the transformer's k-factor improves when the spacing between the winding decreases, and therefore the smallest practical spacing should be used in the design. However, the high parasitic capacity between the windings must also be considered. The k-factor tends to a limiting value for a given spacing S. The data shown in Fig. 2.10 indicates that a design with a ratio of $W/S \approx 2$ is optimum.

The simulation was done with the transformer CAD-tool *FastTrafo*. *FastTrafo* was developed by the author and is partly based on two FEM-cores available from Massachusetts Institute of Technology called *FastHenry* [MIT 96] and *FastCap* [MIT 92].

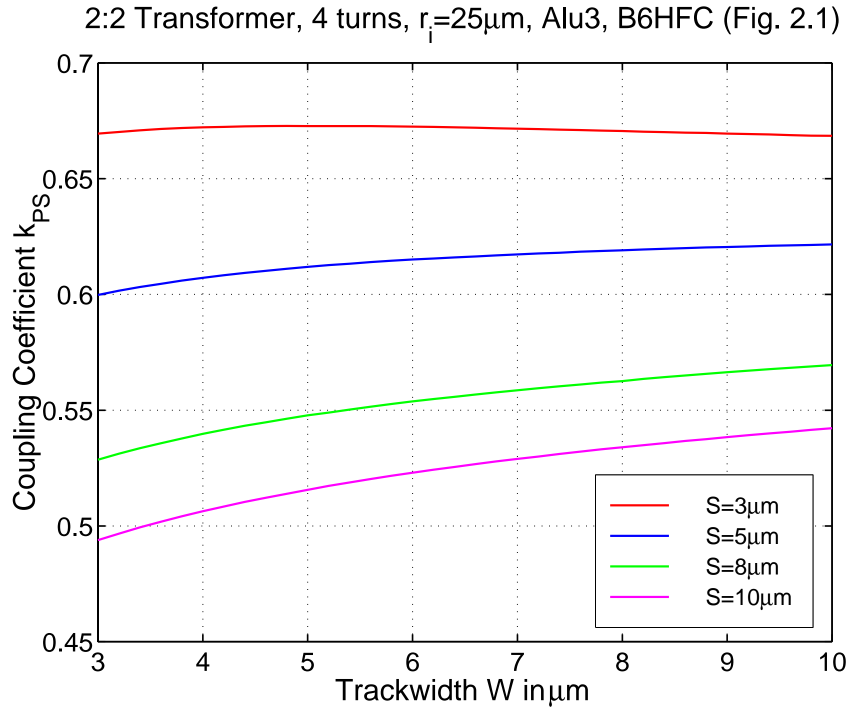

Figure 2.10: k-factor versus trackwidth of a $n = 2:2$ transformer (Fig. 2.5).

2.2.3 Metallization Structure

A closer look insight the transformer's geometric design is illustrated in Fig. 2.11. It shows the detailed layer construction of monolithic transformers, with primary- and secondary winding, different metal layers, cross-overs and VIA's. The transformer's characteristic depends also on the layer construction and process technology. Now a view possibilities to optimize the usage of the metallization for a monolithic transformer are discussed.

Multiple Layers

To reduce the ohmic loss it is possible to use multiple layers of metal to construct each winding. The different layers are connected in parallel with a number of small pins called "VIA". The cross section in Fig. 2.11 shows metal layer 3 in parallel with metal layer 2 for the primary winding and metal layer 1-3 in parallel for the secondary winding. Every half turn of the turns they are connected in parallel with VIA's. This results in reduced ohmic losses in the conductors and a lower insertion loss of the transformer. These losses modify the impedances seen at each port when the transformer is impedance matched to the source and load, and also contribute noise in the final circuit [Long 00]. The disadvantage of this possibility are the increasing parasitic capacities between the windings and the substrate.

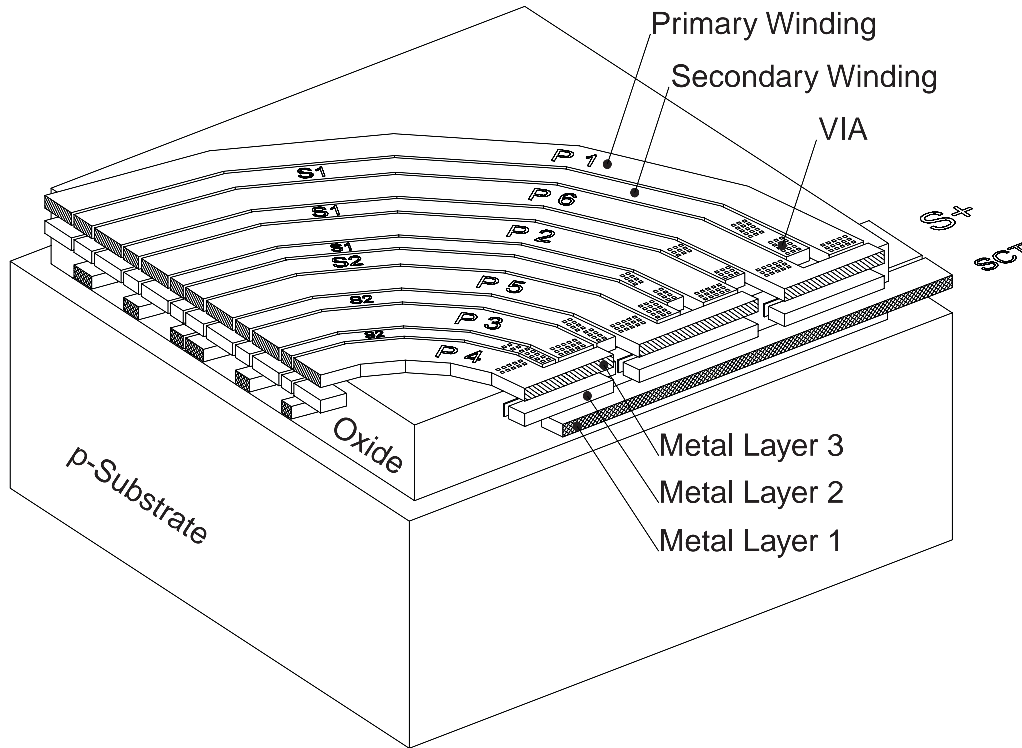

Figure 2.11: Cross section of an integrated transformer.

It was shown previously (Fig. 2.10) that the transformer's k-factor can be improved with varying the trackwidth W and spacing S. Another possibility to increase the k-factor is the usage of multiple layers. In Fig. 2.12 the k-factor of the example transformer shown in Fig. 2.5 is illustrated. The conductor-width W and the used metal layers are choosen to get the same cross-section-area and hence the series-resistance and the overall current-density for each case is nearly the same. The data from Fig. 2.12 shows that the k-factor can be improved significant by using multiple layers and lower conductor-width. The parasitic capacity to ground shown in Fig. 2.13 has also increased by using metal layer Alu1. So optimum in this case is to use Alu2 and Alu3. It shows the lowest parasitic capacity to ground and an improved k-factor. The data from Fig. 2.12 and Fig. 2.13 was generated with *FastTrafo*.

Overlay Coupled Transformers

A monolithic planar transformer is constructed using conductors interwound in the same plane. Another possibility to construct a transformer is to use conductors overlaid as stacked metal. The planar transformer which have the conductors in the same plane is a edge or horizontally coupled transformer. The second kind which have stacked conductors is a overlay or broadside coupled transformer. The

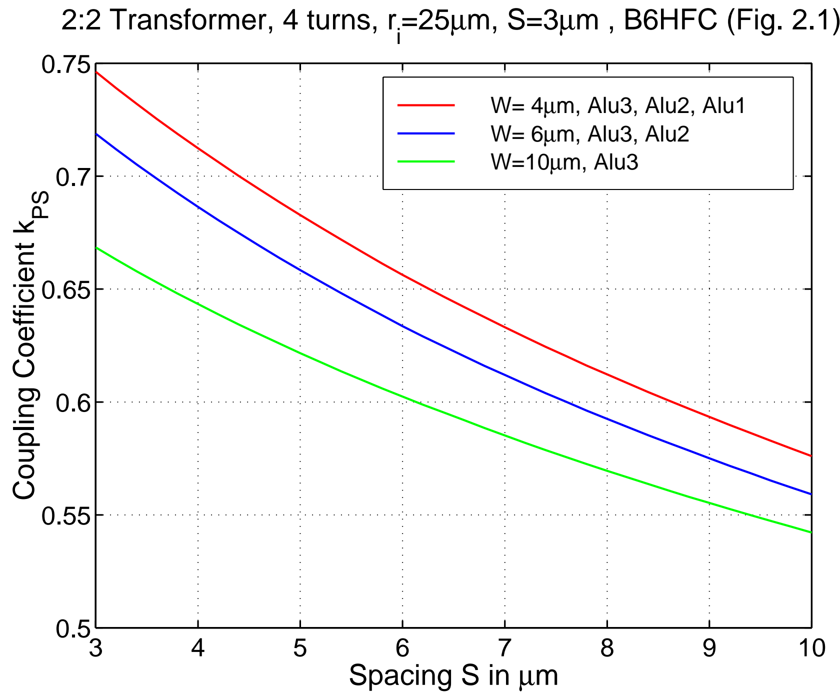

Figure 2.12: k-factor of transformer with different numbers of metal layer.

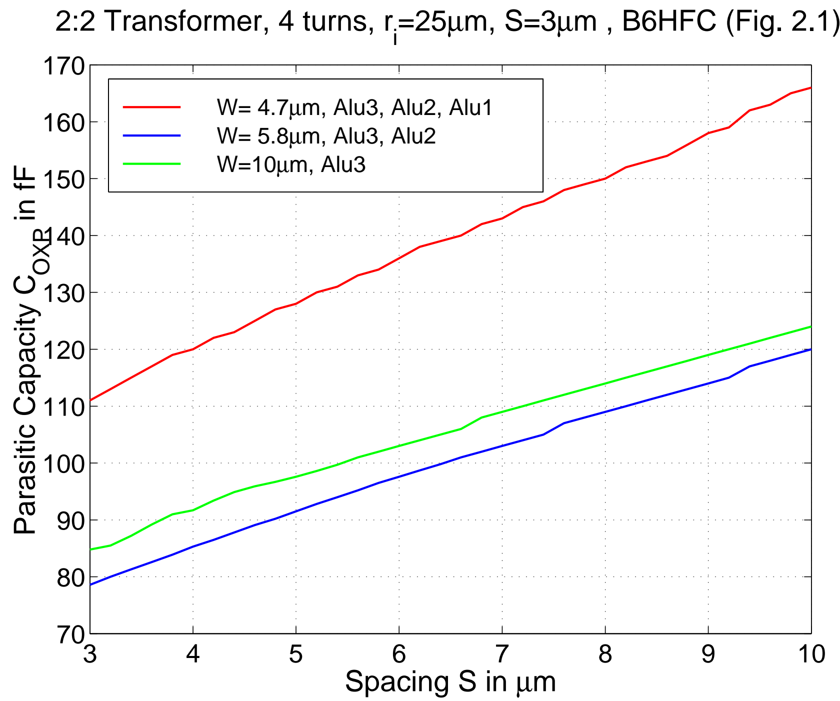

Figure 2.13: Parasitic capacity from primary winding to ground.

advantage of overlaying the windings compared to the planar transformer is that approximately one-half of the chip area is required. The main disadvantage of broadside coupled transformers is a large parallel-plate component to the capacitance between windings due to the overlapping of metal layers, which limits the frequency response. Multiple layers must be shared between the secondary and primary winding to construct the windings , follows a higher ohmic loss. Also, a symmetric design can not be performed, which involves all disadvantages of non-symmetric designs.

The better performance of planar transformers is the reason why only this kind is explained in this work.

Summary of Design Rules

Many aspects of design possibilities have been presented in this chapter. The discussed design rules are valid for the general design of monolithic transformers. The final circuit design depends on the desired electrical characteristics and can differ from the presented design techniques. The designer is able to optimize a lot of parameters in order to make an intelligent design compromise.

A highly optimized circular-shaped monolithic transformer which is used in the power amplifier mentioned in Chapter 1 (Fig. 1.1) is presented in Sect. 4.1. A three dimensional top view of the transformer is shown in Fig. 4.2.

Now lets make a short summery about optimization techniques for monolithic integrated lumped transformers:

- Use **narrowly spaced conductors** to improve the magnetic coupling between windings.
- If possible use a **trackwidth to spacing ratio** of $W/S \approx 2$ for your design.
- **Adjacent conductors** should belong to **different windings**.
- Use a **interlaced winding-scheme** for reaching the desired turn ratio.
- Use **multiple layers of metal** to reduce the ohmic loss.
- Check the performance of **circular and square shape design**.

2.3 Transformer Model

The complete electrical behavior of a monolithic integrated lumped transformer cannot be accurately predicted from closed-form equations. A alternative for design and optimization is a lumped-element equivalent circuit. The aim of precise and fast transient analysis of RF circuits using monolithic transformers was

reached with a compact lumped low order model. The complexity of this model is low enough and the precision is high enough to perform fast and accurate analysis of the integrated circuits.

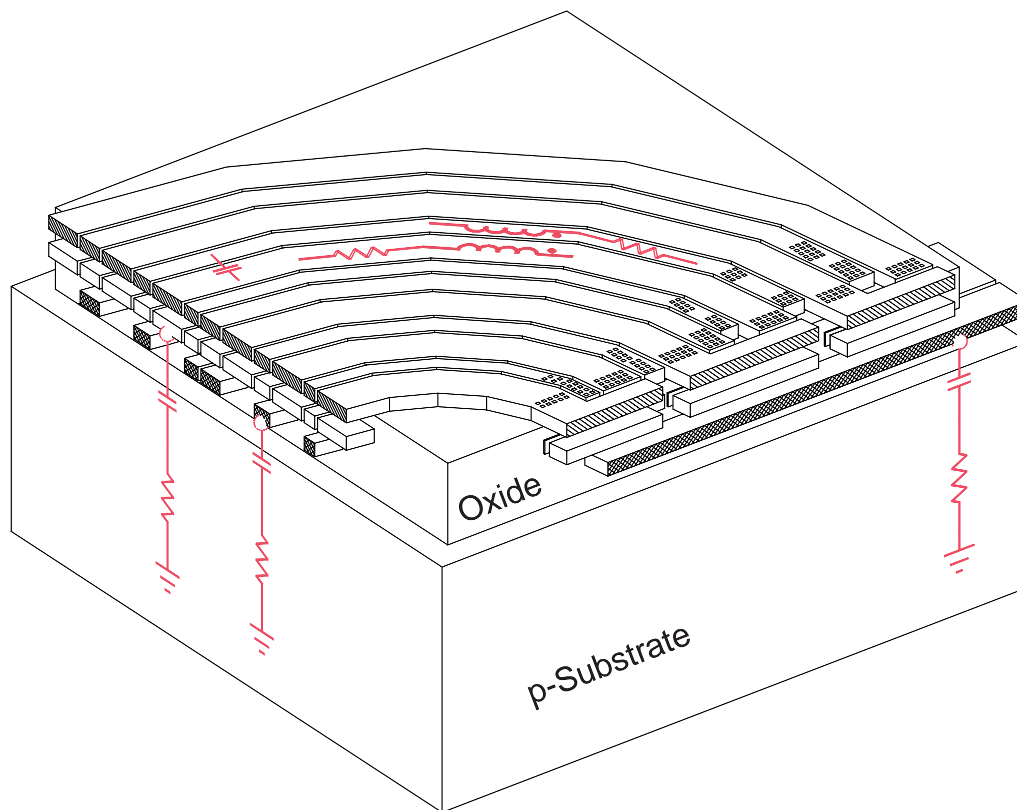

Figure 2.14: Three dimensional cross section of a transformer with basic model elements.

An electrical model of a transformer can be derived from the physical layout and process technology. Fig. 2.14 shows a cross-section of a monolithic integrated lumped transformer. The circuit devices illustrated in the figure are the basic elements of the equivalent circuit and can be identified as:

- Multiple coupled inductors of the windings.
- Ohmic loss in the conductor material due to skin effect, current crowding and finite conductivity.
- Parasitic capacitive coupling between the windings.
- Parasitic capacitive coupling into the substrate.
- Losses in the conductive substrate.

Lumped 16-element Model

With this basic elements a lumped low-order equivalent model was constructed. The model shown in Fig. 2.15 can be used directly in a time-domain circuit simulation (i.e. SPICE).

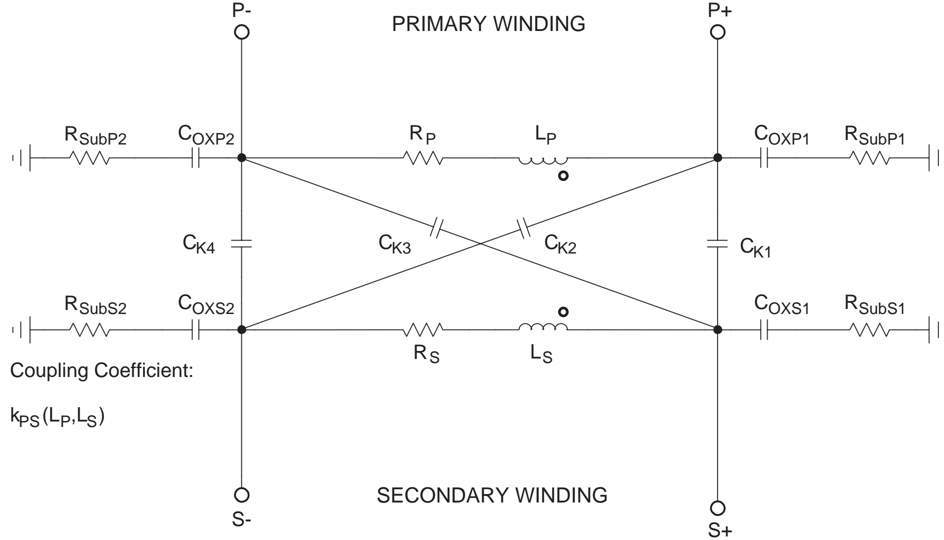

Figure 2.15: Basic equivalent circuit of the transformer without center taps.

Self inductance of the conductors are modeled by components L_P for the primary winding and L_S for the secondary winding. The inductances are coupled mutually denoted by the coupling coefficient k_{PS}.

Ohmic loss in the conductor material due to skin effect, current crowding and finite conductivity is modeled by components R_P for the primary winding and R_S for the secondary winding.

The parasitic capacitive coupling between primary and secondary winding is modeled by components C_{K1}, C_{K2}, C_{K3} and C_{K4}. The sum of all four capacities is equivalent to the static capacity between primary and secondary winding and can be measured between primary and secondary port. The capacities C_{K2} and C_{K3} placed across the windings model the capacity between the individual turns of each winding.

The parasitic capacitive coupling into the substrate is modeled by components C_{OXP1}, C_{OXP2} for the primary winding and C_{OXS1}, C_{OXS2} for the secondary winding. The sum of the capacities for each winding is the static capacity to the substrate.

The losses in the conductive substrate are modeled by components R_{SubP1}, R_{SubP2} for the primary winding and R_{SubS1}, R_{SubS2} for the secondary winding.

Expanded Lumped 24-element Model

In applications it is commonly required to use such transformers in balanced circuits, for which at least at one of the transformer windings a center tap exists. The equivalent circuit in Fig. 2.15 shows the case without center taps. This model can be expanded to include center taps. Fig. 2.16 shows the expanded model with primary and secondary center taps.

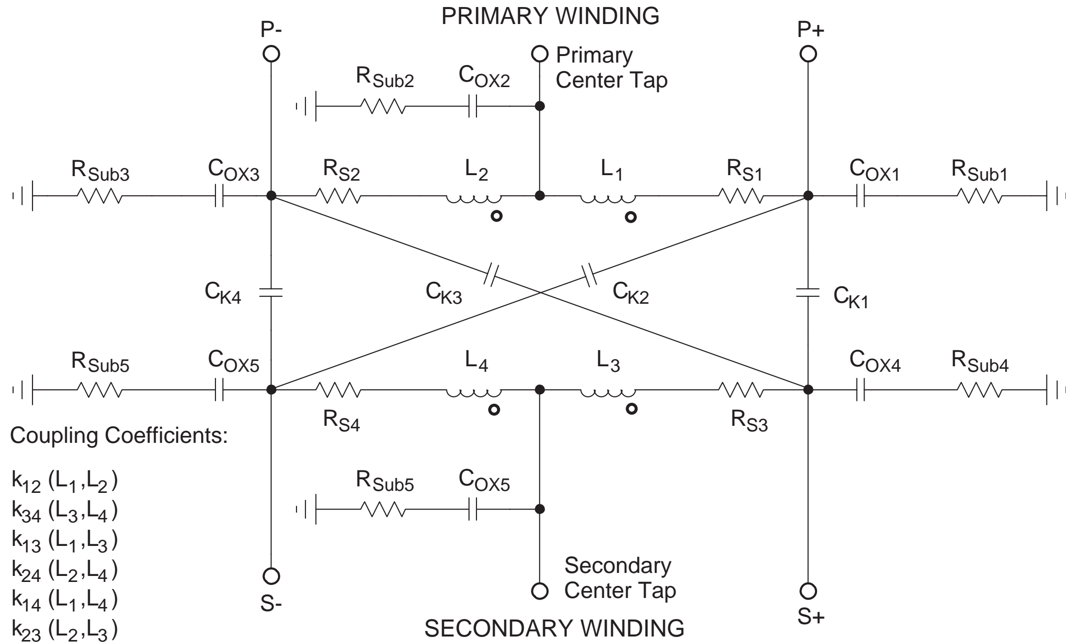

Figure 2.16: The Lumped-Equivalent-Circuit of the transformer [Simbürger 99].

Self inductance of the conductors are splitted into components L_1, L_2 for the primary winding and L_3, L_4 for the secondary winding. Each inductance is coupled mutually with every other inductance, denoted by the coupling coefficients $k_{12}, k_{34}, k_{13}, k_{24}, k_{14}$ and k_{23}. Note that the problem increases to a multiple coupled inductors problem.

Ohmic losses in the conductor material due to skin effect, current crowding and finite conductivity are splitted into R_{S1}, R_{S2} for the primary winding and R_{S3}, R_{S4} for the secondary winding.

The parasitic capacitive coupling between primary and secondary winding is modeled by components C_{K1}, C_{K2}, C_{K3} and C_{K4}. The capacities C_{K2} and C_{K3} placed across the windings model the capacity between the individual turns of each winding. C_{K2} and C_{K3} also describe the different cases of operation (i.e. primary center tap or primary port P- grounded).

The parasitic capacitive coupling into the substrate is modeled by components C_{OX1}, C_{OX2} and C_{OX3} for the primary winding and C_{OX4}, C_{OX5}, and C_{OX6} for

the secondary winding. The sum of the capacities for each winding is the static capacity to the substrate. The division into three capacities on each side is again the modeling for different operation cases.

The losses in the conductive substrate are modeled by components R_{Sub1}, R_{Sub2} and R_{Sub3} for the primary winding and R_{Sub4}, R_{Sub5}, and R_{Sub6} for the secondary winding. The substrate-resistance is distributed into three resistors for each winding.

Conversion from the 24-element to the 16-element Model

The equivalent circuit shown in Fig. 2.16 can be reduced to the model shown in Fig. 2.15. The relation between these two models and its parameters is derived in the following equations.

The inductance values L_P and L_S can be calculated with the following equations.

$$L_P = L_1 + L_2 + 2\,M_{12} = L_1 + L_2 + 2\,k_{12}\,\sqrt{L_1\,L_2} \tag{2.16}$$

$$L_P = L_3 + L_4 + 2\,M_{34} = L_3 + L_4 + 2\,k_{34}\,\sqrt{L_3\,L_4} \tag{2.17}$$

The coupling coefficient k_{PS} can be calculated to

$$k_{PS} = \frac{k_{13}\,\sqrt{L_1\,L_3} + k_{14}\,\sqrt{L_1\,L_4} + k_{23}\,\sqrt{L_2\,L_3} + k_{24}\,\sqrt{L_2\,L_4}}{\sqrt{L_P\,L_S}} \tag{2.18}$$

The series resistance of the windings follow as

$$\begin{aligned} R_P &= 2\,R_{S1} = 2\,R_{S2} \\ R_S &= 2\,R_{S3} = 2\,R_{S4} \end{aligned} \tag{2.19}$$

The substrate resistances R_{Sub} are converted to

$$\begin{aligned} R_{SubP1} = R_{SubP2} = R_{Sub1}/2 \\ R_{SubS1} = R_{SubS2} = R_{Sub4}/2 \end{aligned} \tag{2.20}$$

The parasitic oxid capacities C_{OX} follow as

$$\begin{aligned} C_{OXP1} = C_{OXP2} = 2\,C_{OX1} \\ C_{OXS1} = C_{OXS2} = 2\,C_{OX4} \end{aligned} \tag{2.21}$$

The parasitic capacitive coupling between the windings, denoted by C_K, is the same in both models.

Validity of the Transformer Model

The transformer models presented in Sect. 2.3 result in fast and accurate analysis of the integrated circuits. The complexity of the equivalent models are low enough and the precision is high enough for accurate simulation of the electrical characteristics. In Chapter 4 the measurement is compared to the simulation results of two design examples. It shows in details the accuracy of the presented transformer model.

In general the transformer model is valid down to DC. Normally monolithic transformers have operating frequencies in the GHz-range and hence the DC-case is not of interest. When biasing primary and secondary side on different levels the validity of the DC-case is helpful and necessary.

The upper frequency limit of the model depends on the transformer geometry. As shown previously in Sect. 2.2 the unequation (2.4) must be fulfilled for valid simulation results. The maximum operating frequency of the transformer in typical applications is about 2/3 times of the self resonant frequency. In most cases the upper limit of the model is about 3/2 times the self resonant frequency of the transformer.

Chapter 3

Parameter Extraction

The lumped low-order equivalent model considered in Sect. 2.3 describes the electrical behavior of a monolithic integrated lumped transformer. This chapter gives the background details about extraction of all elements used in the equivalent-circuit. In Sect. 3.1 the inductance of transformers built up from straight conductors is derived. The losses in the conductors due to skin effect and current crowding are derived in Sect. 3.2. The conductive substrate causes additional losses treated in Sect. 3.3. In Sect. 3.4 some thesis about the parasitic capacitive coupling between the windings and the substrate are presented. Finally test structures for the measurement are presented.

3.1 Inductance Calculation

Inductance extraction is based on Maxwell's Equations

$$\vec{\nabla} \times \vec{H} = \vec{J} + \partial_t \vec{D} \tag{3.1}$$

where $\vec{H}$ is the magnetic field quantity, $\vec{J}$ is the current density and $\vec{D}$ is the electric flux density.

Now we apply the magnetoquasistatic assumption. The frequencies of interest will be considered small enough such that the displacement current in (3.1) can be neglected.

$$\vec{\nabla} \times \vec{H} = \vec{J} \tag{3.2}$$

This assumption is clearly justified within the conductors where the conductivity is large. From the Ampere-Maxwell-Law (3.1) in magnetoquasistatic case (3.2) is it possible to derive the known formulas of self-inductance L and mutual-inductance M for two current loops [Smythe 68].

$$L = \mu \oint \oint \frac{1}{4\pi r} \mathrm{d}\vec{\mathbf{s}} \, \mathrm{d}\vec{\mathbf{s}} \tag{3.3}$$

$$M = \mu \oint \oint \frac{1}{4\pi |\vec{\mathbf{r}}_1 - \vec{\mathbf{r}}_2|} \, \mathrm{d}\vec{\mathbf{s}}_1 \, \mathrm{d}\vec{\mathbf{s}}_2 \tag{3.4}$$

The mutual-inductance formula (3.4) is known as the *Neumann Formula*. The integration is round of two current loops. In most cases it exist a closed-form equation of (3.4).

The self-inductance formula is mathematical more expensive and only in a view cases exist a closed-form equation. The self-inductance of a loop is the mutual inductance to itself.

Now we start the calculation of the basic element, a straight conductor, and will end at a transformer. The derivation based on (3.4) of the following formulas is not executed in this work. The basic formulas are already noted in [Grover 46] and [Greenhouse 74].

Mutual Inductance of Two Parallel Filaments

The mutual inductance of two parallel filaments with equal length is the basic case for the treatment of circuits made up of parallel elements. The inductance-calculation of circuits made up of straight elements of negligible cross section (filaments) have been solved and it exists a closed-form equation of (3.4).

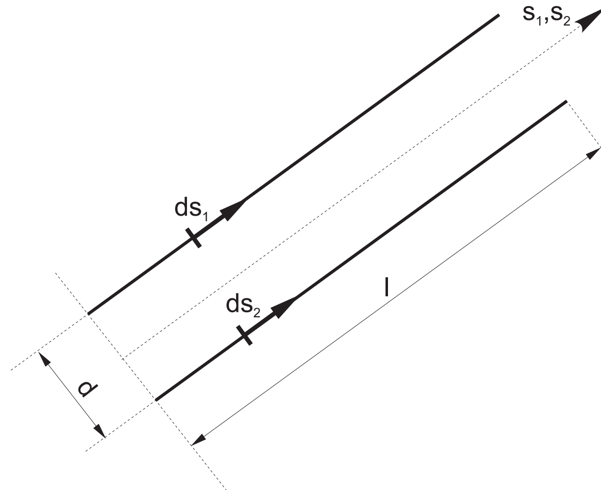

Figure 3.1: Parallel conductor elements with same length

Assuming the lengths of the filaments in Fig. 3.1 to be l and their distance apart d the exact formula for the mutual inductance is

$$M = \frac{\mu_o}{2\pi}\, l \left[\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}}\right) - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l} \right] \tag{3.5}$$

If $l \gg d$ a better way is to make a row expansion of (3.5)

$$M = \frac{\mu_o}{2\pi}\, l \left[\ln\frac{2\,l}{d} - 1 + \frac{d}{l} - \frac{1}{4}\frac{d^2}{l^2} \cdots \right] \tag{3.6}$$

The mutual inductance is dominated by $\ln(2l/d)$ and with the assumption that $l \gg d$ some terms are negligible.

Geometric Mean Distance GMD

In calculating the mutual inductance of two conductors whose cross sectional dimensions are small compared to their distance, the formulas above are valid. The mutual inductance is sensibly the same as the mutual inductance of filaments along their axes.

A monolithic integrated transformer consists of conductors with a rectangular cross sections with non-negligible dimensions. In typical transformer designs the spacing S between two turns is smaller than the conductor-width W of the conductors. The cross-section dimensions of the conductors are to large to justify the simplification made above. To use the formulas for calculating the inductance of monolithic transformers they must be corrected. The basic formula (3.5) for the mutual inductance must be integrated over the cross sections of the conductors. The structure of the formula (3.5) is maintained, in fact only the distance d is replaced by the corrected distance d_{GMD}, called geometric mean distance.

The geometric mean distance GMD between two conductors is the distance between two infinitely thin filaments whose mutual inductance is equal to the mutual inductance between the two original conductors. More about the GMD and many tables with the GMD for different cross sections can be found at [Grover 46].

In the case of monolithic integrated transformers a rectangular conductor cross section is used. Fig. 3.2 illustrates two parallel conductor elements with rectangular cross section and its dimensions.

The corrected distance d_{GMD} between the conductors in Fig. 3.2 for inductance calculation follows as

$$d_{GMD} = d\, e^k \tag{3.7}$$

where k is the correction factor listed in Table 3.1.

With the use of the geometric mean distance d_{GMD} the basic equation (3.6) for two parallel filaments follows to

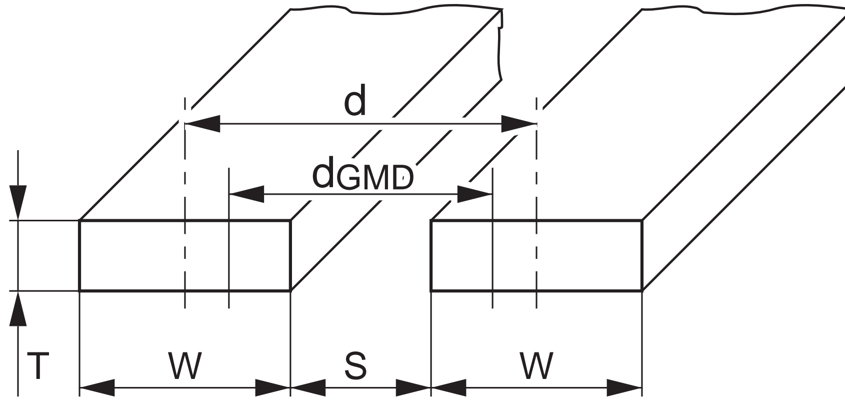

Figure 3.2: Parallel conductor elements with rectangular cross section.

W/d	T/W=0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0	0	0	0	0	0	0	0	0	0	0	0
0.05	-0.0002	-0.0002	-0.0002	-0.0002	-0.0002	-0.0002	-0.0001	-0.0001	-0.0001	-0.0000	0.0000
0.10	-0.0008	-0.0008	-0.0008	-0.0008	-0.0007	-0.0006	-0.0005	-0.0004	-0.0003	-0.0002	0.0000
0.15	-0.0019	-0.0019	-0.0018	-0.0017	-0.0016	-0.0014	-0.0012	-0.0010	-0.0006	-0.0003	0.0000
0.20	-0.0034	-0.0033	-0.0032	-0.0030	-0.0028	-0.0025	-0.0021	-0.0017	-0.0012	-0.0006	0.0000
0.25	-0.0053	-0.0052	-0.0051	-0.0048	-0.0044	-0.0039	-0.0034	-0.0027	-0.0019	-0.0010	0.0000
0.30	-0.0076	-0.0076	-0.0073	-0.0069	-0.0064	-0.0057	-0.0048	-0.0038	-0.0027	-0.0014	0.0001
0.35	-0.0105	-0.0104	-0.0100	-0.0095	-0.0087	-0.0078	-0.0066	-0.0052	-0.0036	-0.0018	0.0002
0.40	-0.0138	-0.0136	-0.0132	-0.0125	-0.0115	-0.0102	-0.0086	-0.0068	-0.0047	-0.0024	0.0002
0.45	-0.0176	-0.0174	-0.0169	-0.0159	-0.0146	-0.0130	-0.0110	-0.0086	-0.0059	-0.0029	0.0003
0.50	-0.0220	-0.0217	-0.0210	-0.0198	-0.0182	-0.0161	-0.0136	-0.0106	-0.0073	-0.0036	0.0005
0.55	-0.0269	-0.0266	-0.0257	-0.0243	-0.0222	-0.0197	-0.0164	-0.0128	-0.0087	-0.0042	0.0007
0.60	-0.0325	-0.0321	-0.0310	-0.0292	-0.0267	-0.0235	-0.0196	-0.0152	-0.0103	-0.0048	0.0010
0.65	-0.0388	-0.0383	-0.0369	-0.0347	-0.0316	-0.0277	-0.0231	-0.0178	-0.0120	-0.0055	0.0014
0.70	-0.0458	-0.0452	-0.0435	-0.0408	-0.0370	-0.0324	-0.0269	-0.0207	-0.0137	-0.0062	0.0019
0.75	-0.0536	-0.0529	-0.0509	-0.0476	-0.0431	-0.0375	-0.0310	-0.0237	-0.0156	-0.0070	0.0023
0.80	-0.0625	-0.0616	-0.0591	-0.0551	-0.0497	-0.0431	-0.0354	-0.0269	-0.0176	-0.0075	0.0031
0.85	-0.0725	-0.0714	-0.0683	-0.0634	-0.0569	-0.0491	-0.0401	-0.0302	-0.0195	-0.0081	0.0037
0.90	-0.0839	-0.0825	-0.0786	-0.0726	-0.0648	-0.0555	-0.0451	-0.0337	-0.0216	-0.0087	0.0046
0.95	-0.0973	-0.0954	-0.0903	-0.0828	-0.0734	-0.0625	-0.0504	-0.0374	-0.0236	-0.0092	0.0056
1.00	-0.1137	-0.1106	-0.1037	-0.0942	-0.0828	-0.0700	-0.0561	-0.0413	-0.0258	-0.0098	0.0065

Table 3.1: Correction factor k of (3.7) for rectangular cross section with W/d and T/W [Grover 46].

$$M = \frac{\mu_o}{2\pi}\; l\; \left[\ln \frac{2\,l}{d_{GMD}} - 1 + \frac{d_{GMD}}{l} - \frac{1}{4}\frac{d_{GMD}^2}{l^2}\cdots\right] \tag{3.8}$$

Mutual Inductance of Unequal Parallel Conductors

Two filaments of lengths l_j and l_m are separated by a distance d. The situation is illustrated in Fig. 3.3.

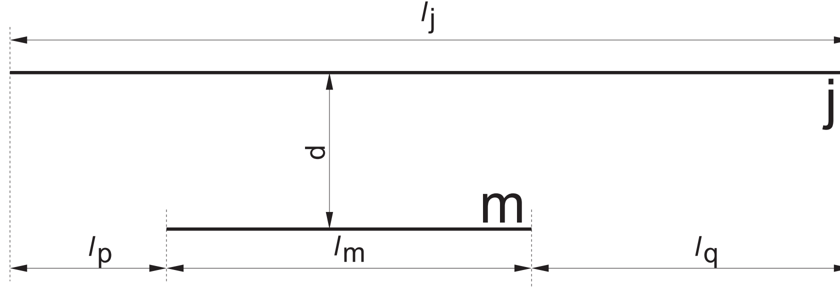

Figure 3.3: Parallel conductor filaments with different length.

The mutual inductance between conductor j and m can be calculated as

$$M_{j,m} = \frac{1}{2}\left[M(l_m + l_p) + M(l_m + l_q) - M(l_p) - M(l_q)\right] \tag{3.9}$$

where the individual M-terms are calculated using the basic formula (3.6). For conductors with rectangular cross section use the distance d_{GMD} derived in (3.7). Formula (3.9) applies the laws of summation of mutual inductances and is based on the case of equal parallel filaments.

In the case of $l_p = l_q$ (3.9) simplifies to

$$M_{j,m} = M(l_m + l_p) - M(l_p) \tag{3.10}$$

for $l_p = 0$,

$$M_{j,m} = \frac{1}{2}\left[M(l_j) + M(l_m) - M(l_q)\right] \tag{3.11}$$

Other more general expressions (i.e. filaments inclined at an angle to each other) are available in [Grover 46], we will limit ourselves for purposes of this work to the noted relationships.

Self Inductance of a Straight Conductor

The self inductance of a straight conductor is an included case in the mutual inductance of two parallel equal conductors. The self inductance is the mutual inductance to itself.

Based on (3.8) the self inductance of a straight conductor with rectangular cross section and constant current density was noted by [Greenhouse 74] and can be written as

$$L = \frac{\mu_o}{2\pi} l \left[\ln\left(\frac{2l}{W+T}\right) + 0.50049 + \frac{W+T}{3l}\right] \tag{3.12}$$

where l is the length of the conductor, W the width and T the height of the rectangular cross section.

Inductance Calculation of Monolithic Transformers

Transformers composed of straight conductors can be treated with the summation of self- and mutual-inductances of the individual conductor elements. The calculation procedure will be explained with the help of the transformer presented in Fig. 2.5. The layout of the transformer is illustrated in Fig. 3.4. The transformer has a turn ratio of $n = 2 : 2$. For the inductance calculation the primary winding is divided into $n_P = 11$ individual conductors numbered from 1-11. The secondary winding is divided into $n_S = 11$ individual conductors numbered from 12-22.

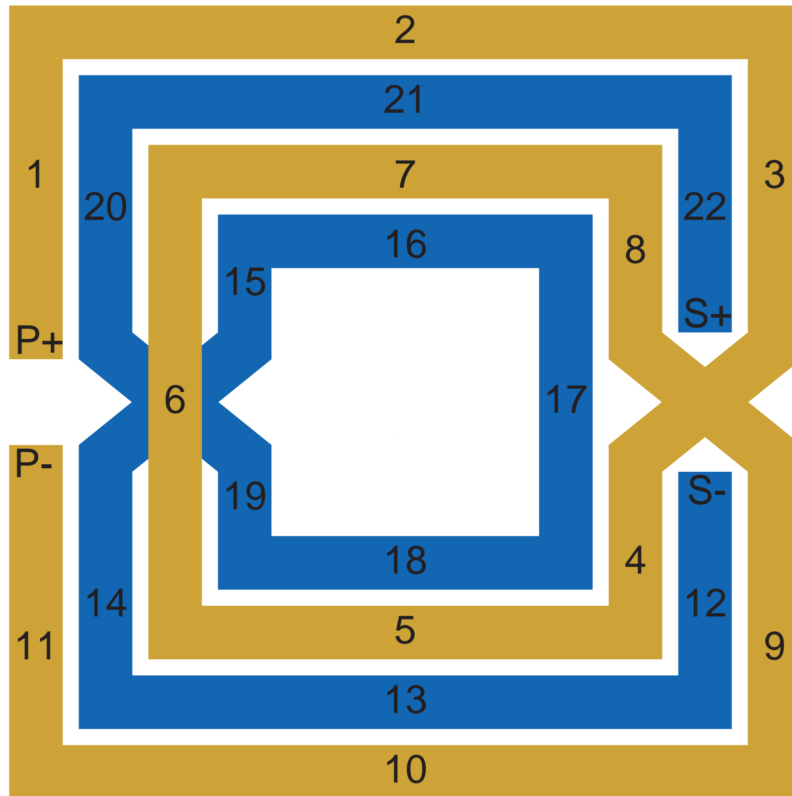

Figure 3.4: Square-shaped monolithic transformer with a turn ratio of $n = 2 : 2$.

For the self inductance calculation of the individual conductors L_i equation (3.12) is used. The self inductance of the primary- L_P and secondary-winding L_S is the sum of all self inductances of the conductors L_i plus the sum of the mutual inductances of every conductor to every conductor $M_{i,k}$. The complete self inductance

of the windings can be written as

$$L_P = \sum_{i=1}^{n_P} L_i + 2 \sum_{i=1}^{n_p-1} \sum_{k=i+1}^{n_P} M_{i,k} \tag{3.13}$$

$$L_S = \sum_{i=n_P+1}^{n_P+n_S} L_i + 2 \sum_{i=n_P+1}^{n_P+n_S-1} \sum_{k=i+1}^{n_p+n_S} M_{i,k} \tag{3.14}$$

where i, k are the numbers of the individual conductors (i.e. For the secondary winding in Fig. 3.4 the conductor numbers are $i = 12 \dots 22$).

The mutual inductance M between the two windings is the sum of the mutual inductances of every primary conductor to every secondary conductor. The complete mutual inductance between the windings can be written as

$$M = \sum_{i=1}^{n_P} \sum_{k=n_P+1}^{n_P+n_S} M_{i,k} \tag{3.15}$$

The summation indices are again the numbers of individual conductors. The mutual inductance of the element $M_{i,k}$ is calculated with (3.8) or (3.9).

The presented method is realized in *FastTrafo* which uses the FEM-core *FastHenry* [MIT 96] for inductance calculation. The whole transformer geometry built up of straight conductors is the input to the FEM-core. The exact modeling of the planar construction is an important task for an accurate inductance extraction. The exact modeling of the layer construction is less important.

Fig. 3.5 shows the simulation of the self inductance as a function of primary turns. The device under test is the transformer *BL62S005* which is presented in Sect. 4.1. The data plotted in Fig. 3.5 was extracted with *FastTrafo*. The inductance is proportional to $N^{1.9}$, in theory it is proportional to N^2. The plot in Fig. 3.5 shows both curves. The simulation shows clearly the five cross-over sections of the primary winding.

3.2 Skineffect and Current Crowding

At radio frequencies the penetration of current and magnetic field into the surface of conductors tends only to a limited depth. If the thickness of a conductor is much greater than the depth of penetration, its behavior at high frequencies becomes a surface phenomenon.

Maxwell discovered that the voltage required to force a varying current through a wire increases more than could be explained by inductive reactance. The phenomenon is called "skin effect". The current is concentrated in the outer surface of the conductor, it is crowded to the outer edge of the conductor.

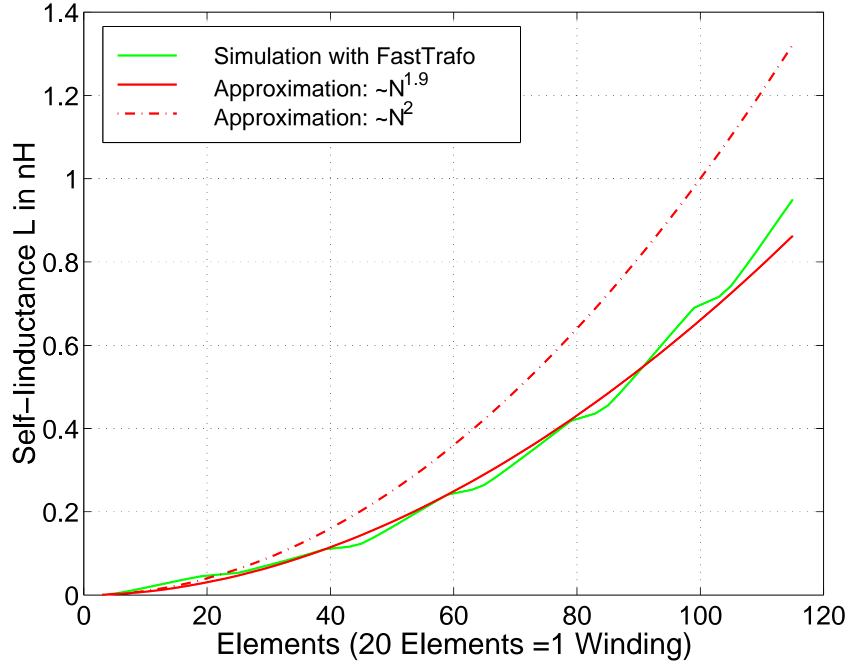

Figure 3.5: Primary self inductance of the transformer *BL62S005* with 6 turns on the primary side.

The depth of current penetration in a conductor depends on the frequency and also on the properties of the conductive material, its conductivity σ or resistivity ρ and its permeability μ.

The depth of penetration is defined as the depth at which the current density (or magnetic flux) is attenuated by $1/e$ (-8.7dB). The depth of penetration δ, by this definition, is

$$\delta = \sqrt{\frac{2\rho}{\mu\omega}} \tag{3.16}$$

δ is always greater than 0.9μm at frequencies smaller than 10 GHz in aluminum as conductor material.

3.2.1 Equivalent Series Resistance

The conductor-height T of monolithic transformers depends on the semiconductor process and is in a typical range of $0.5\mu m \ll T \ll 2\mu m$. So in most cases the skin-effect in vertical direction is negligible. The horizontal conductor dimensions (conductor-width W) can be greater and the resistance can rise significantly at frequencies smaller than 10 GHz.

The series resistance of the conductors at near direct current frequencies can be written as

$$R_{AC} = R_{DC} = \rho \frac{l}{WT} \tag{3.17}$$

Equation (3.17) is valid when the conductor dimensions W and T are smaller than the penetration depth δ. If this assumption is not fulfilled the series resistance rises at higher frequencies. The series resistance is proportional to $\sqrt{f}$ for high frequencies.

$$R_{AC} \sim \sqrt{f}, \qquad f \to \infty \tag{3.18}$$

At low frequencies the resistance is proportional to

$$R_{DC} \sim 1 + f^2, \qquad f \to 0 \tag{3.19}$$

With (3.18) and (3.19) a equation for the resistance R_{AC} as a function of frequency can be found. An accurate formula for the series resistance was given by [Lofti 95].

$$R_{AC} = R_{DC} \left[1 + \left(\frac{f}{f_l} \right)^2 + \left(\frac{f}{f_u} \right)^5 \right]^{\frac{1}{10}} \tag{3.20}$$

$$f_l = \frac{\pi \rho}{2\mu WT}, \quad f_u = \frac{\pi^2 \rho}{\mu T^2} \left[\mathrm{K} \left(\sqrt{1 - \frac{T^2}{W^2}} \right) \right]^{-2} \tag{3.21}$$

The frequencies f_l and f_u are the cutting frequencies of the low frequency case and of the high frequency case. K is the elliptic integral first order and is available in tables or i.e in the software *Matlab*^{TM}.

$$\mathrm{K}(x) = \int_0^{\frac{\pi}{2}} \frac{1}{\sqrt{1 - x^2 \sin^2(\phi)}} \, d\phi \tag{3.22}$$

The error of equation (3.20) within the assumption that $0.3 < T/\delta < 2$ is smaller than 1%.

Fig. 3.6 shows the primary and secondary series resistance of the example transformer presented in Sect. 2.2.2 (Fig. 2.5(b)) with different track width W. The conductor material is aluminum and has a conductivity of $\sigma = 33S/\mu m$ and a thickness of $T = 1.4\mu m$. The simulation with the lower track width W shows the higher DC-resistance but the skin-effect starts at higher frequencies compared to the simulations with higher track width. The simulation was done with the transformer CAD-tool *FastTrafo*.

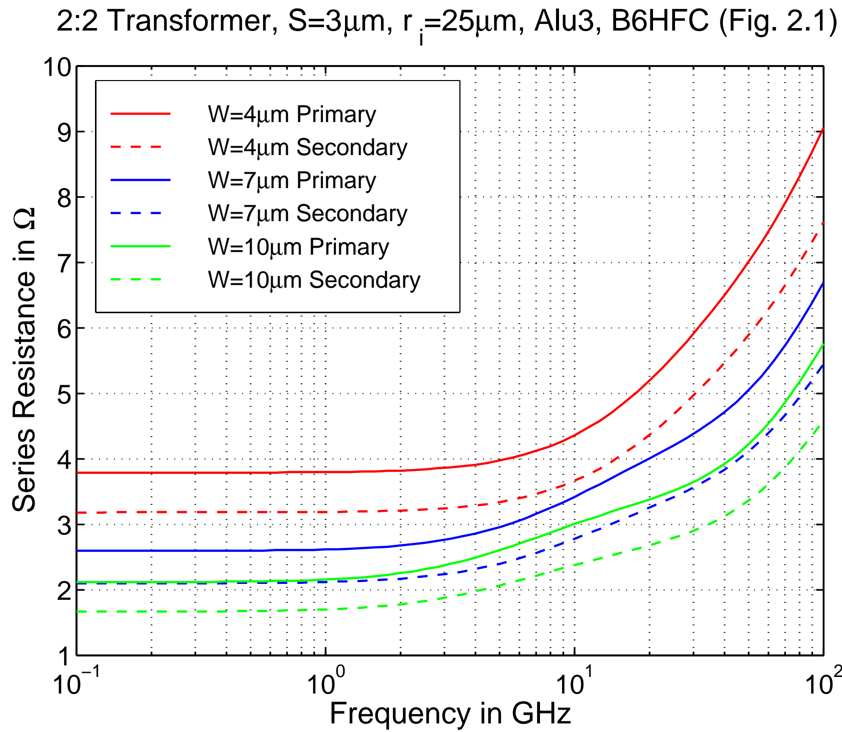

Figure 3.6: Series resistance of a 2:2 Transformer (Fig. 2.5(b)) as a function of frequency.

3.3 Substrate Loss

The substrate-material of silicon based technologies is p$^-$-doted silicon. It is a mixture of conductor and dielectric, which means that the substrate of each technology has a finite conductivity σ and relative permittivity $\varepsilon_r \geq 1$. In recent semiconductor processes the conductivity can reach values from a few Siemens per Meter up to 200 S/m .

Capacitive coupling from the conductor to substrate and finite conductivity of the substrate causes a current flow from the conductor through the substrate down to the ground plane. This current flow represents additional losses which are modeled by substrate resistances R_{Sub} in the equivalent circuit of Sect. 2.3. Now a new expression for the substrate resistance is derived. The formula is based on impedance expressions in [Hilberg 81] and simulations with the 2-D FEM field simulator *Maxwell field* [Ansoft 93].

3.3.1 Conductor on Substrat

Monolithic integrated transformers are complex 3-D geometries. Step by step we want to develop an accurate approximation for the substrate resistance.

First we simplify the situation to a 2-D-problem. Figure 3.7 shows a single conductor placed directly on the substrate. On the upper side the conductor is surrounded by a dielectric. On the bottom side the substrate with a finite conductivity σ is situated. The ground plane is at the bottom of the substrate. The area upside the conductor is not of interest for resistance calculation.

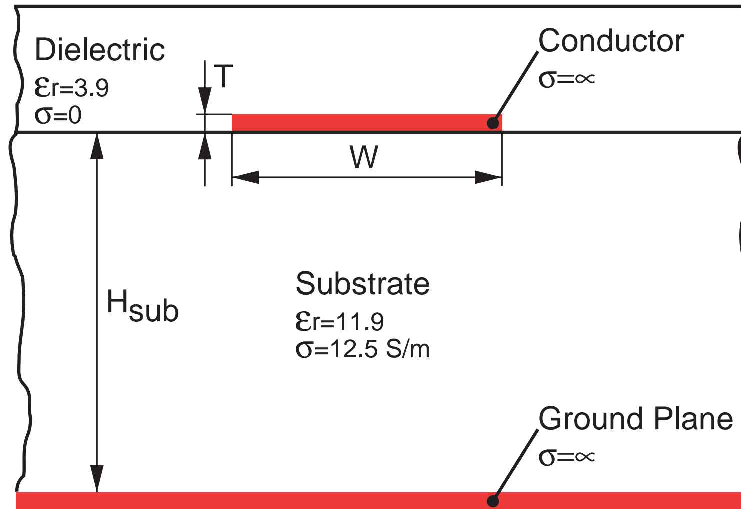

Figure 3.7: Conductor placed directly on the substrate.

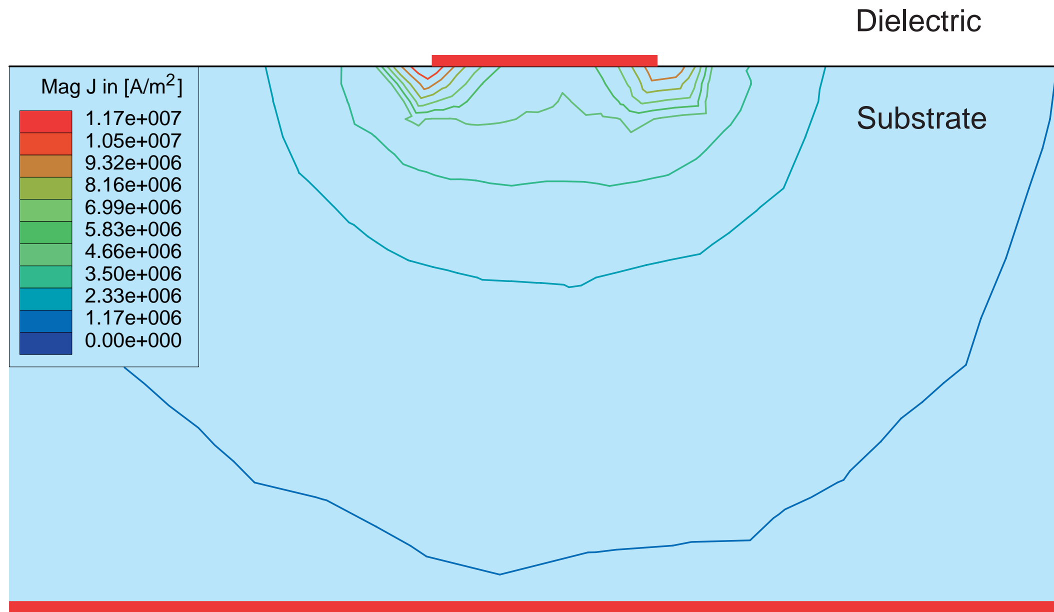

Figure 3.8: Lines of constant current density around a conductor placed on the substrate.

Fig. 3.8 shows lines of constant current density representing the current-flow from

the conductor to the ground plane. The voltage amplitude is 1V. The substrate material has a thickness of $H_{Sub} = 200\mu m$ and a conductivity of $\sigma = 12.5$S/m. The current density has a maximum at the edges of the conductor. At some distance to the conductor the lines of constant current density get an elliptic shape. The simulation was done with the 2-D FEM simulator *Maxwell field* by [Ansoft 93].

Now we want to calculate the resistance from the conductor to the ground plane. To solve this task it makes sense to reduce the problem to a known physical layout. The "mirror method" is a perfect tool to convert the situation to a known problem and also to go back to original physical layout.

If we mirror horizontally at the line of the conductor we get the situation shown in Fig. 3.9. There is exact correspondence between the parts on either side of the central line.

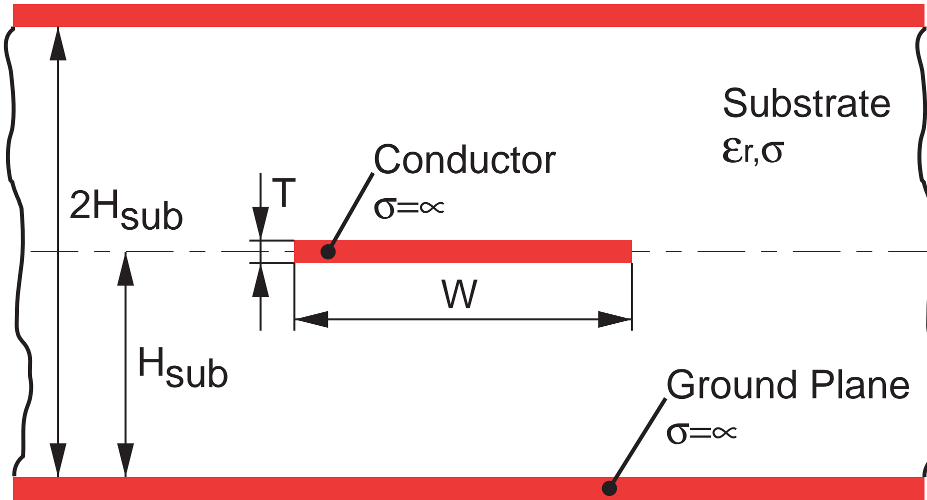

Figure 3.9: Mirror method: The situation in Fig. 3.7 is mirrored horizontally.

Under the condition that the conductivity of the substrate $\sigma_{Sub} = 0$ we can handle the geometry in Fig. 3.9 as a transmission line. The characteristic impedance of a lossless transmission line can be written as

$$Z = \sqrt{\frac{L'}{C'}}, \quad \sigma_{Sub} = 0, \ \sigma_{COND} = \infty \tag{3.23}$$

where L' is the inductance and C' the capacity per length unit of the transmission line.

It exists an impedance-formula for the physical layout shown in Fig. 3.9. In the case of a perfect insulator ($\sigma = 0$) instead the substrate the formula for the characteristic impedance was noted by [Hilberg 81].

$$Z = \frac{\eta}{2\pi} \ln\left[2\coth\left(\frac{\pi}{8}\frac{W}{H_{Sub}}\right)\right], \quad \text{for } Z > \eta/4 \tag{3.24}$$

$$Z = \frac{\pi\eta}{8} / \ln\left[2\, e^{\frac{\pi}{4}\frac{W}{H_{Sub}}}\right], \quad \text{for } Z < \eta/4 \tag{3.25}$$

where η is a constant depending on the material. In the case of the transmission line η is the phase velocity in the dielectric.

$$\eta = \sqrt{\frac{\mu}{\epsilon}} \tag{3.26}$$

The current field lines in Fig. 3.8 are similar to the electric field lines of the equivalent transmission line. Because of this fact we want to suppose that the specific resistance R_{Sub} is proportional to the impedance Z of the transmission line.

$$R'_{Sub} \sim Z \tag{3.27}$$

Some simulations for the specific substrate resistance make clear that the constant η is the specific resistivity ρ of the substrate.

$$\eta = \rho \tag{3.28}$$

With (3.28) the formula for the specific substrate resistance of a single conductor placed on the substrate can be written as

$$R'_{Sub} = \frac{\rho}{\pi} \ln\left[2\coth\left(\frac{\pi}{8}\frac{W}{H_{Sub}}\right)\right], \quad \text{for } W/H_{Sub} < 1 \tag{3.29}$$

$$R'_{Sub} = \frac{\rho\pi}{4} / \ln\left[2\, e^{\frac{\pi}{4}\frac{W}{H_{Sub}}}\right], \quad \text{for } W/H_{Sub} > 1 \tag{3.30}$$

The approximation and simulation of the substrate resistance is illustrated in Fig. 3.10. Note the two valid ranges for the approximations. In practice W/H_{Sub} is always smaller than 1 and therefore (3.29) is relevant. The error of the approximations in the valid range compared to the simulation is always smaller than 3%. The simulations was done with *FastHenry* and *Maxwell Field Simulator*.

3.3.2 Conductor Suspended in Dielectric

A conductor placed directly on the substrate as considered in Sect. 3.3.1 is not the case at monolithic integrated transformers. Mostly, semiconductor processes allow only conductor suspended in a dielectric above the substrate. We have to

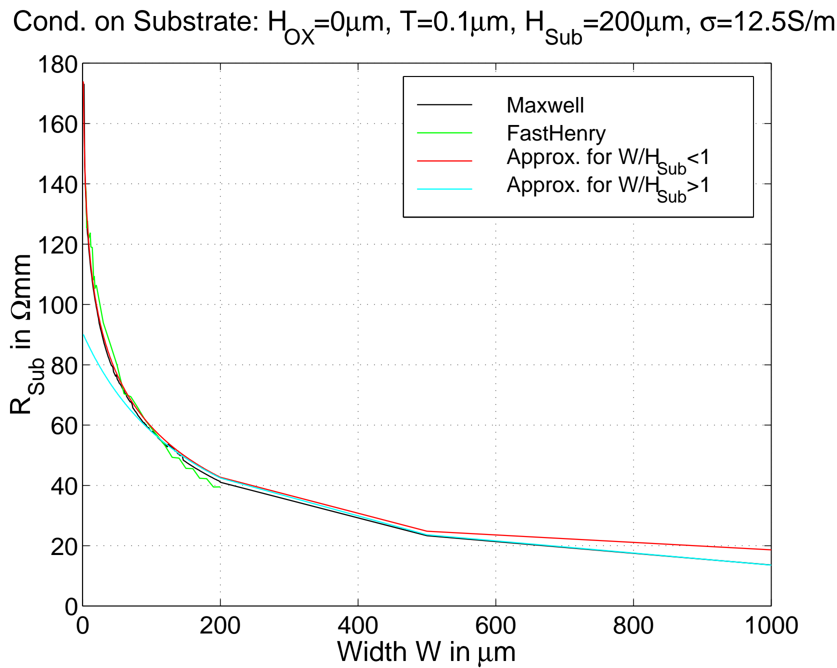

Figure 3.10: Specific resistance from a single trace placed on the substrate to the ground plane.

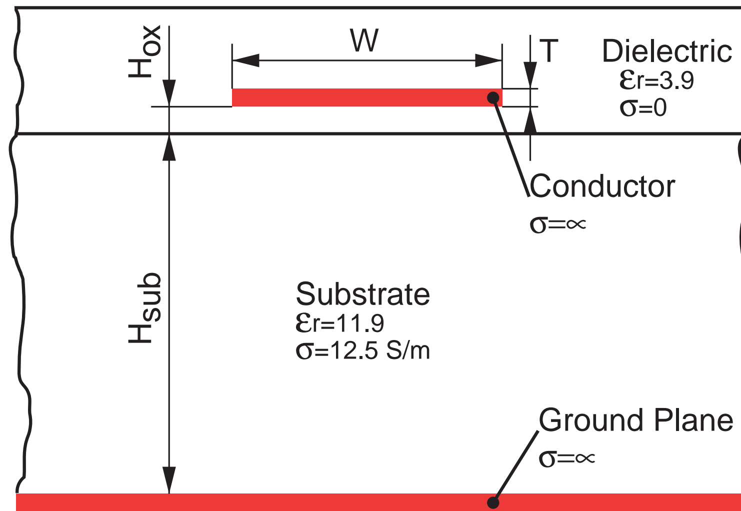

Figure 3.11: Conductor suspended in a dielectric above the substrate.

work out a formula based on (3.29) and (3.30) to calculate the resistance from the conductor through the substrate to the ground plane.

Fig. 3.11 shows a conductor (i.e a turn of a transformer) suspended in an ideal

dielectric ($\sigma = 0$). The conductor has a width of W and a distance to the substrate of H_{OX}. The conductive substrate has a height of H_{Sub}. A ground plane is placed at the bottom.

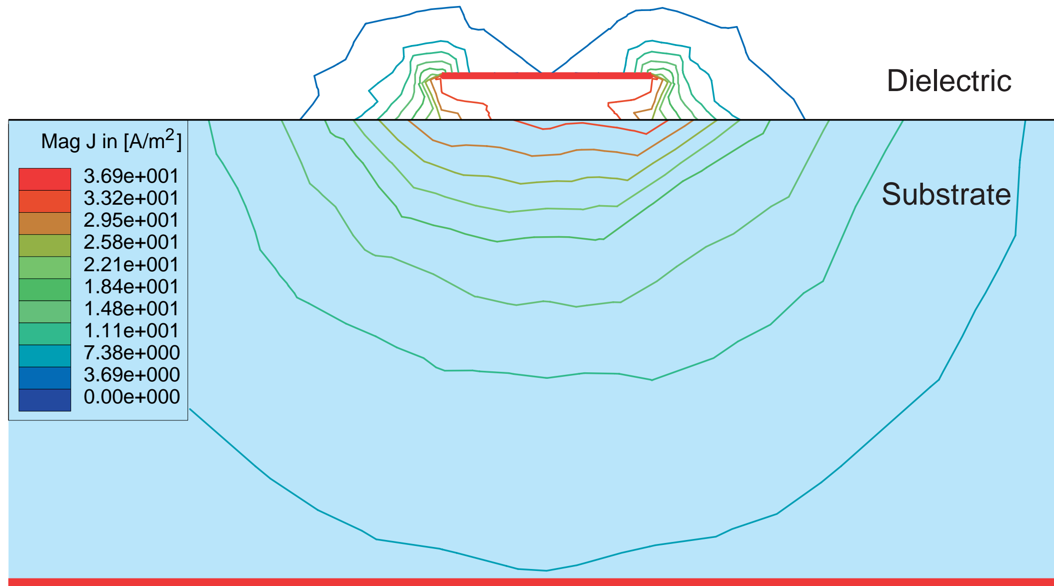

Figure 3.12: Lines of constant current density around a conductor suspended in a dielectric.

Fig. 3.12 shows the simulation done with the *Maxwell Field Simulator*. The voltage amplitude is 1V. The substrate material has a thickness of $H_{Sub} = 200\mu m$ and a conductivity of $\sigma = 12.5$S/m. Capacitive coupling causes a displacement current to the substrate. Fig. 3.12 shows lines of constant current density which have again an elliptic shape at some distance to the conductor.

From Fig. 3.12 is clear that the current-feed-in area at the substrate edge has a greater width than the physical width W caused by capacitive coupling. We define an effective feed-in width W_{eff} depending on the distance H_{OX} and the conductor height T.

$$W_{eff} = W + 6\,H_{OX} + T \tag{3.31}$$

The physical width W is replaced in (3.29) and (3.30) by the effective width W_{eff} and the specific substrate resistance of a single conductor suspended in a dielectric above the substrate can be written as

$$R'_{Sub} = \frac{\rho}{\pi} \ln\left[2 \coth\left(\frac{\pi}{8}\frac{W + 6\,H_{OX} + T}{H_{Sub}}\right)\right], \quad \text{for } \frac{W_{eff}}{H_{Sub}} < 1 \tag{3.32}$$

$$R'_{Sub} = \frac{\rho\pi}{4} / \ln\left[2\; e^{\frac{\pi}{4}\frac{W+6\,H_{OX}+T}{H_{Sub}}}\right], \quad \text{for } \frac{W_{eff}}{H_{Sub}} > 1 \tag{3.33}$$

The equations are valid within the range whereby in practice (3.32) is relevant.

The approximation and simulation of the substrate resistance is illustrated in Fig. 3.13. For distances $H_{OX} > 0$ the substrate tends to a limited value if W is near zero ($W \to 0$). The error of the approximations in the valid range compared to the simulation is always smaller than 3%. The simulation data in Fig. 3.13 was produced with *Maxwell Field Simulator*.

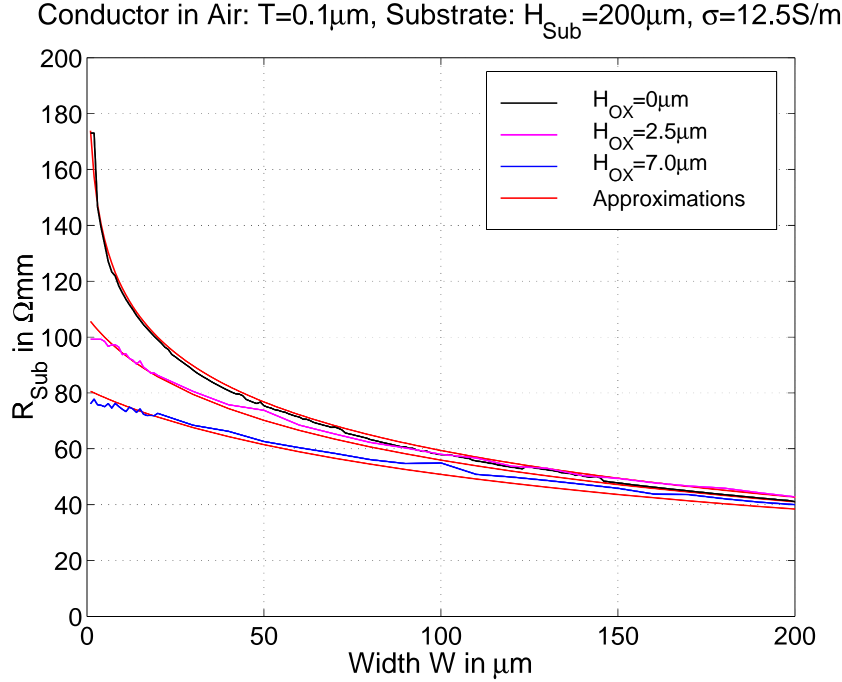

Figure 3.13: Specific resistance from a single conductor to ground plane.

R_{Sub} of a complete transformer winding is based on (3.33) and (3.32) where W is replaced by the width of the primary winding $W_P = r_{OP} - r_{IP}$ or secondary winding $W_S = r_{OS} - r_{IS}$ as shown in Fig. 2.5. R_{SubP} for the primary winding can be written as

$$\begin{aligned} R_{SubP} &= \frac{\rho}{\pi\, l_{MP}} \ln\left[2 \coth\left(\frac{\pi}{8}\frac{W_P + 6\, H_{OX} + T}{H_{Sub}}\right)\right] \\ R_{SubS} &= \frac{\rho}{\pi\, l_{MS}} \ln\left[2 \coth\left(\frac{\pi}{8}\frac{W_S + 6\, H_{OX} + T}{H_{Sub}}\right)\right] \end{aligned} \quad (3.34)$$

within the range $W_{eff}/H_{Sub} < 1$ and

$$\begin{aligned} R_{SubP} &= \frac{\rho\pi}{4\, l_{MP}} / \ln\left[2\ e^{\frac{\pi}{4}\frac{W_P+6\,H_{OX}+T}{H_{Sub}}}\right] \\ R_{SubS} &= \frac{\rho\pi}{4\, l_{MS}} / \ln\left[2\ e^{\frac{\pi}{4}\frac{W_S+6\,H_{OX}+T}{H_{Sub}}}\right] \end{aligned} \quad (3.35)$$

within the range $W_{eff}/H_{Sub} < 1$, where l_{MP} and l_{MS} are the mean perimeters of the transformer windings. In the case of a circular transformer as shown in Fig. 2.5 l_{MP} and l_{MS} are calculated as

$$l_{MP} = \pi(r_{OP} + r_{OP}),\ l_{MS} = \pi(r_{OS} + r_{IS}) \tag{3.36}$$

In the case of a square shaped transformer as shown in Fig. 2.4 l_{MP} and l_{MS} are calculated as

$$l_{MP} = 4\,(a_{OP} + a_{OP}),\ l_{MS} = 4\,(a_{OS} + a_{IS}) \tag{3.37}$$

The resistances R_{Sub1} to R_{Sub6} of the model shown in Fig. 2.16 can be determined as

$$\begin{aligned} R_{Sub1} = R_{Sub3} = 4R_{SubP},\ R_{Sub2} = 2R_{SubP} \\ R_{Sub4} = R_{Sub6} = 4R_{SubS},\ R_{Sub5} = 2R_{SubS} \end{aligned} \tag{3.38}$$

3.4 Capacity Extraction

Parasitic capacities are difficult to determine accurately. The conductors of monolithic integrated transformers represent closely coupled lines. Because of the dominance of the edge singularity and coupled conductor construction, capacitive effects are best investigated in mesh point analysis and simulations. However, some basics about capacity calculation are presented in this section.

The parameters needed to characterize the capacity of coupled structures are the even- and odd-mode capacitances of parallel coupled conductors.

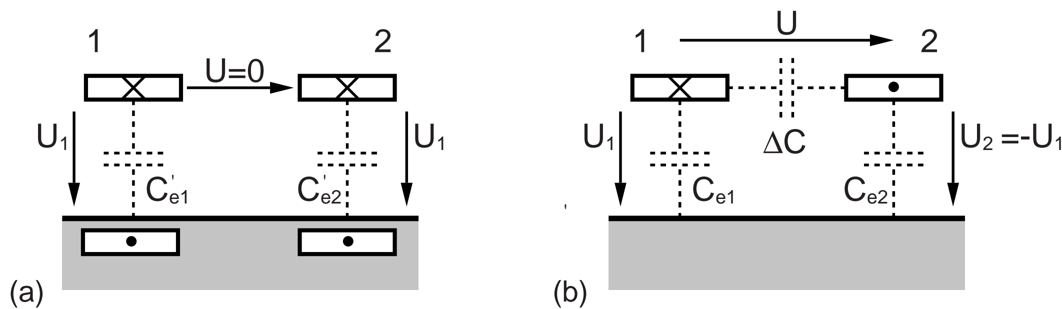

Figure 3.14: (a)Even- and (b)odd-mode capacities of two conductors.

Fig. 3.14 shows the two possible cases for two coupled conductors embedded in a uniform homogeneous dielectric of permittivity ϵ and permeability μ_0. The even-mode happens if in both conductors the voltage have the same amplitude and phase. If the voltages are not in phase a gap capacity ΔC represents the odd-mode. The operation mode of a monolithic transformer is a mixture of both modes.

Fringing Capacities

The capacity calculation can be splitted into several parts of capacities. Fig. 3.15 shows all considered capacities for the calculation of the total odd-mode and even-mode capacity.

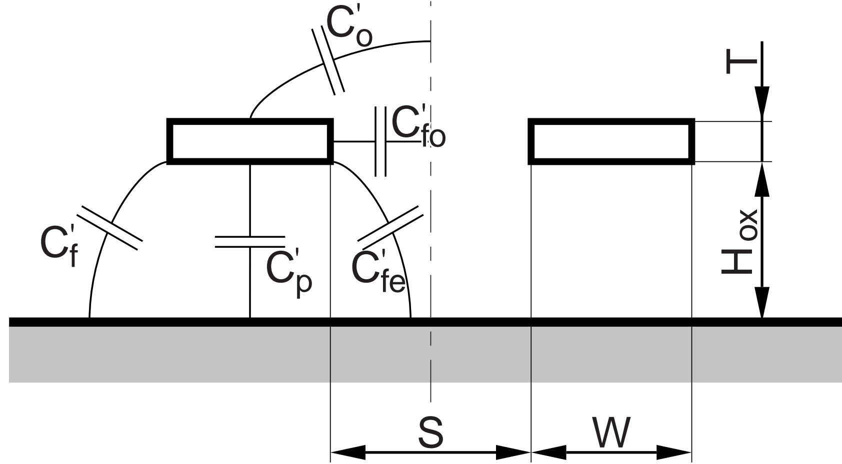

Figure 3.15: Capacitive coupled rectangular conductors suspended in a dielectric.

To find total even-mode capacitance C'_e to ground (Fig. 3.14) the appropriate components of fringing capacitance are added to the parallel-plate component C'_p. For a line of more than two conductors the total even-mode capacitance can be written as

$$C'_e = C'_p + 2C'_{fe} \tag{3.39}$$

In calculating total capacitance for the end lines in Fig. 3.4, care must be taken to add to the parallel-plate component the appropriate fringing capacitance at each edge of the conductor. The even-mode capacitance for the end conductor is

$$C'_e = C'_p + C'_{fe} + C'_f \tag{3.40}$$

The difference between odd- and even-mode fringing capacitance is denoted by the gap capacitance $\Delta C'$.

$$\Delta C' = C'_o + C'_{fo} - C'_{fe} \tag{3.41}$$

The parallel-plate capacitance between a conductor and the ground plane mentioned in the equations before using the notation of Fig. 3.15 is

$$C'_p = \epsilon \frac{W}{H_{OX}} \tag{3.42}$$

The calculation of the other fringing capacities in Fig. 3.15 can be found in [Gupta 69] and [Smith 71]. The even- and odd-mode capacities are considered by the capacities C_{K1} to C_{K4} and C_{OX1} to C_{OX6} in the transformer model shown in Fig. 2.16.

As mentioned before the best way to extract the capacity of complex geometries is a simulation based on mesh analysis. The capacity-calculation of a complete integrated monolithic transformer in the tool *FastTrafo* is based on *FastCap* [MIT 92]. The exact modeling of the layer construction is important to get accurate results. In order to reach short processing times only a small part of the transformer's cross section is the input to the FEM-core *FastCap*. The static specific capacities from primary to secondary C'_{PS}, primary C'_{OXP} to substrate and secondary C'_{OXS} to substrate are extracted.

The static capacities of the whole transformer are

$$C_{OXP} = l_{MP}\, C'_{OXP},\;\; C_{OXS} = l_{MS}\, C'_{OXS},\;\; C_{PS} = l_M\, C'_{PS} \tag{3.43}$$

where l_{MP} and l_{MS} is calculated in (3.36) and (3.37). l_M is the mean perimeters of the transformer. In the case of a circular transformer as shown in Fig. 2.5 l_M is calculated as

$$l_M = \pi\,[\max(r_{OP}, r_{OS}) + \min(r_{IP}, r_{IS})] \tag{3.44}$$

In the case of a square shaped transformer as shown in Fig. 2.4 l_M is calculated as

$$l_M = 4\,[\max(r_{OP}, r_{OS}) + \min(r_{IP}, r_{IS})] \tag{3.45}$$

C_{OX1} to C_{OX6} in the equivalent model shown in Fig. 2.16 are determined as

$$\begin{aligned} C_{OX1} = C_{OX3} = C_{OXP}/4,\;\; C_{OX2} = C_{OXP}/2 \\ C_{OX4} = C_{OX6} = C_{OXS}/4,\;\; C_{OX5} = C_{OXS}/2 \end{aligned} \tag{3.46}$$

The sum of the capacities C_{OX} for each winding is the static capacity C_P and C_S to the substrate.

The parasitic capacitive coupling between primary and secondary winding in the equivalent model are determined as

$$C_{K1} = C_{K2} = C_{K3} = C_{K4} = C_{PS}/4 \tag{3.47}$$

3.5 Test-Structures for Measurement and Characterization

Scattering parameters (S-parameters) characterize the electrical behavior of a monolithic transformer completely. To compare the measurement with the model we need to measure the S-parameters of the transformer. Therfore, transformers are placed as a test-structure on silicon.

Fig. 3.16 shows the test-structure of the example transformer *BL62S005* considered in Sect. 4.1. The connection between measurement equipment and device under test (DUT) is performed by tiny needles. To put the needles on the DUT, pads are needed which have big dimensions related to the transformer geometry. The pads represent a parallel plate capacitor and falsify the measurement of the transformer. So additional test structures are necessary to get the S-parameters of the DUT.

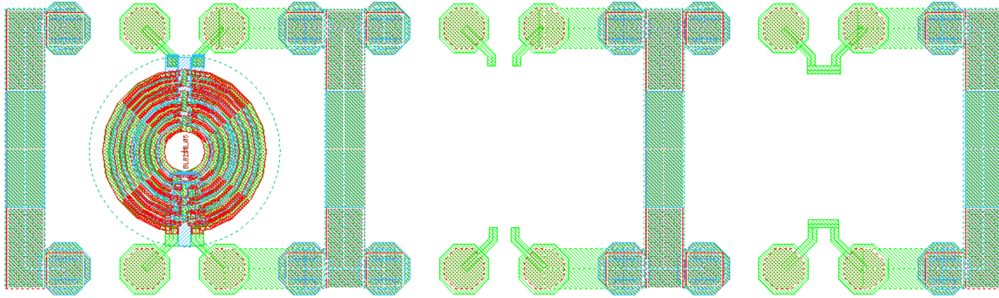

Figure 3.16: Test-structures for measurement of transformer *BL62S005* with transformer-, open- and short-structure.

As known from network-analyzers we can calibrate with open- and short-test-structures. Fig. 3.16 shows additional test-structures for open and short. After measured S-parameters of open and short we can analyze the data. De-embedding is the key for this task. The following steps show how to get the corrected S-parameters of the DUT. The S-parameters are converted to Y-parameters standardized to $Z_0 = 50\,\Omega$. The conversion in both directions is defined as

$$\mathbf{Y} = \frac{1}{Z_0}\left[(\mathbf{E}-\mathbf{S})(\mathbf{E}+\mathbf{S})^{-1}\right] \tag{3.48}$$

$$\mathbf{S} = \left[(\mathbf{E}-Z_0\mathbf{Y})(\mathbf{E}+Z_0\mathbf{Y})^{-1}\right] \tag{3.49}$$

where $\mathbf{E}$ is the identity matrix with ones on the diagonal and zeros elsewhere.

$$\mathbf{E} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$$

The conversion from S-parameter to Z-parameter and back is defined as

$$\mathbf{Z} = Z_0\left[(\mathbf{E}+\mathbf{S})(\mathbf{E}-\mathbf{S})^{-1}\right] \tag{3.50}$$

$$\mathbf{S} = \left[(\mathbf{Z}/Z_0-\mathbf{E})(\mathbf{Z}/Z_0+\mathbf{E})^{-1}\right] \tag{3.51}$$

The measured S-parameters of the transformer-structure $\mathbf{S}$ corrected with the measured S-parameters of the open structure $\mathbf{S}_{OP}$ can be calculated as

$$\mathbf{S}_{Tr-Op} \leftrightarrow \mathbf{Y}_{Tr-Op} = \mathbf{Y} - \mathbf{Y}_{Op} \tag{3.52}$$

The next step is to correct with the measured S-parameters of the short structure $\mathbf{S}_{Sh}$.

$$\mathbf{S}_{Tr} \;\leftrightarrow\; \mathbf{Z}_{Tr} = \mathbf{Z}_{Tr-Op} - \mathbf{Z}_{Sh} \tag{3.53}$$

$\mathbf{S}_{Tr}$ describes the electrical characteristic of the transformer and can be compared to the model. The data of the transformer-structure $\mathbf{S}$ in addition to test-structures $\mathbf{S}_{Sh}$, $\mathbf{S}_{Op}$ applies after de-embedding the real scattering parameters $\mathbf{S}_{Tr}$ of the transformer.

Fig. 3.17 shows the test structures of the example transformer *N3M2* considered in Sect. 4.2. Only a open structure is available which results in a bad de-embedding.

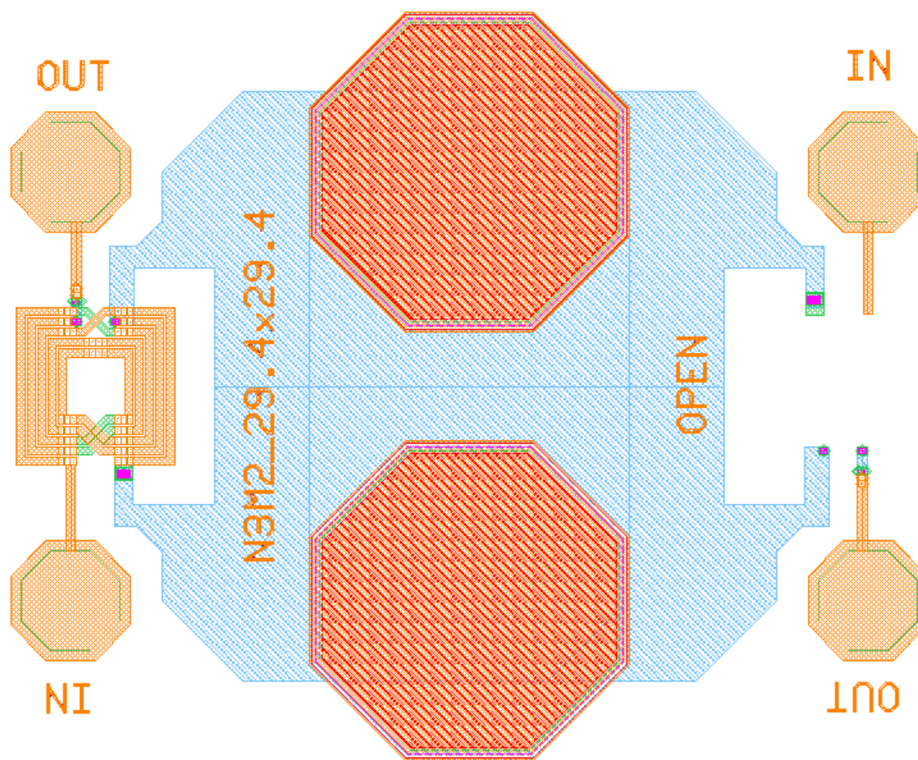

Figure 3.17: Test-structures for measurement of transformer *N3M2* with transformer- and open-structure.

Chapter 4

Design Examples

A method for characterization of monolithic lumped planar transformers has been proposed. The modeling and parameter extraction of such transformers has been verified by multiple transformers. In this work the measurement of two types of transformers is presented as example. The first type offers a high coupling performance up to 4 GHz. The second type of transformer offers a high self resonance frequency of 20 GHz.

4.1 Monolithic Transformer *BL62S005*

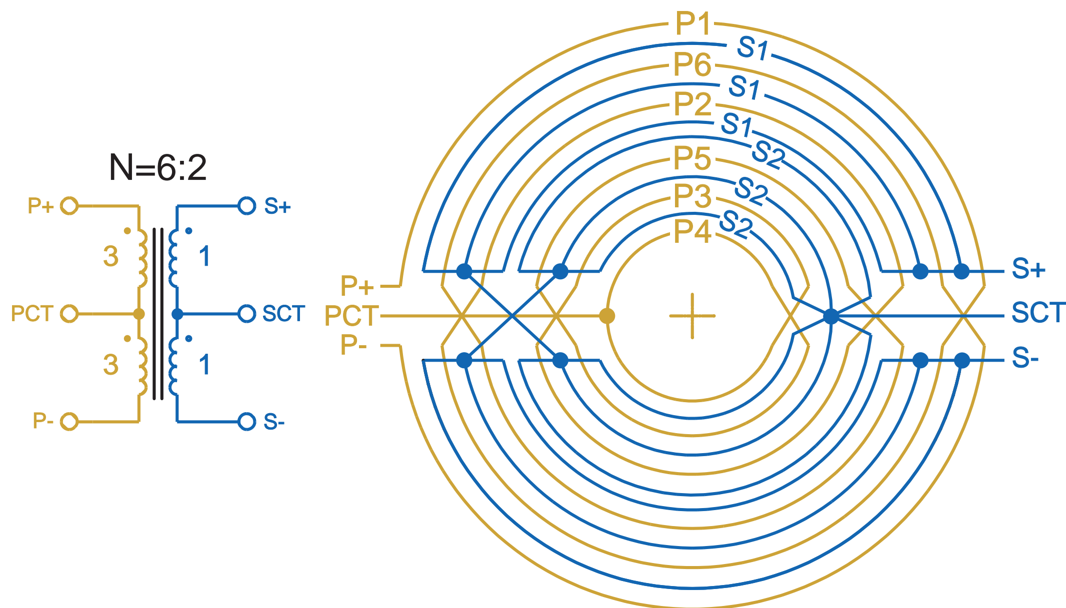

Figure 4.1: Transformer *BL62S005*: (a) Winding scheme (b) Schematic symbol [Simbürger 00].

The monolithic integrated transformer *BL62S005* was designed for the use as input-balun and interstage matching network in power amplifiers [Simbürger 00].

Fig. 4.1 shows the schematic symbol and the planar winding scheme of the transformer. The transformer offers a high coupling performance due tue an interlaced winding scheme. The six primary turns P1-P6 are connected in series. On the secondary side the three outer and the three inner turns are connected in parallel to form two groups S1 and S2. The groups are connected in series. With six primary turns and two secondary turns a turn ratio of $n = 6 : 2$ is achieved. Centertaps for balanced applications on the primary side PCT and on the secondary side SCT are available.

Fig. 4.2 shows a three-dimensional topview of the transformer. The primary ports, P+, PCT and P-, are located on the left side. The secondary ports, S+, SCT and S-, are located on the right side. The transformer design is completely symmetric about a line. The outer diameter is $2r_O = 205\,\mu$m and the inner diameter is $2r_I = 50\,\mu$m. The lateral spacing between the turns is about $1.5\,\mu$m and has different values for each metal layer. The conductor width on the primary side is about $W = 4\,\mu$m and different for each winding. The conductor width on the secondary side about $W = 3\,\mu$m and also different for each winding.

The operation frequency of 1.9 GHz is in the range of mobile communications. The same design was used in a power amplifier at 900 MHz [Heinz 00]. To get an operation frequency at 900 MHz the whole transformer was scaled by a factor 2 from $205\,\mu$m to $410\,\mu$m outer diameter.

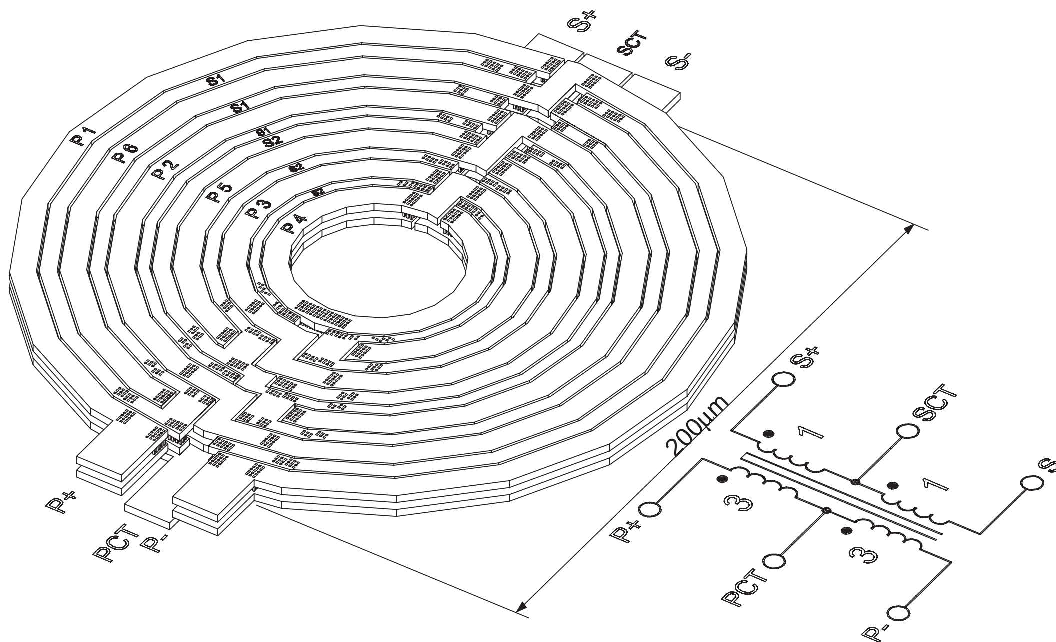

Figure 4.2: 3-D-view of the example transformer *BL62S005* [Simbürger 00].

A three dimensional cross section of the transformer *BL62S005* is shown in Fig. 2.11. The primary winding consists of metal 3 and metal 2 connected in parallel and is separated to the substrate by H_{OX}=3.1 μm. The secondary winding consists of metal 1-3 connected in parallel to decrease the ohmic loss. The distance to the substrate is H_{OX}=1.6 μm resulting in a higher capacitive coupling into the substrate compared to the primary winding.

4.1.1 Measurement and Simulation Results up to 5GHZ

The equivalent circuit of the high coupling performance transformer *BL62S005* is shown in Fig. 4.3. All parameter values are extracted by simulation with *Fast-Trafo*.

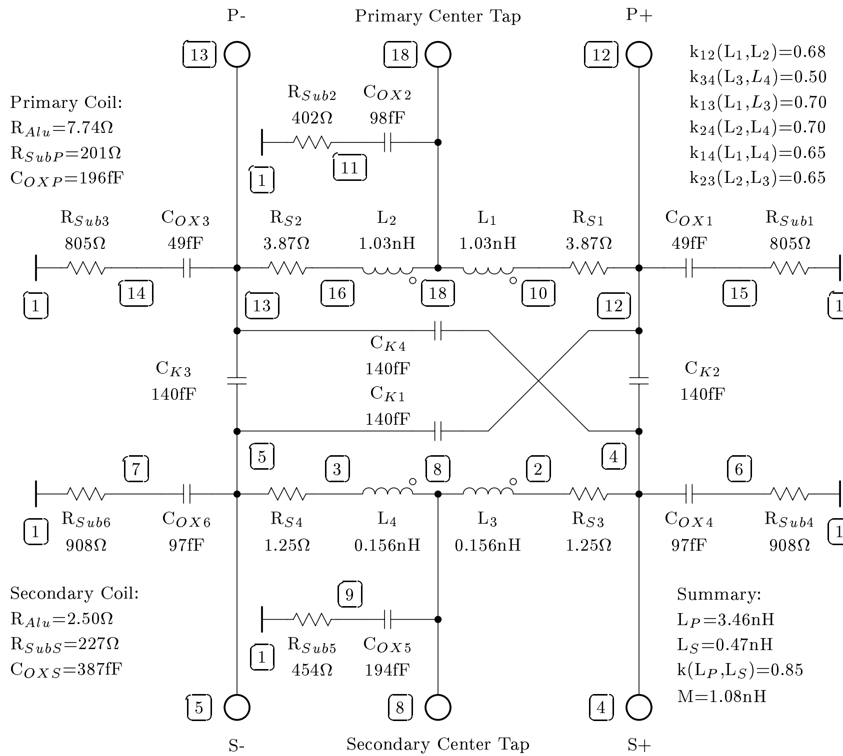

Figure 4.3: Equivalent circuit of the transformer *BL62S005*.

The values of the primary and secondary self inductance are

$$L_P = L_1 + L_2 + 2\,k_{12}\,\sqrt{L_1\,L_2} = 3.46\,\mathrm{nH}$$
$$L_S = L_3 + L_4 + 2\,k_{34}\,\sqrt{L_3\,L_4} = 0.47\,\mathrm{nH}$$

The strength of magnetic coupling between primary and secondary side denoted by the k-factor is

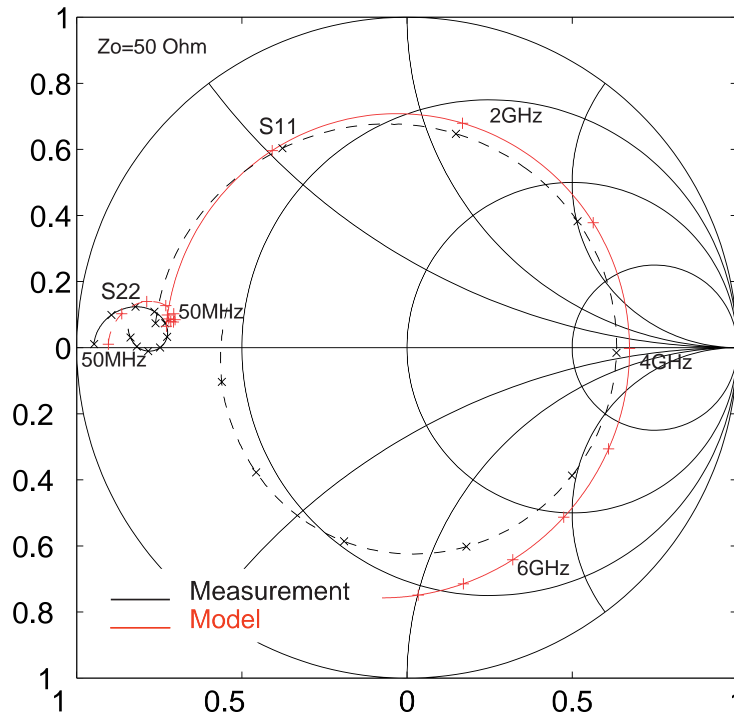

Figure 4.4: Scattering parameters S11 and S22 of the transformer *BL62S005*.

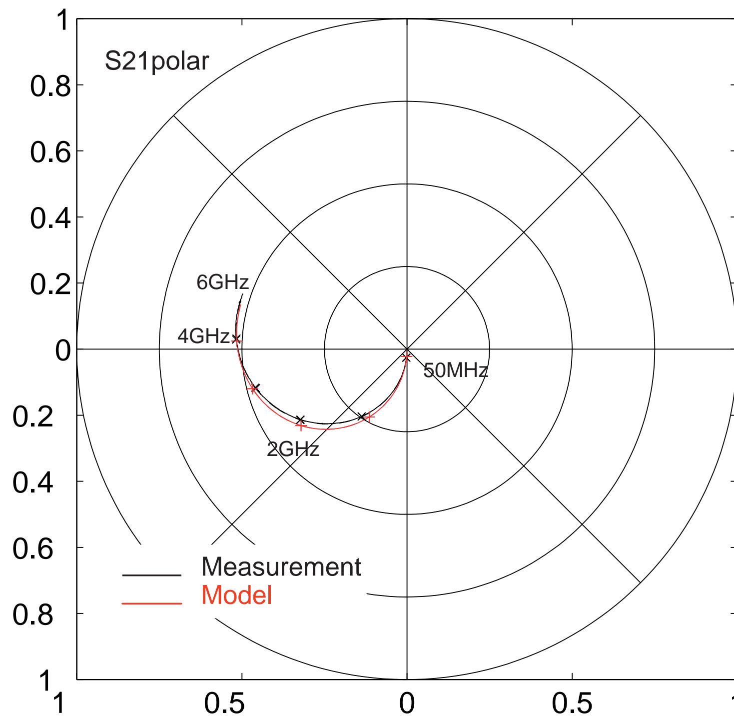

Figure 4.5: Transmission S21 in polar-diagram of the transformer *BL62S005*.

$$k_{PS} = \frac{k_{13}\sqrt{L_1 L_3} + k_{14}\sqrt{L_1 L_4} + k_{23}\sqrt{L_2 L_3} + k_{24}\sqrt{L_2 L_4}}{\sqrt{L_P L_S}} = 0.85$$

The series resistance of the conductors on the primary side is $R_{Alu} = 7.74\,\Omega$ and on the secondary side $R_{Alu} = 2.50\,\Omega$. Tue due the greater distance to the substrate the parasitic capacity of the primary winding $C_{OXP} = 196\,\text{fF}$ is only the half capacity compared to the secondary winding ($C_{OXS} = 387\,\text{fF}$). The substrate resistances of both windings are in the same range of about $200\,\Omega$.

The transformer is placed as a test structure on silicon (Fig. 3.16) to measure the scattering parameters of the primary and secondary coil as well as of the primary-to-secondary transmission. The center taps are left open. De-embedding was done with open- and short-test-structures.

Fig. 4.4 shows the measured and simulated reflection S11 and S22 of the high coupling performance transformer *BL62S005*. The transformers S11 shows a nearly short circuit at low frequencies (50 MHz). The secondary winding is matched to a driver stage with a low input impedance. Therefore, S22 shows a very low impedance over the whole frequency range. Measurement and model shows excellent agreement up to 6 GHz.

Fig. 4.5 shows the real and imaginary part of S21. The insertion loss is about 9 dB at 1.9 GHz. The difference between simulation and model is negligible.

The S-parameter describes the electrical behavior of a monolithic transformer completely. But, not only the scattering parameters must be observed. Also the Z-parameters, Y-parameters, k-factor and Q-factor give a fundamental insight to the transformer's characteristic. This parameters can be derived directly from the S-parameters.

Especially Y_{11}^{-1}, which represents the input impedance of the secondary short-circuit transformer, becomes significant importance because of the low input impedance of the driver stage and output stage (Fig. 1.1(a)). Fig. 4.6 shows the real part of the measured and simulated Y_{11}^{-1} and Y_{22}^{-1}. Fig. 4.7 shows the imaginary part. The conversion from S-Parameter to Y-Parameter is done with (3.49) standardized to $Z_0 = 50\,\Omega$. Simulation and measurement agrees well up to 3 GHz.

Fig. 4.8 shows primary inductance L_p and secondary L_s as a function of frequency. The self inductances are analyzed using

$$L_P = L_1 + L_2 + 2\,k_{12}\sqrt{L_1 L_2} = \text{Im}\left(Z_{11}\right)/\omega \tag{4.1}$$

$$L_S = L_3 + L_4 + 2\,k_{34}\sqrt{L_3 L_4} = \text{Im}\left(Z_{22}\right)/\omega \tag{4.2}$$

Simulated and measured self resonance is at 4 GHz.

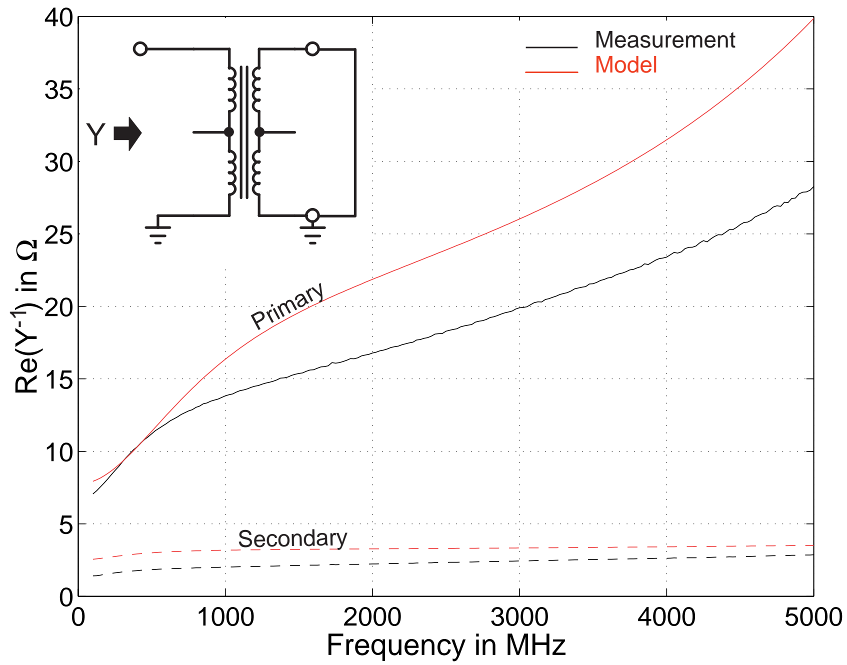

Figure 4.6: Real-part of input-impedance with secondary short-circuitt of the transformer *BL62S005*.

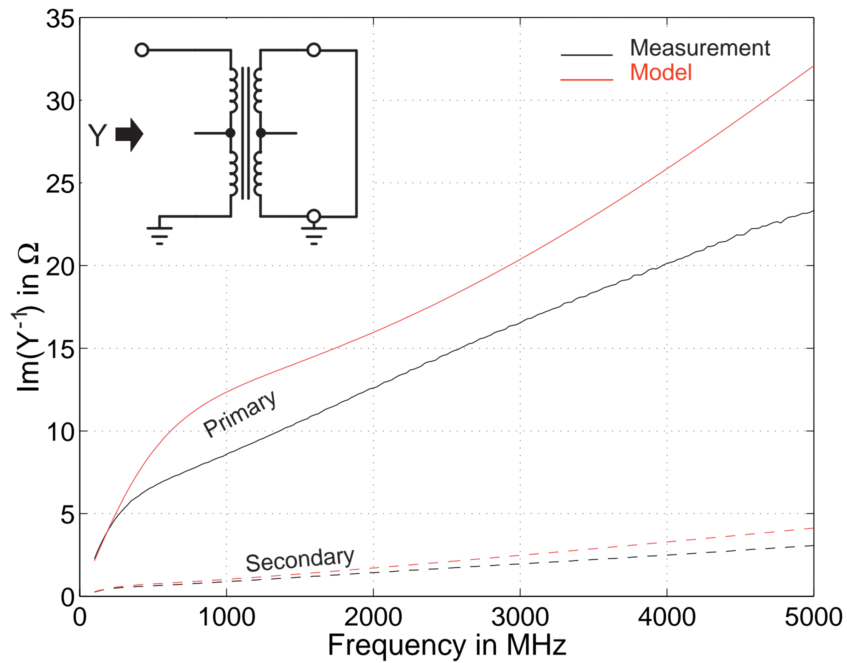

Figure 4.7: Imaginary-part of input-impedance with secondary short-circuit.

Analyzing the coupling coefficient as a function of frequency the relation

$$M = k_{13}\sqrt{L_1 L_3} + k_{14}\sqrt{L_1 L_4} + k_{23}\sqrt{L_2 L_3} + k_{24}\sqrt{L_2 L_4} = \sqrt{(Y_{11}^{-1} - Z_{11})\frac{Z_{22}}{\omega^2}} \quad (4.3)$$

is useful. Then the coupling coefficient can be written as

$$k(L_P, L_S) = \frac{M}{\sqrt{L_P L_S}} = \sqrt{\frac{(Y_{11}^{-1} - Z_{11})Z_{22}}{Im(Z_{11})Im(Z_{22})}} \quad (4.4)$$

Fig. 4.9 shows the coupling coefficient versus frequency. A k-factor of 0.9 at 1.9 GHz is a very high value for monolithic lumped planar transformers.

The quality factor is analyzed using the following expressions

$$Q = \mathrm{Im}\left(Z_{11}\right)/\mathrm{Re}\left(Z_{11}\right) \quad (4.5)$$

$$Q = \mathrm{Im}\left(Y_{11}^{-1}\right)/\mathrm{Re}\left(Y_{11}^{-1}\right) \quad (4.6)$$

Fig. 4.10 shows the characteristic Q-factor of the primary and secondary winding. Therefore, the output is left open. Typical Q-factor values of monolithic transformer windings are up to 8. Fig. 4.11 shows the quality factor of the transformer with shorted output. This is an important case because of the low input impedance of the output-driver stage.

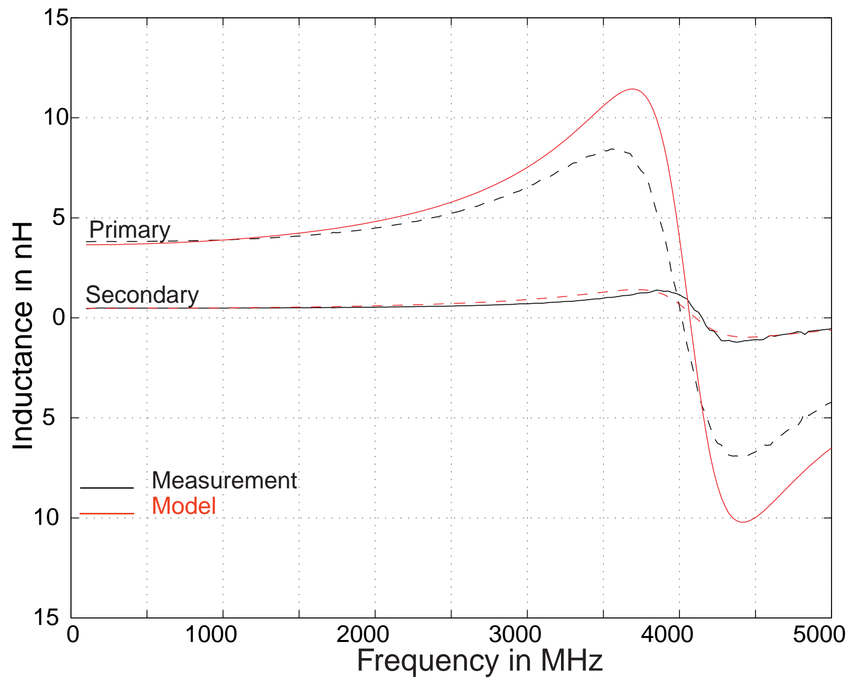

Figure 4.8: Self inductance of primary and secondary winding of the transformer *BL62S005*.

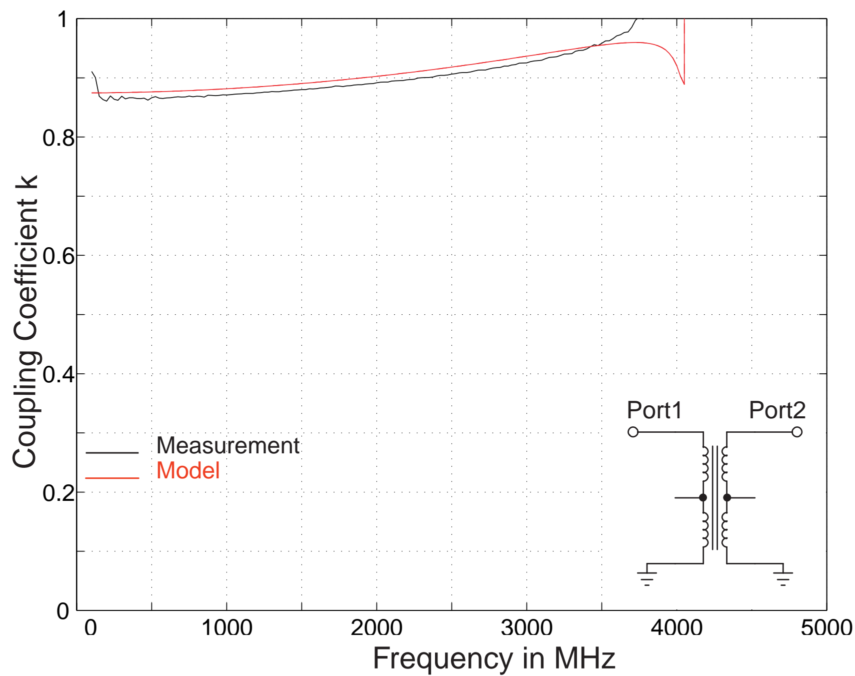

Figure 4.9: Coupling coefficient k versus frequency of the transformer *BL62S005*.

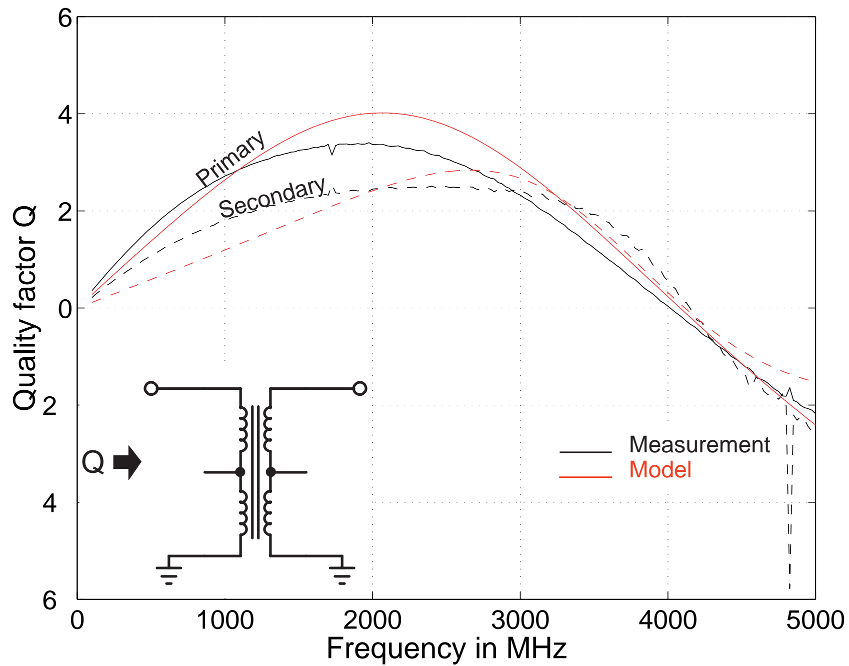

Figure 4.10: Quality factor with open at the secondary-side of the transformer *BL62S005*.

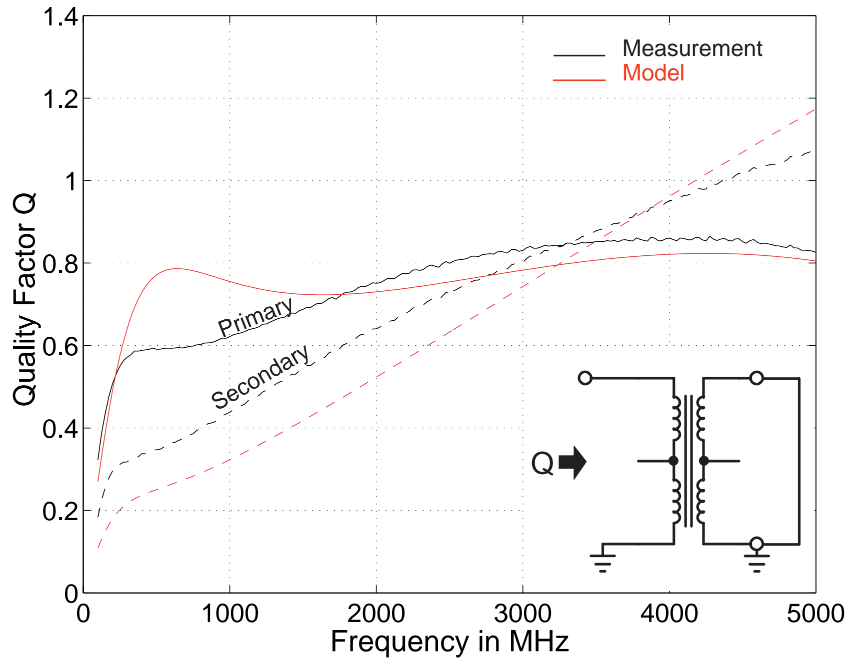

Figure 4.11: Quality factor with short at the secondary-side of the transformer *BL62S005*.

4.2 Monolithic Transformer *N3M2*

The monolithic transformer *N3M2* has a high frequency performance due tue small outer dimensions. Fig. 4.12 shows the planar winding scheme and the schematic symbol of the transformers. Three primary turns P1-P3 are connected in series. Two secondary turns S1,S2 are also connected in series which results in a turn ratio of $n = 3 : 2$. A Center Tap on the secondary side is available.

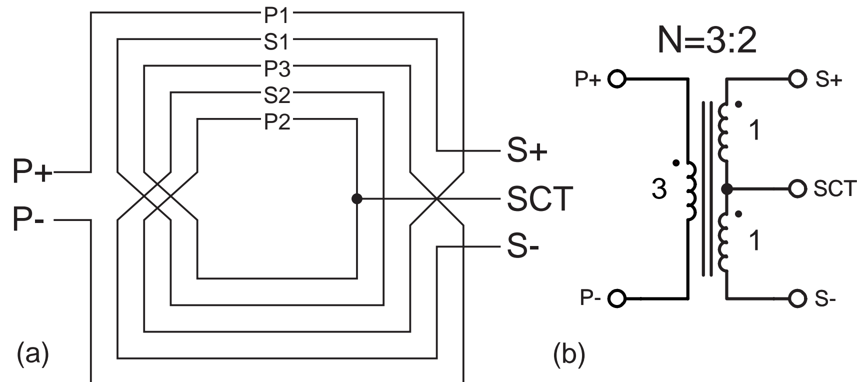

Figure 4.12: High frequency performance transformer *N3M2*: (a) Winding scheme (b) Schematic symbol.

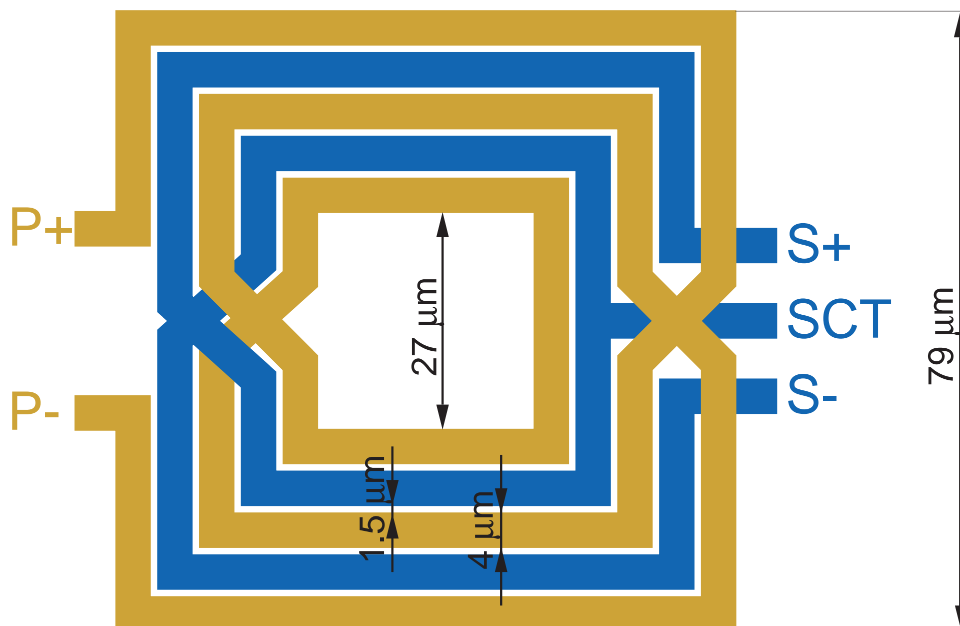

Figure 4.13: Square-shaped high frequency performance transformer *N3M2* with a turn ratio of $n = 3 : 2$.

The physical layout of the monolithic transformer is illustrated in Fig. 4.13. The primary ports, P+ and P-, are located on the left side. The secondary ports, S+, SCT and S-, are located on the right side. The transformer design is completely symmetric about a line. The outer dimensions are $79 \times 79\,\mu\text{m}^2$ and the inner dimensions are $27 \times 27\,\mu\text{m}^2$. The lateral spacings between the turns is $1.5\,\mu$m. The conductor-width is $4\,\mu$m of each turn.

The layer construction of the transformer is kept simple. Metal 3 and metal 2 are connected in parallel in both windings, primary and secondary. The windings are separated to the substrate by H_{OX}=3.2 μm.

4.2.1 Measurement and Simulation Results up to 20GHZ

The equivalent circuit of the high frequency performance transformer *N3M2* is shown in Fig. 4.14. All parameter values are extracted by simulation with *Fast-Trafo*.

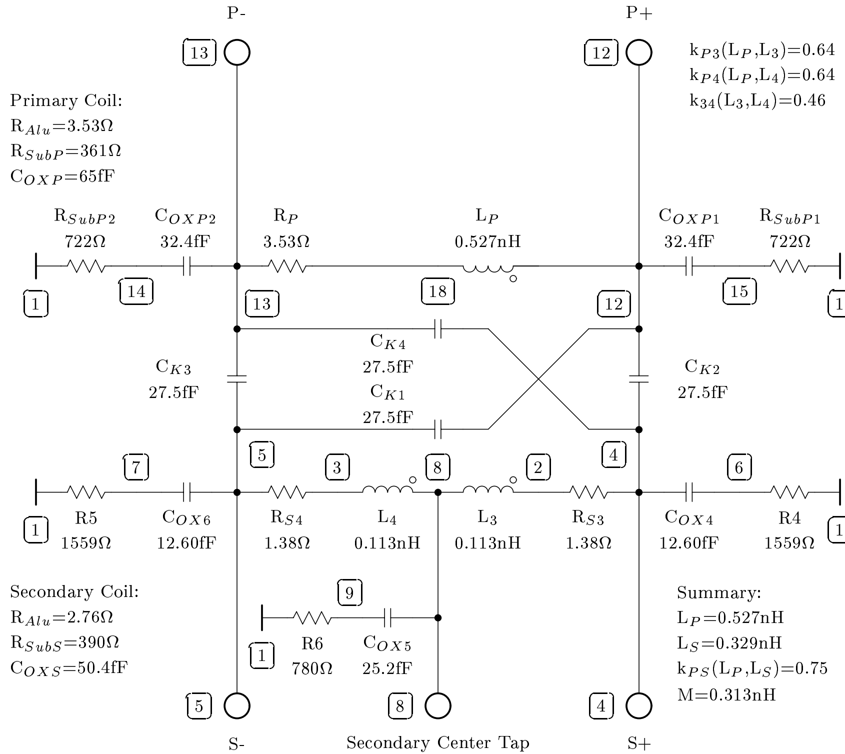

Figure 4.14: Equivalent circuit of the transformer *N3M2*.

The values of the primary and secondary self inductance are

$$L_P = 0.527\,\text{nH}$$
$$L_S = L_3 + L_4 + 2\,k_{34}\sqrt{L_3\,L_4} = 0.329\,\text{nH}$$

The strength of magnetic coupling between primary and secondary side denoted by the k-factor is

$$k_{PS} = \frac{k_{P3}\sqrt{L_P\,L_3} + k_{P4}\sqrt{L_P\,L_4}}{\sqrt{L_P\,L_S}} = 0.75$$

The series resistance of the conductors on the primary side is $R_{Alu} = 3.53\,\Omega$ and on the secondary side $R_{Alu} = 2.76\,\Omega$. The parasitic capacity of the primary winding is $C_{OXP} = 65\,\mathrm{fF}$. The secondary has a bit small value of $C_{OXS} = 54\,\mathrm{fF}$. The substrate resistances of the primary winding is $R_{SubP} = 361\,\Omega$ and in the same range compared to the secondary winding which has a substrate resistance of $R_{SubP} = 390\,\Omega$.

The transformer is placed as a test structure on silicon (Fig. 3.17) to measure the scattering parameters of the primary and secondary coil as well as of the primary-to-secondary transmission. The center tap is left open. De-embedding was done with an open-test-structure.

Fig. 4.15 shows the measured and simulated reflection S11 and S22 of the high frequency performance transformer *N3M2*. The transformers S11 and S22 shows a nearly short circuit at low frequencies (50 MHz). Measurement and model shows good agreement up to 20 GHz.

Fig. 4.16 shows the real and imaginary part of S21. The insertion loss is about 3 dB at 15 GHz. The difference between simulation and model is acceptable.

Fig. 4.17 shows primary inductance L_p and secondary L_s as a function of frequency. The secondary self inductances is analyzed using

$$L_S = L_3 + L_4 + 2\,k_{34}\sqrt{L_3\,L_4} = \mathrm{Im}\left(Z_{22}\right)/\omega \tag{4.7}$$

Simulated and measured self resonance is at 20 GHz.

Analyzing the coupling coefficient as a function of frequency the relation

$$M = k_{P3}\sqrt{L_P\,L_3} + k_{P4}\sqrt{L_P\,L_4} = \sqrt{(Y_{11}^{-1} - Z_{11})\frac{Z_{22}}{\omega^2}} \tag{4.8}$$

is useful. Then the coupling coefficient can be written as

$$k(L_P, L_S) = \frac{M}{\sqrt{L_P L_S}} = \sqrt{\frac{(Y_{11}^{-1} - Z_{11})Z_{22}}{Im(Z_{11})Im(Z_{22})}} \tag{4.9}$$

Fig. 4.18 shows the coupling coefficient versus frequency. The simulated k-factor differs from the measured k-factor. The reason is a missing short-test-structure for correct de-embedding. There is a difference of about 0.1 over the whole frequency

range. The incorrect de-embedding is also visible in the transmission S21 and the Q-factor. It shows the importance of the test-structures for measurement.

The quality factor is analyzed using the following expressions

$$Q = \mathrm{Im}\left(Z_{11}\right)/\mathrm{Re}\left(Z_{11}\right) \tag{4.10}$$

$$Q = \mathrm{Im}\left(Y_{11}^{-1}\right)/\mathrm{Re}\left(Y_{11}^{-1}\right) \tag{4.11}$$

Fig. 4.19 shows the characteristic Q-factor of the primary and secondary winding. Therefore, the output is left open. Fig. 4.20 shows the quality factor of the transformer with shorted output. This is an important case because of the low input impedance of the output stage.

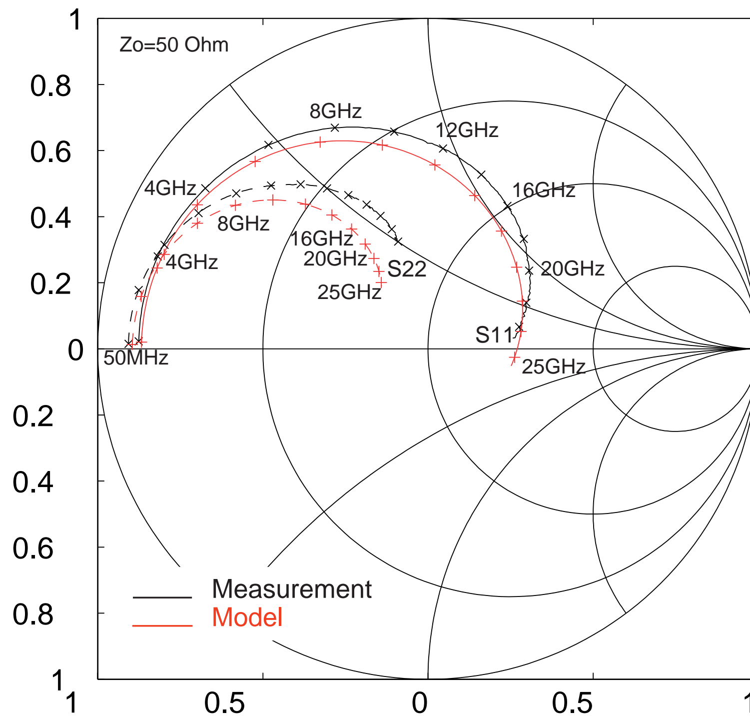

Figure 4.15: Scattering parameters S11 and S22 of the transformer *N3M2*.

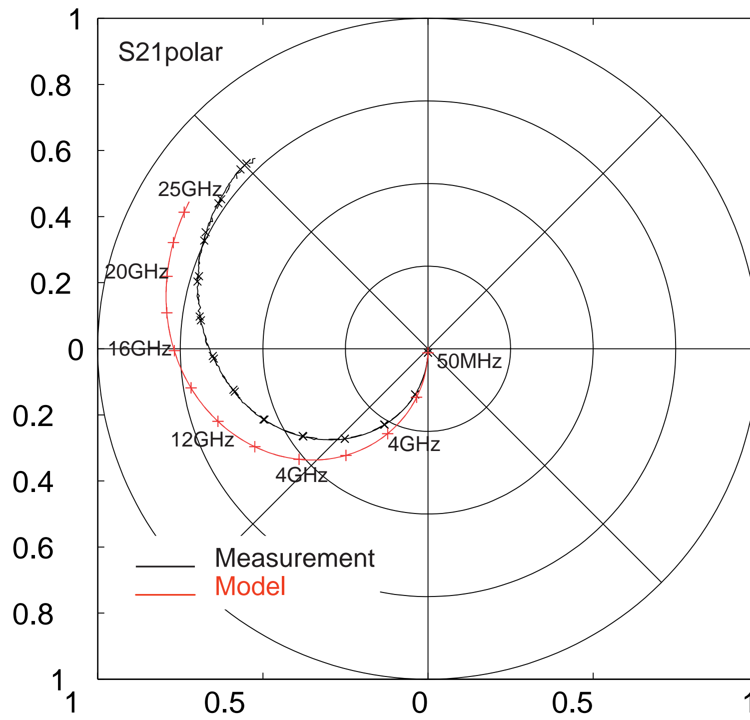

Figure 4.16: Transmission S21 in polar-diagram of the transformer *N3M2*.

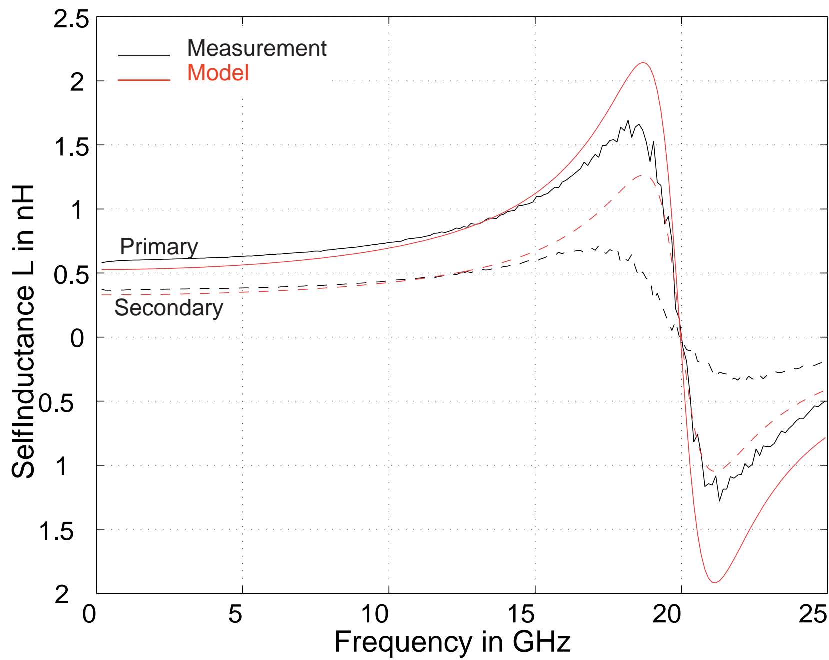

Figure 4.17: Self inductances of primary and secondary winding of the transformer *N3M2*.

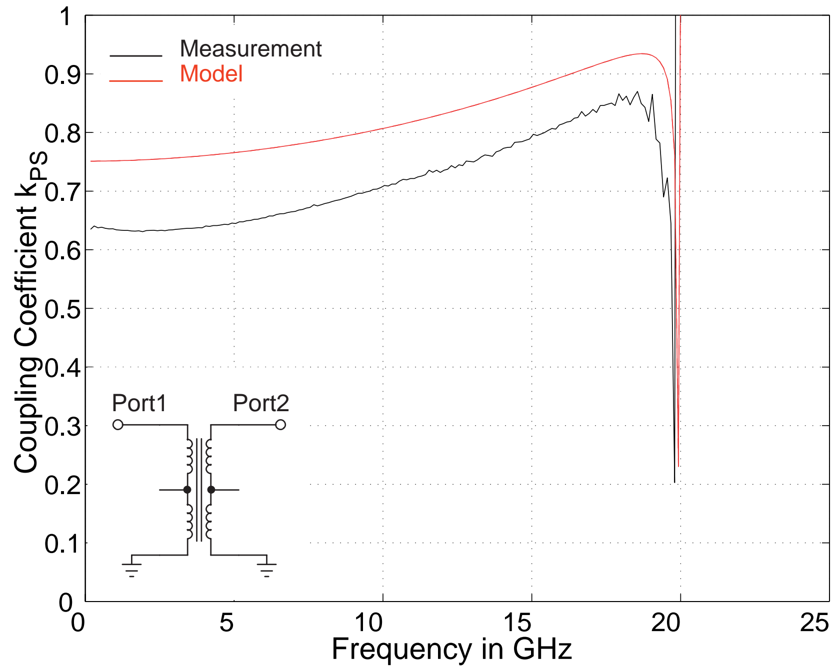

Figure 4.18: Coupling coefficient k over frequency of the transformer *N3M2*.

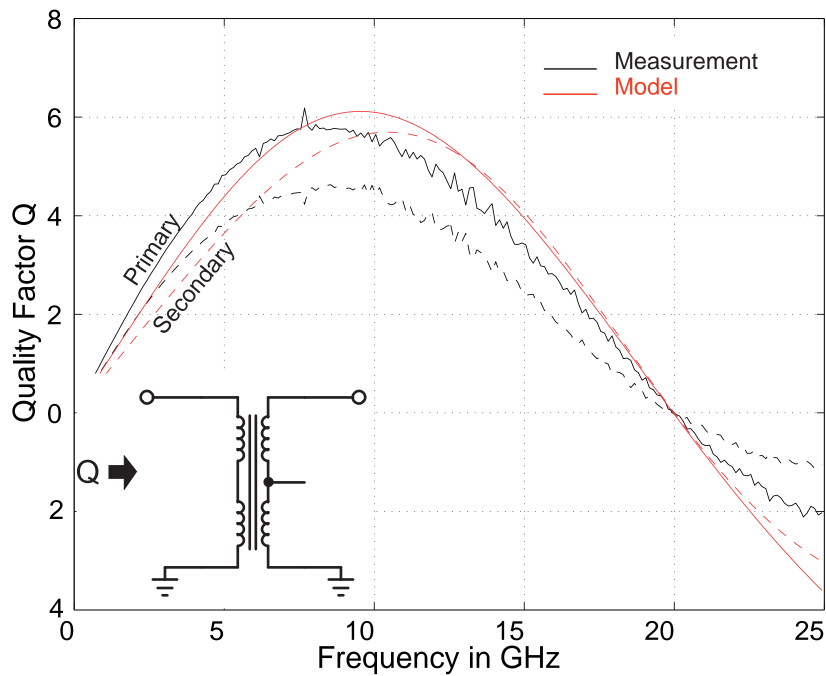

Figure 4.19: Quality factor with open at the secondary-side of the transformer *N3M2*.

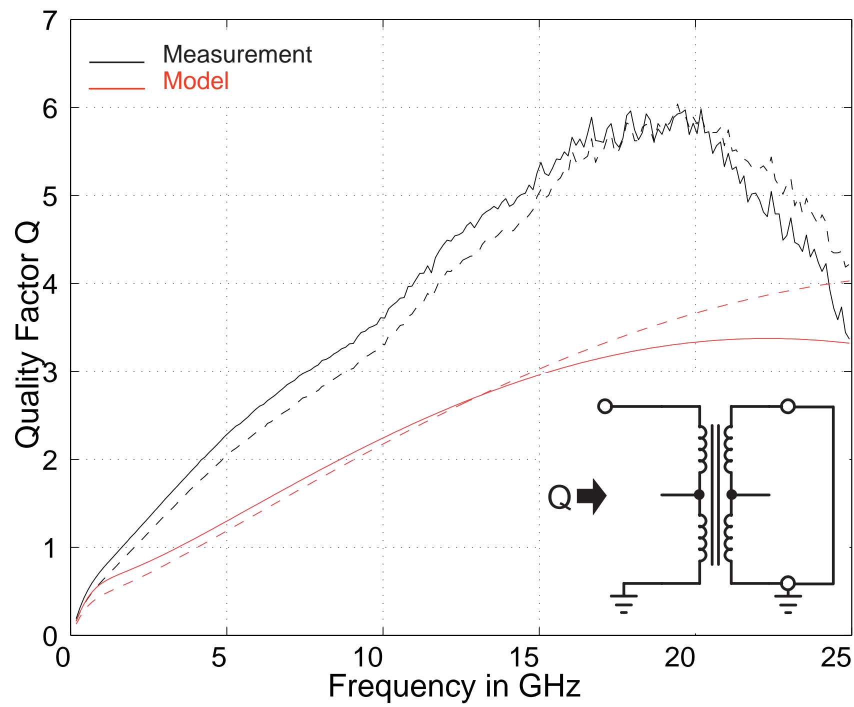

Figure 4.20: Quality factor with short at the secondary-side of the transformer *N3M2*.

Conclusion

Various types of monolithic lumped planar transformers fabricated on silicon based technologies have been presented. Many aspects of design possibilities and optimization techniques are treated in this work. The discussed design rules are valid for general designs of monolithic transformers. The designer is able to optimize a lot of parameters in order to make an intelligent design compromise.

The aim of precise and fast transient analysis of RF circuits using monolithic transformers was achieved with a compact lumped low order model which was derived from the physical layout and process technology. The complexity of this model is low enough and the precision is high enough to perform fast and accurate analysis of the integrated circuits in order to make quick design processes.

A method for parameter extraction and background details about all elements used in the equivalent-circuit have been presented. The full electrical behaviour derived from complex transformer geometries can be accurately predicted.

The method for characterization of monolithic integrated lumped planar transformers has been verified by multiple transformers. Two transformers are considered in detail from computer simulation and experimental results. The model and the measurement show excellent agreement.

Now it is possible to predict the electrical characteristic of monolithic transformers up to 20 GHz. The designer is able to use such elements in the RF-circuits including all advantages of transformers. This work has shown the complete modeling and simulation of monolithic lumped planar transformers .

FastTrafo Manual

Introduction

This manual describes *FastTrafo*, a parameter extraction program for monolithic integrated lumped transformers and inductors. *FastTrafo* computes self and mutual inductance, resistance and capacity between primary-, secondary-winding and substrate. It finally displays a characterization of the transformer. The computation is done by *FastHenry* and *FastCap*. For further information look at the *FastHenry*- and *FastCap*-manual.

The manual is divided into four sections. The first section explains the handling of the graphic interface. The interface creates a input file for *FastTrafo* which contains the description of the transformer geometries. The second section shows how to create a technology file. The technology file contains all necessary information of the semiconductor process. The third sections subject are the outputs of *FastTrafo*. The fourth section lists the system requirements to run *FastTrafo*.

How to Prepare a Input File

The Graphic Interface

The graphic interface (Figure 4.21) provides you an easy input to the computer and gives you valid choices for several inputs. It is also possible to write a input-file for *FastTrafo* on a text-editor. The input file specifies the transformer or inductance **geometries** and the **simulation** settings. The following sections explain each input necessary to run *FastTrafo*.

The Geometry Inputs

- **Technology**
  The pop-up menu gives you a list of available technology-files. For each technology it must exist a description of the dielectric- and metal-layers and its characteristics. How to write such a technology-file is explained in section 4.2.1.

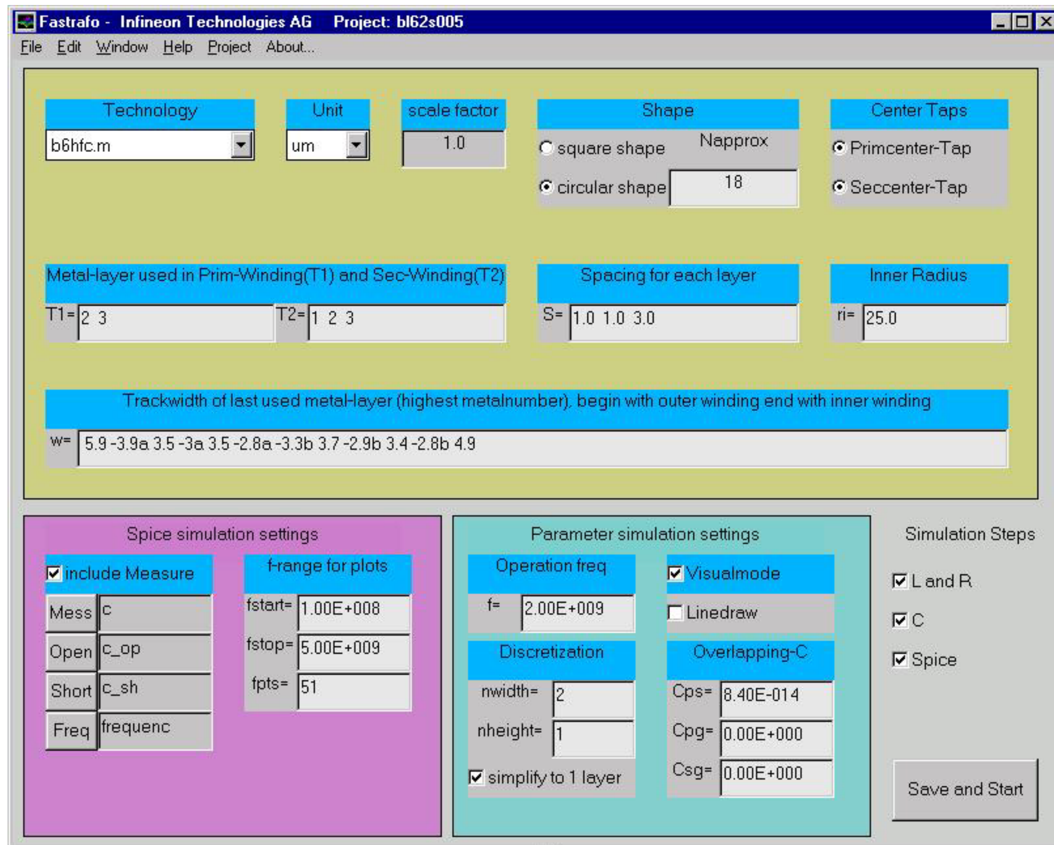

Figure 4.21: The Graphic Interface of *FastTrafo*

- **Unit**
  Choose the unit you want to use for the geometric input.

- **Scale-Factor**
  All lengths of the input are multiplied with the scale-factor. A very useful tool to shift the operation frequency of the transformer. There is also a little rule check implemented. If the spacing between two windings is smaller than allowed it is set to the minimal allowed spacing.

- **Shape**
  You can choose rectangular- or circular-shape for your design. If you use circular-shape you have to give the number of segments **Napprox** which approximate the circle. Note that Napprox must be a even number. A useful range for Napprox is from 6 up to 20.

- **Center Taps**
  It is recommended to select primary- and a secondary center taps. The Spice simulation supports only the mode with two center taps. The inductance values and the coupling coefficients without center taps can be calculated

with Formula 4.12-4.14. They are printed in the TEX-documentation. How to produce the TEX-documentation see Section 4.2.1.

$$L_P = L_1 + L_2 + 2\,M_{12} = L_1 + L_2 + 2\,k_{12}\sqrt{L_1\,L_2} \tag{4.12}$$

$$L_S = L_3 + L_4 + 2\,M_{34} = L_3 + L_4 + 2\,k_{34}\sqrt{L_3\,L_4} \tag{4.13}$$

$$k_{PS} = \frac{k_{13}\sqrt{L_1\,L_3} + k_{14}\sqrt{L_1\,L_4} + k_{23}\sqrt{L_2\,L_3} + k_{24}\sqrt{L_2\,L_4}}{\sqrt{L_P\,L_S}} \tag{4.14}$$

- **Metal-Layers**
  $T1$ and $T2$ specify which metal-layers are used for the primary and secondary side. Type in the metal-numbers separated by spacings you want to use. Syntax:

```
T1= <metal-number> <metal-number> ...
T1= 2 3  Metal-layer 2 and 3 are used for the primary winding
```

- **Spacing**
  S is a vector containing the spacing between two traces for each metal-layer. Begin with the first metal-number and end with the highest metal-number. Note that you have to begin with the first metal-number although it is maybe not used in your design. If you don't specify all spacings or set them smaller than allowed they are set to the minimal spacing. Syntax:

```
S= <spacing metal 1 > <spacing metal 2 > <spacing metal 3 > ...
S= 1.5  1.5  3.0
```

  In the example above the spacing between two traces in metal-layer 1 is 1.5 *units*. In metal-layer 3 it is 3 *units* and in all others the minimal spacing is used. The minimal allowed spacing is defined in the technology-file (section 4.2.1).

- **Trackwidth**
  w is a string which contains substrings for each winding. The substrings are separated by spacings and include the information about primary- or secondary winding, the trackwidth and the group of each winding.The string begins with the substring of the outer winding and ends with the inner winding of the transformer or coil. The values given for the trackwidth are associated and valid for the last metal-layer (highest metal-number) used in the transformer design. Syntax:

```
w = <+/-><width><group> <+/-><width><group> ......
w= 5.9 -3.9a 3 -3.5a
```

Each substring starts with a float number, which is the trackwidth of the winding. A positive number means a primary winding and a negative number a secondary winding. The trackwidth can be followed by a group-string. All windings with the same string are connected in parallel.
In this example the transformer has four windings. The outer winding is a primary winding with a trackwidth of 5.9 *units* followed by a secondary winding with a trackwidth of 3.9 *units*. The second and the fourth winding have the same group-string and are switched together. Between the two secondary windings is a primary winding with 3.0 *units* trackwidth. The example-transformer above has a turn ratio of 2 : 1.

- **Inner Radius**
  The inner radius specifies the hole in the middle of the transformer. If square shape is selected the inner radius is half the sidelength of the square. Figure 4.22 shows the definiton of *ri*.

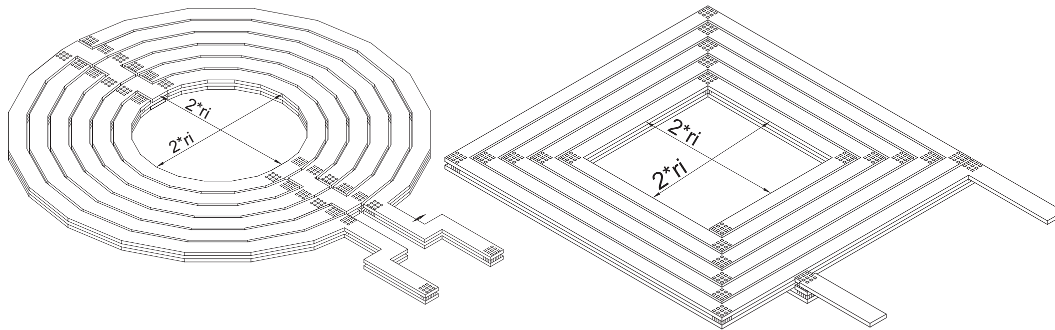

Figure 4.22: Definition of the inner radius in square and circular shape

The Simulation Inputs

- **Include Measure**
  You can include a measurement of your transformer. Measurement and simulation is plotted in one diagram. A comparison between simulation and measurement shows the quality of the transformer model. It is possible to calibrate the pads with the **Open** and **Short**-file to minimize the measurement-error.

- **Operation frequency**
  The parameters for the lumped equivalent circuit (Figure 4.30) are calculated only for the operation frequency. This model is sufficient enough to get good simulation results. Generally the parameters are a a function of the frequency.

- **Discretization**
  Each segment of the transformer is discretized into filaments. Figure 4.23 shows the discretization done by *FastHenry* and Figure 4.24 done the discretization made by *FastCap*.

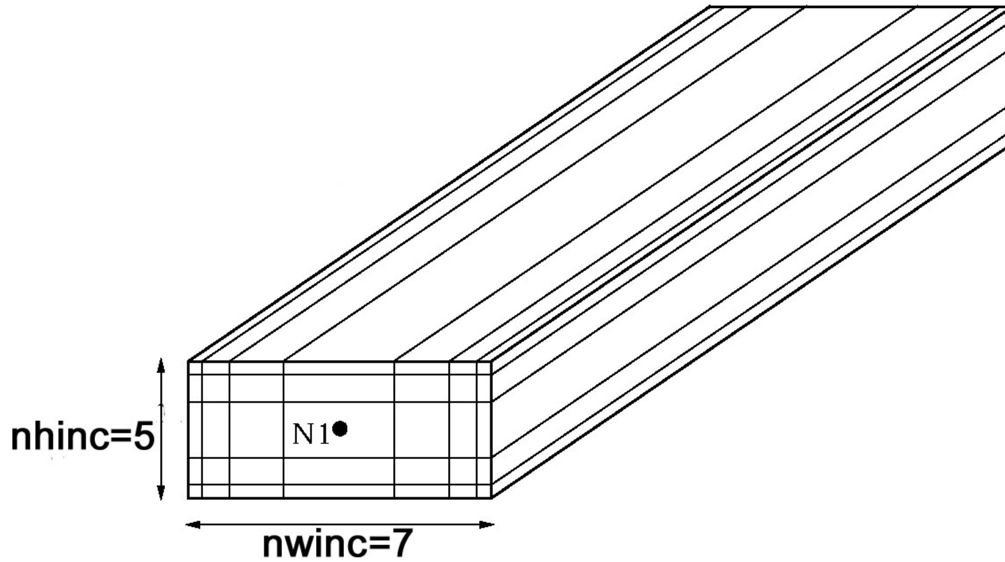

Figure 4.23: Segment discretized by *FastHenry* into 35 filaments

- **nwidth** is the number of filaments in width and **nheight** the number of filaments in height. *FastHenry* uses different numbers of filmanents in height and width. In *FastCap* the number of filaments are in width and height the same and therefore the greatest number of nheight and nwidth is used. In addition *FastCap* discretizes the segment also in length.

  Be aware of too high values for nwidth and nheight. It directly rises memory consumption and simulation time. A useful range is up to 6 filaments in each direction and depends on the total number of segments.

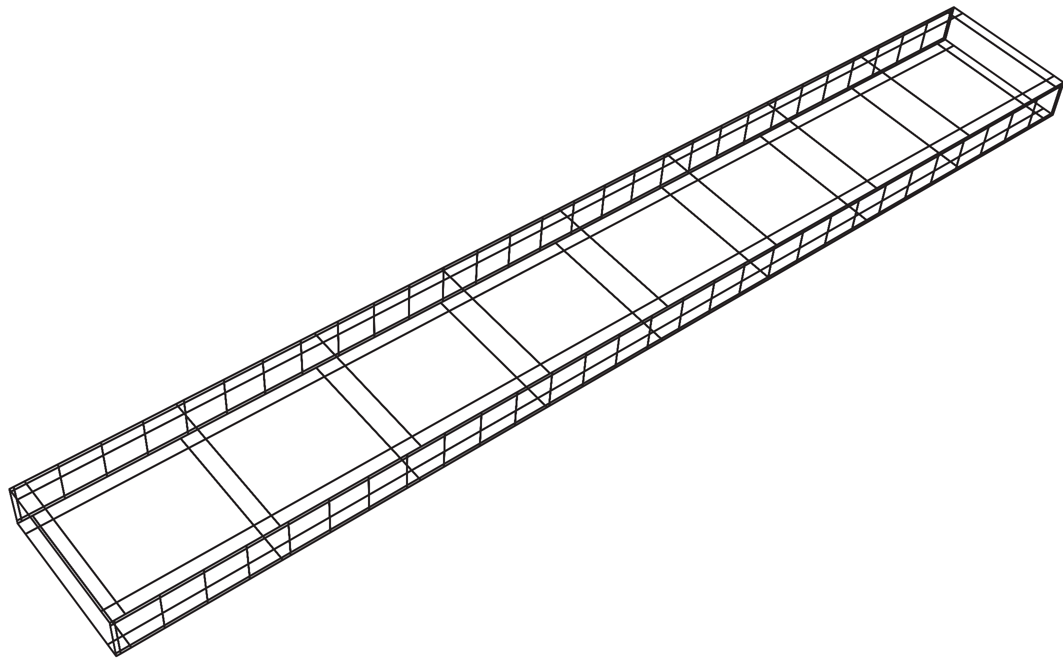

Figure 4.24: Segment discretized by *FastCap*

- **Visualmode**
  In visualmode *FastHenry* and *FastCap* produce Postscript-pictures of the transformer or inductor. It should help you to verify the geometry inputs and the winding scheme. *FastCap* produces a cross-section (Figure 4.25, Figure 4.26) of the design. You can check the layers, spacings and the trackwidth. *FastHenry* shows the whole transformer (Figure 4.27). The **linedraw**-button produces a winding-scheme (Figure 4.28).

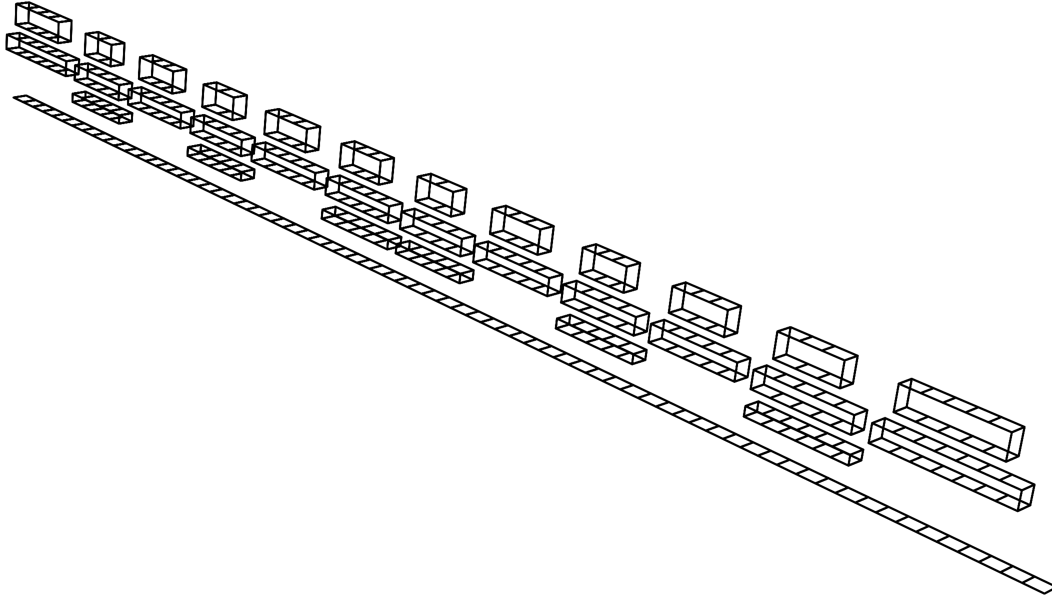

Figure 4.25: 3-D-Crossection of the transformer Bl62s005

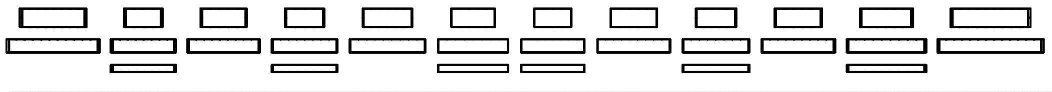

Figure 4.26: 2-D-Crossection produced by *FastCap*

- **Overlapping-C**
  In this manual the area where the traces cross each other is called cross-area. The cross-area can be layouted in various ways and is very design specific. So it makes no sense to automate the calculation of the cross-area-capacity. It belongs to you to make an estimation about the capacity. **Cps** is the capacity from the overlapping primary- and secondary-traces. **Cpg** is the capacity from primary-traces to substrate. **Csg** is the capacity from secondary-traces to substrate. This capacities are only in addition instead of the cross-area-capacity. If you set them to zero the calculated capacity is too small but a good enough estimation to see the characteristics of the design.

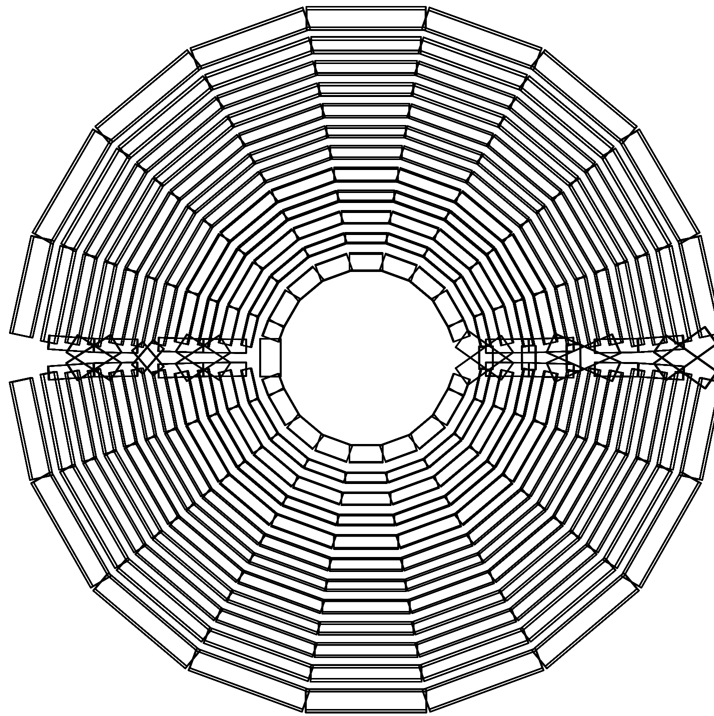

Figure 4.27: The whole transformer Bl62s005

Plain Input-File

It is also possible to write a input-file for *FastTrafo* on a text editor. The filename must not be longer than 8 characters and is a M-file which means the extension is ".m". You have to create a new directory in the project directory. The directoryname must be the same as the filename without extension. Here is an example of a input-file for *FastTrafo*. The definitions are explained before in Section 4.2.1.

```
unit='um';  % possible units: km, m, cm, mm, um
Tech_Name='h:\ftrafo\tech\b6hfc'; %Path and Name of technologyfile

square_shape=0; % For Square-Geometry =1, Circular-Geometry=0
scale_factor=1.00; % All length are multiplied with scale_factor
ri=25.00;      % Inner radius

T1=[2  3];  % Metal-layer included in  primary winding
T2=[1  2  3];   % Metal-layer included in secondary winding

S=[1  1  3]; % Spacing [1-metal 2-metal 2-metal ...]

% Trackwidth of last used metal-layer (highest metalnumber)
% Begin with outer winding end with inner winding)
```

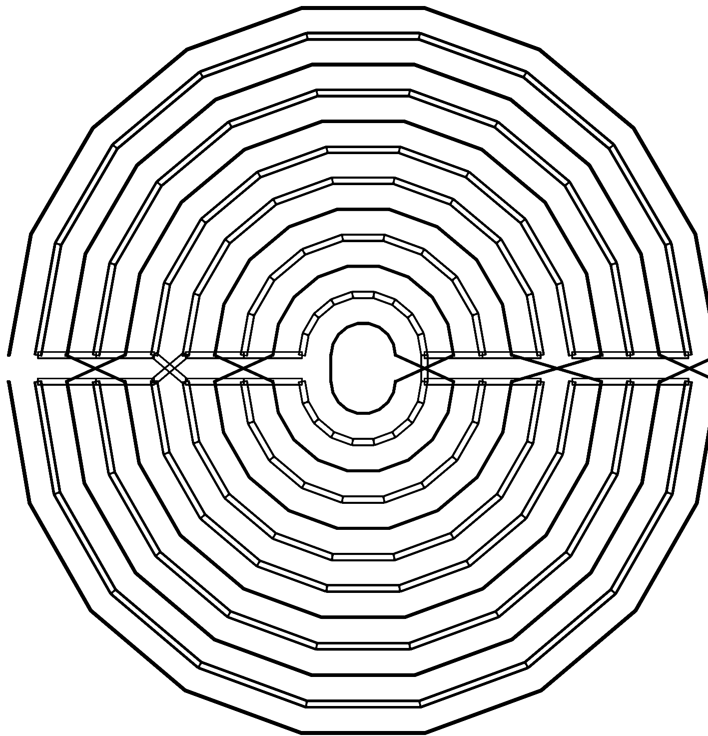

Figure 4.28: Winding scheme of the transformer

```
w=' 5.9 -3.9a 3.5 -3a 3.5 -2.8a -3.3b 3.7 -2.9b 3.4 -2.8b 4.9' ;

Napprox=18 ;    %Circular-shape is approximated with Napprox-parts

Primcenter=1 ;  %Primcenter=1 -> with  primary Centertap
Seccenter=1 ;   %Seccenter=1  -> with  secondary Centertap

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Simulation parameters
visualize=0 ; % For Visualization-Mode =1; No Simulation !!!!
linedraw=0 ;  % if =1 Visualization is a linedraw

simplify=1 ;  % Simplified Calculation only one metal in fasthenry
nwinc=2 ;     % Number of discretized filaments in width
nhinc=1 ;     % Number of discretized filaments in height

% Frequencyrange for Simulation
fbeg=2.00E+009 ; %Begin-Frequency
fend=2.00E+009 ; %End-Frequency
ndec=2 ;         % Points per decad
```

```
cps=8.40E-014 ;  % Additional Capacity in Crossarea
cpg=0.00E+000 ; csg=0.00E+000;

% Frequencyrange for Matlabplots (trafo.m)
fstart=1.00E+008 ;   % Start frequency
fstop=5.00E+009 ;    % Stop frequency
fpoints=5.10E+001 ;  % Number of points

fmarkers=1.00E+009 ; % Markerdistance in Smith-Chart
fmess=2.00E+009 ;    % Operation-frequency

% Mess-files (if not given set to '')

mess_include=1 ; % if =1 include Messfiles
Mess_path='h:\ftrafo\projects\bl62s005\v1\' ; % Path of Mess-files
Mess_Name='c' ; % Name of Mess-file (without extension)
open_name='c_op' ; % Name of Open-file
short_name='c_sh' ; % Name of Short-file
freq_name='frequenc' ; % Name of Frequency-file
```

How to Create a Technology-File

This section describes how to create a technology-file for a certain semiconductor process. The technology-file will be explained with the example of the B6HFC-Process.

Building a Technology-File

The technology-file consists of several definitions which describe the metallization of the process. In Section 4.2.1 an example of a technology-file is explained . All characters after a leading %-character are comments and no definitions.

- **Length-Unit**
  First you have to specify the **length-unit** for the inputs. Possible units are m, cm, mm and μm. Syntax:

  ```
  Techunit='<unit>';
  ```

- **Dielectric-Layers**
  Now you can define the **dielectric-layers**. Each layer is specified in one line and you can define as many layers as you want. Syntax:

```
D(<layer-number>,:)=[<Z-coord> <height> <relative-permittivity> ];
```

The dielectric-layers are sorted and numbered with increasing `z-coordinate`. The dielectric with the lowest `z-coordinate` has the `layer-number` 1 and the dielectric with the highest `z-coordinate` has the highest `layer-number`. $Z = 0$ is defined at the upper edge of the substrate.

- **Substrate**
  The substrate is a non-ideal-dielectric and has a conductivity $[\sigma] = [1S/m]$ as an additional information. Remind that $Z = 0$ is defined at the upper edge of the substrate. Syntax:

  ```
  Sub=[<Height> <relative-permittivity>  <Conductivity>];
  ```

- **Metal-Layers**
  Each metal-layer is specified in one line and you can define as many layers as you want. Syntax:

  ```
  M(<layer-number>,:)=[<Z-coordinate> <height> <min-spacing>];
  ```

  The metal-layers are sorted and numbered with increasing `z-coordinate`. The metal with the lowest `z-coordinate` has the `layer-number` 1 and the metal with the highest `z-coordinate` has the highest `layer-number`. `Min-spacing` is the minimal allowed distance between two traces in the actual metal-layer.

- **Conductivity**
  The conductivity $[\sigma] = [1S/m]$ of the metal-material is set by `sigma`. Syntax:

  ```
  sigma=<metal-conductivity>;
  ```

Example: B6HFC-Process

The metallization of the B6HFC-Process with all metal- and dielectric-layers is shown in Figure 4.29. The B6HFC-Process has three metal layers, Alu1, Alu2 and Alu3. The conductor material is aluminium and has a conductivity of $\sigma = 33S/\mu m$. The first dielectric layer has an $\varepsilon r = 3.9$ and a thickness of $6.45\mu m$. The second dielectric layer, the passivation, has an $\varepsilon r = 7.5$ and a thickness of $0.55\mu m$. The substrate is $200\mu m$ thick, the conductivity is $\sigma = 12.5S/m$. The relative permittivity of the substrate is $\varepsilon r = 11.9$. The following file-list is the complete technology-file for the B6HFC-process.

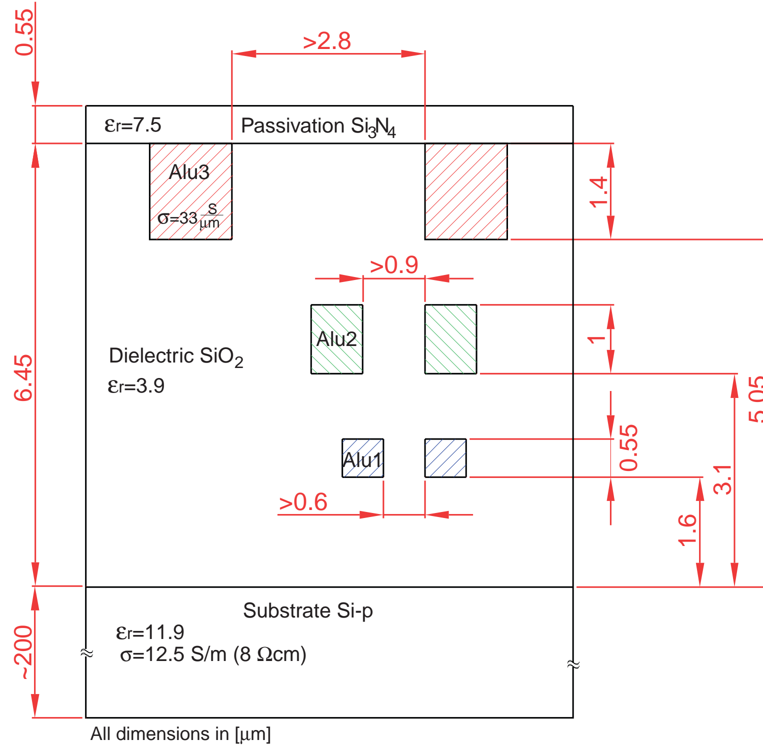

Figure 4.29: Metallization of the B6HFC-process

```
% Techfile for B6HFC

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%General Settings

Techunit='um';  % possible units:  m, cm, mm, um

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Dielectric
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Note: Z-Cor is defined at the bottom-edge  of the object
%    Z=0   is defined at the upper-edge   of the substrat


%       Z-Cor   Height   Er
D(2,:)=[6.45    0.55     7.5  ];    % Pass
D(1,:)=[0       6.45     3.9  ];    % Oxid

%    Height    Er       Conductivity(S/m)
Sub=[200       11.9     12.5];    % Substrat
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Metal layers
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%       Z-Cor   Height Spacingmin
M(3,:)=[5.05    1.4    2.8     ];   % Alu3
M(2,:)=[3.1     1      0.9     ];   % Alu2
M(1,:)=[1.6     0.55   0.6     ];   % Alu1


sigma=33e6;    % Conductivity(S/m) of Conductor
```

Simulation Outputs

The Lumped-Equivalent-Circuit

The simulation with *FastHenry* and *FastCap* extracts the parameters for the lumped equivalent circuit (Figure 4.30). *FastHenry* computes self and mutual inductance between primary-, secondary-winding and the series resistance of the windings The capacity between primary-, secondary-winding and substrate is calculated by *FastCap*. This model is sufficient enough to get good simulation results. Generally the parameters are a a function of the frequency.

FastTrafo creates a spice-netlist of the equivalent circuit which is then simulated in SPICE.
Please note that the spice simulation is only available for transformers and not for inductors.
The output are three plots. S-Parameter, Z-Parameter, and 1/Y-Parameter of the transformer.

TEX-Documentation

After the SPICE-Simulation is done, *FastTrafo* produces a file named `main.tex`. This file can be compiled with a version of LATEX. The result is a short documentation of the transformer including the lumped-equivalent-circuit and plots of the S-Parameter, Z-Parameter, and 1/Y-Parameter.

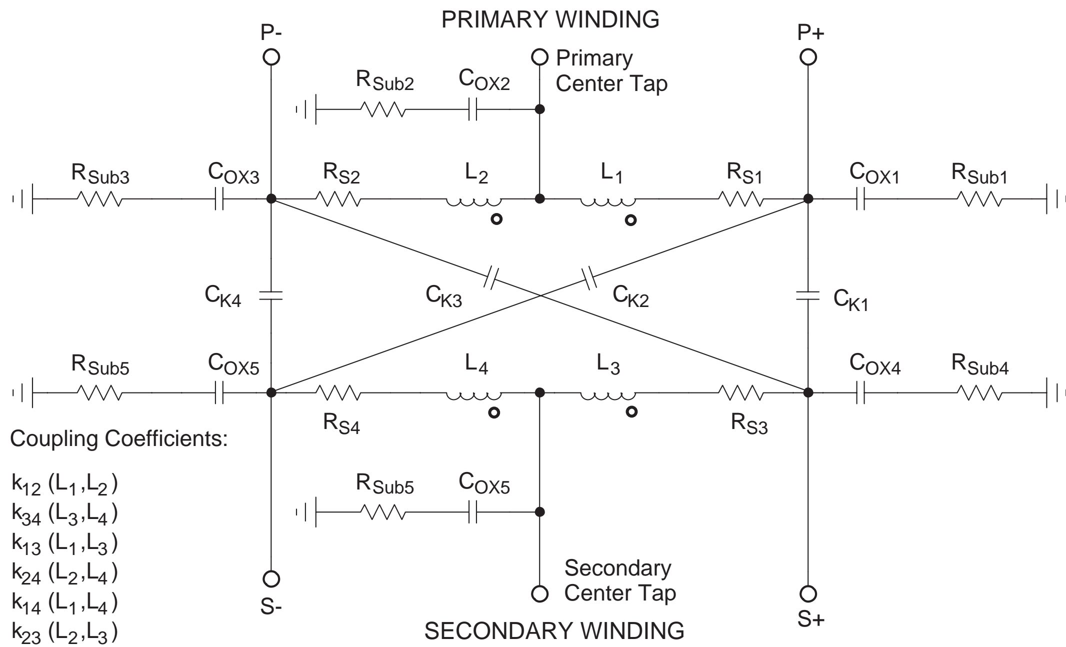

Figure 4.30: The Lumped-Equivalent-Circuit of the transformer.

System Requirements

Hardware Requirements for *FastTrafo*

Processor:
To get enough processor power for the inductance- and capacitance-simulation a *Pentium-II-Processor* or a equivalent processor should be installed.

RAM:
For the inductance-simulation the memory consumption is no problem. To avoid a run out of memory during the capacitance-simulation it is recommended to install at least 256 MB RAM.

Harddisk:
The maximum installation needs 45 MB Diskspace.

Software Requirements for *FastTrafo*

Matlab:
FastTrafo is written in Matlab-Language. It was tested with *Matlab* Version 5.1, other versions may work only with significant errors.

IsSpice4:
For the simulation of the lumped-equivalent-circuit IsSpice4 is required.

FastHenry:
For the inductance-simulation *FastHenry* (included Shareware) is required.

FastCap:
For the capacitance-simulation *FastCap* (included Shareware) is required.

Latex:
To compile the documentation-file a version of Latex is needed.

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