CHAPTER 7
SIMULATIONS AND PRACTICAL DESIGNS OF FLYBACK CONVERTERS

The flyback converter probably represents the most popular structure found on the market. The vast majority of consumer products make use of this converter: notebook adapters, DVD players, set-top boxes, satellite receivers, CRT TVs, LCD monitors, and so on. Three traits can justify this success: simplicity, ease of design, and low cost. For many designers, the flyback converter remains synonymous with poor EMI signature, large output ripple, and large-size transformers. After this fair warning, let us first discover how a flyback works before we go through several design examples.

7.1 AN ISOLATED BUCK-BOOST

If you remember the buck-boost converter (Fig. 1-38), you will certainly notice that the flyback takes its inspiration from this arrangement (Fig. 7-1).

The buck-boost delivers a negative voltage referenced to the input ground, without isolation. By swapping the inductor and the power switch, a similar arrangement is kept, but this time referenced to the input rail. Finally, coupling an inductor to the main one via a core, we obtain an isolated flyback converter. The secondary diode can be in the ground path (as shown), or in the positive wire, as more commonly encountered.

As with the nonisolated buck-boost, the energy is first stored from the input source during the on time. At the switch opening, the inductor voltage reverses and forward biases the catch diode, routing the inductor current to the output capacitor and the load. However, as the inductor and the load share the same ground, the output voltage is negative. On the flyback, a coupled-inductor configuration helps to adopt the needed polarity by playing on the winding dot positions and the diode orientation: the output voltage can be either positive or negative, above or below the input voltage, by adjusting the turns ratio. Physically separating the windings also brings galvanic isolation, needed for any mains-connected power supplies. *Galvanic?* Yes, this term relates to the physicist Luigi Galvani (1737–1798, Italy), who discovered the action of electric currents on nerves and muscles. So if you do not want to reiterate his experiments, you'd better watch the ability of the selected transformer to block any leakage current!

Further to this historical digression, let us purposely separate both the on and off events to see which exactly plays a role. Figure 7-2a portrays a parasitic-elements-free flyback when the power switch is closed. During this time, the voltage across the primary inductance L_p is equal

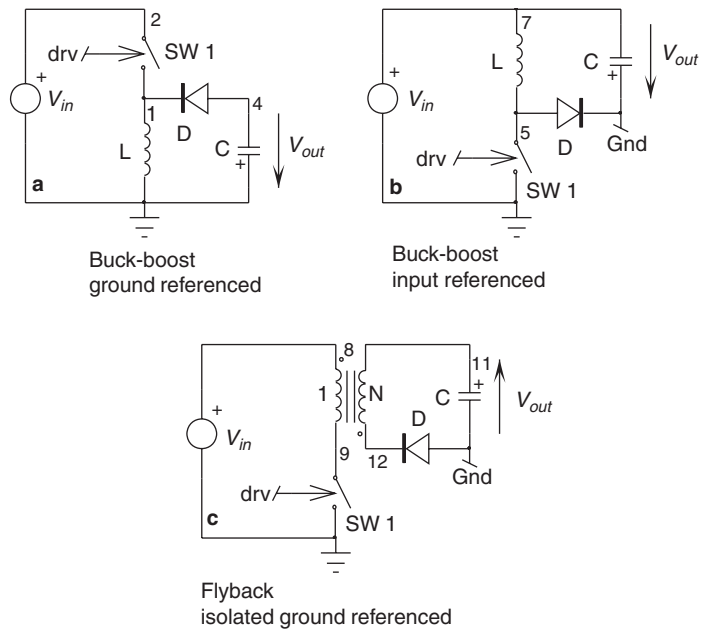

FIGURE 7-1 Rotating the buck-boost inductor leads to the flyback converter.

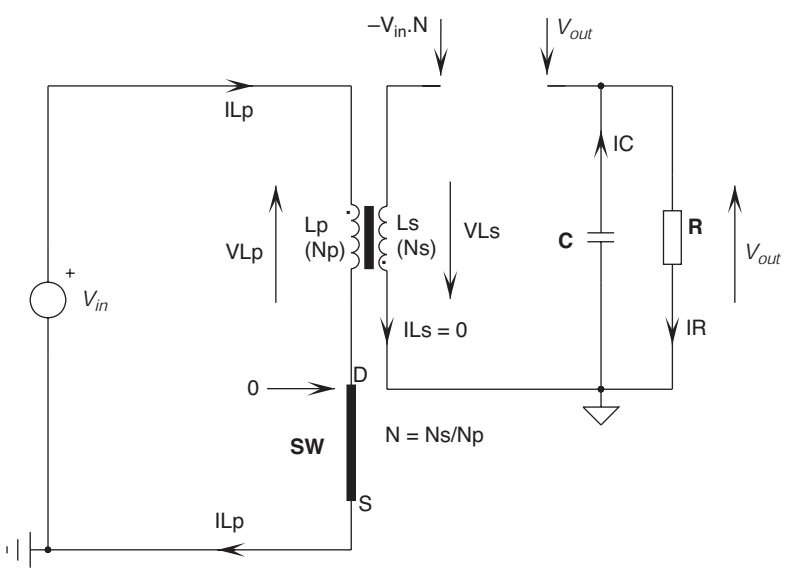

FIGURE 7-2a During the on time, the output capacitor supplies the load on its own.

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to the input voltage (if we neglect the switch voltage drop). The current in this inductor increases at a rate defined by

$$S_{on} = \frac{V_{in}}{L_p} \tag{7-1}$$

Associating the on time t_{on} and the valley current, Eq. (7-1) can be updated to define the peak current value

$$I_{peak} = I_{valley} + \frac{V_{in}}{L_p} t_{on} \tag{7-2a}$$

Here I_{valley} represents the initial inductor current condition for $t = 0$, at the beginning of the switching cycle (if we are in CCM). If it is zero, as for the DCM case, we have

$$I_{peak} = \frac{V_{in}}{L_p} t_{on} \tag{7-2b}$$

During this time, there is no current flowing in the secondary side inductor. Why? Because of the winding dot configuration: the current enters on the primary side by the dot and should leave the secondary side by its dot as well. However, the diode presence prevents this current from circulating in this direction. During the on time, the dot arrangement on the transformer makes the diode anode swing negative, thus blocking it. As its cathode keeps to V_{out} thanks to the capacitor presence, the *peak inverse voltage* (PIV) undergone by the rectifier is simply

$$\text{PIV} = V_{in}N + V_{out} \tag{7-3}$$

where N is the turns ratio linking both inductors, equal to

$$N = \frac{N_s}{N_p} \tag{7-4}$$

We purposely adopted this definition for N to stay in line with the SPICE transformer representation where the ratio is normalized to the primary. An N ratio of 0.1 simply means we have a 1-to-0.1 turns relationship between the primary and the secondary, for instance, 20 turns on the primary and 2 turns on the secondary.

Because current does not circulate in both primary and secondary inductors at the same time, the term *transformer* is improper for a flyback converter but is often used in the literature (here as well), probably for the sake of clarity. A true transformer operation implies the simultaneous circulation of currents in the primary and secondary sides. For this reason, it is more rigorous to talk about coupled inductors. Actually, a flyback "transformer" is designed as an inductor, following Eq. (4A-20) recommendations.

When the PWM controller instructs the power switch to turn off, the voltage across the primary inductor suddenly reverses, in an attempt to keep the ampere-turns constant. The voltage developed across L_p now appears in series with the input voltage, forcing the upper switch terminal voltage (the drain for a MOSFET) to quickly jump to

$$V_{DS,off} = V_{in} + V_{L_p} \tag{7-5a}$$

However, as the secondary diode now senses a positive voltage on its anode (or a current circulating in the proper direction), it can conduct. Neglecting the diode forward drop V_f, the

secondary-side-transformer terminal is now biased to the output voltage V_{out}. As a matter of fact, since both inductors are coupled, this voltage, translated by the turns ratio 1/*N*, also appears on the primary side, across the primary inductor L_p. We say the voltage "flies" back across the transformer during the off time, as shown in Fig. 7-2b, hence the name *flyback*.

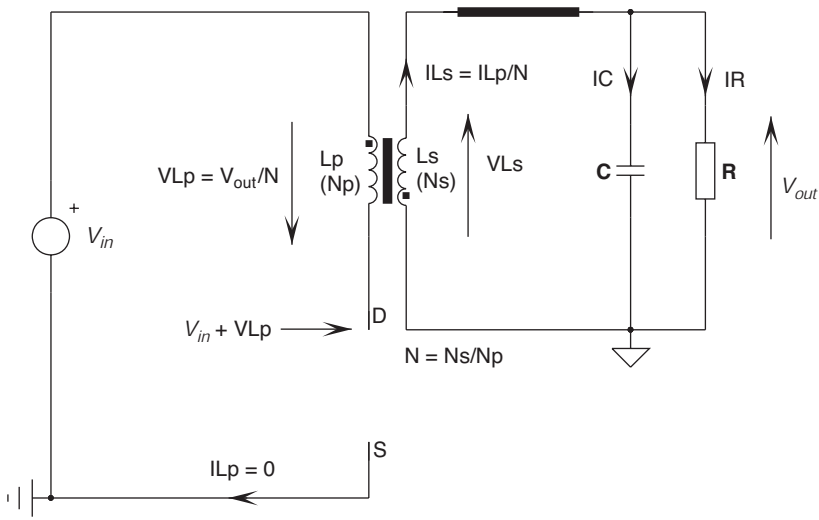

FIGURE 7-2b During the off time, the switch voltage jumps to the input voltage plus the primary inductor voltage.

The switch voltage at the opening is then

$$V_{DS,off} = V_{in} + V_{out}\frac{N_p}{N_s} = V_{in} + \frac{V_{out}}{N} = V_{in} + V_r \tag{7-5b}$$

where V_r is called the *reflected* voltage:

$$V_r = \frac{V_{out}}{N} \tag{7-5c}$$

The voltage applied across the inductor now being negative (with respect to the on-time sequence), it contributes to reset the core magnetic activity. The rate at which reset occurs is given by

$$S_{off} = -\frac{V_{out}}{NL_p} \tag{7-6}$$

By introducing the off-time definition, Eq. (7-6) can be updated to extract the valley current if the flyback operates in CCM:

$$I_{valley} = I_{peak} - \frac{V_{out}}{NL_p}t_{off} \tag{7-7a}$$

For the DCM case, where the inductor current goes back to zero, we have

$$I_{peak} = \frac{V_{out}}{NL_p}t_{off} \tag{7-7b}$$

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If we now combine Eqs. (7-2a) and (7-7a), we can extract the dc transfer function of the CCM flyback controller:

$$I_{valley} = I_{peak} - \frac{V_{out}}{NL_p}t_{off} = I_{valley} + \frac{V_{in}}{L_p}t_{on} - \frac{V_{out}}{NL_p}t_{off} \tag{7-8}$$

Rearranging the above equations, we obtain

$$\frac{V_{out}}{NL_p}t_{off} = \frac{V_{in}}{L_p}t_{on} \tag{7-9}$$

Expressing the duty cycle D in relation to the on and off times, we reach the final definition for CCM:

$$\frac{V_{out}}{V_{in}} = \frac{Nt_{on}}{t_{off}} = \frac{NDT_{sw}}{(1 - D)T_{sw}} = \frac{ND}{1 - D} \tag{7-10}$$

It is similar to that of the buck-boost converter except that the turns ratio now takes place in the expression. Please note that inductor volt–seconds balance would have led us to the result in a much quicker way!

7.2 FLYBACK WAVEFORMS, NO PARASITIC ELEMENTS

To understand how typical signals evolve in a flyback converter, a simple simulation can be of great help. This is what Fig. 7-3a proposes. In this example, the transformer implements the simple T model described in App. 4-B. Figure 7-3b portrays the waveforms delivered by the simulation engine. If we now observe the input current, it is pulsating, exactly as a buck or a buck-boost input waveform. Looking at the diode current, we also observe a pulsating nature, confirming the bad-output-signature reputation of the flyback converter. The diode current appears at the end of the on time and jumps to a value depending on the turns ratio. These

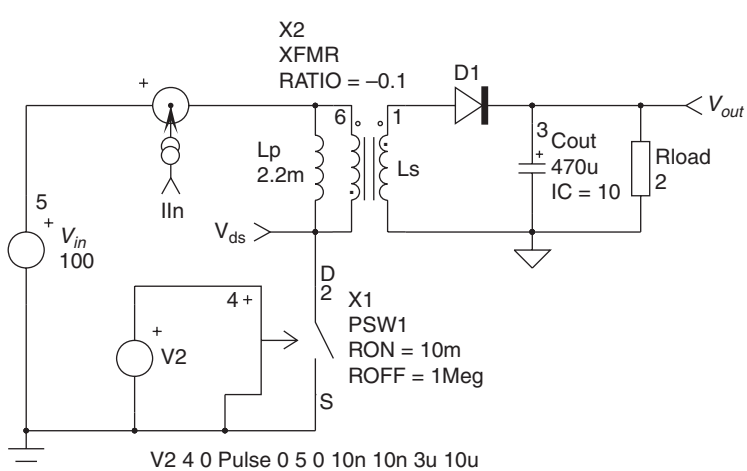

FIGURE 7-3a A simplified flyback converter operated in CCM.

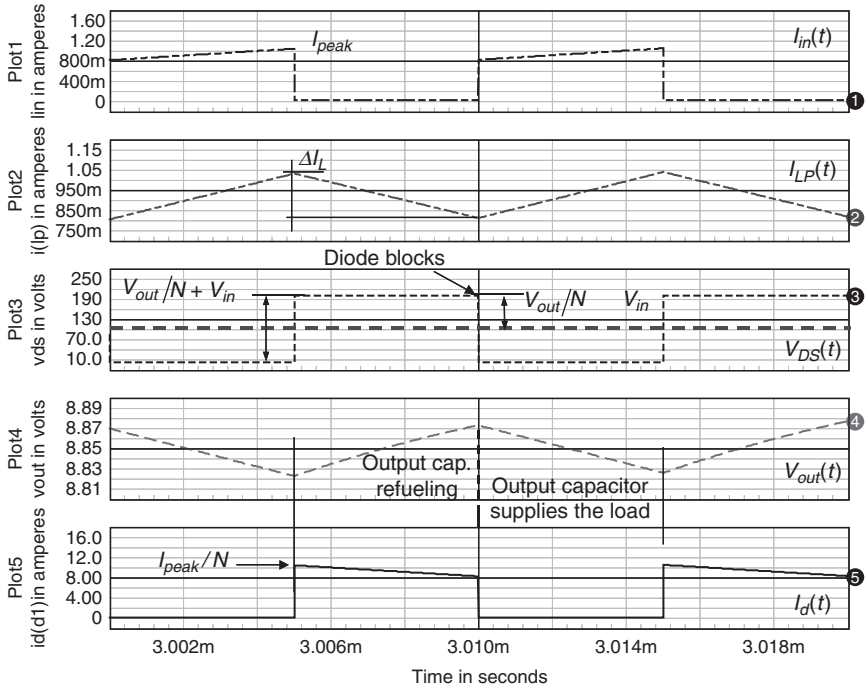

FIGURE 7-3b The simulation waveforms in CCM, no parasitic elements.

current discontinuities will naturally induce some output ripple on the capacitor, often further degraded by the presence of its ESR.

At the end of the off time, the upper switch terminal swings to a plateau level equal to that defined by Eq. (7-5b). Here, without a parasitic capacitor, the voltage transition is immediate. Given the 100 V input source, the switch jumps to around 200 V and stays there until the next on-time event. The rest of the waveforms are similar to those obtained with a buck-boost converter operated in CCM.

Calculating the average value of the input current will lead us to a very useful design equation, fortunately already derived in Chap. 5, in the buck-boost section, Eqs. (5-108) to (5-114). We can, however, derive a similar equation by observing the energy mechanisms. As the switch turns on, the inductor current is already at the valley point. The energy initially stored is thus

$$E_{L_p,valley} = \frac{1}{2} L_p I_{valley}^2 \tag{7-11}$$

At the end of the on time, the current has reached its peak value. The newly stored energy in the inductor then becomes

$$E_{L_p,peak} = \frac{1}{2} L_p I_{peak}^2 \tag{7-12}$$

Finally, the total energy accumulated by the inductor is found by subtracting these two equations:

$$E_{L_p,accu} = \frac{1}{2} L_p I_{peak}^2 - \frac{1}{2} L_p I_{valley}^2 = \frac{1}{2} L_p \left(I_{peak}^2 - I_{valley}^2 \right) \tag{7-13}$$

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Power (watts) is known to be energy (joules) averaged over a switching cycle. Given the converter efficiency η, the transmitted power is simply

$$P_{out} = \frac{1}{2}\left(I_{peak}{}^2 - I_{valley}{}^2\right)L_p F_{sw}\eta \tag{7-14}$$

If during operation the load is reduced, the converter enters DCM, allowing the valley current to reach zero. We have simulated this behavior, and the updated set of curves is seen in Fig. 7-3c. The peak drain voltage remains the same, but as the primary-inductance-stored energy drops to zero, the secondary diode suddenly blocks. At this point, the core is said to be reset, fully demagnetized. Without diode conduction, the primary reflected voltage disappears, and the drain goes back to the input voltage. A third state prolongs the off time, where no current circulates in the primary branch. This is the dead time portion, already discussed in the small-signal chapter. In this case, Eq. (7-14) can be updated by setting the valley current to zero:

$$P_{out} = \frac{1}{2} I_{peak}{}^2 L_p F_{sw}\eta \tag{7-15}$$

In both CCM and DCM plots, the second upper curve depicts the primary (or magnetizing) inductor current. This inductor stores energy during the on time and dumps its charge to the secondary side during the off time. On a real flyback circuit, it is impossible to observe this current as the magnetizing inductance cannot be accessed alone. You will thus use the input current to characterize the transformer rms and peak current stresses.

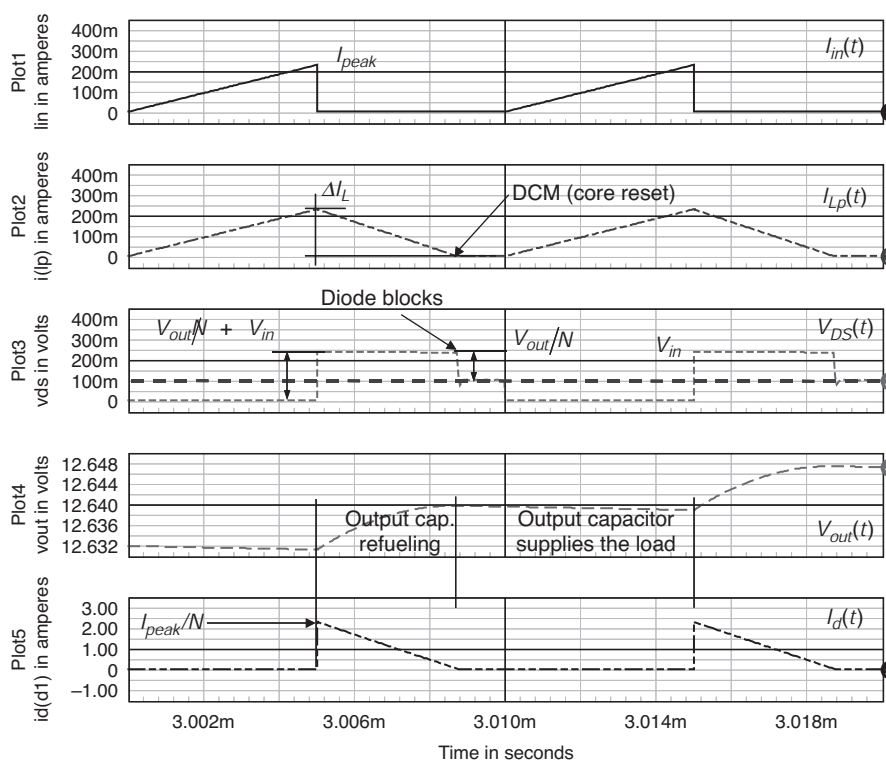

FIGURE 7-3c Simulation waveforms in DCM, no parasitic elements. As one can see on the output voltage, the converter is not fully stabilized at the time we captured the shot.

In the above examples, we ran the converters open loop, as exemplified by Fig. 7-3a. Despite similar duty cycles, the output level naturally varies as we operate in two different modes. Equation (7-10) defines the relationship between the output and the input voltage for the CCM mode. The link between V_{out} and V_{in} in DCM mode appears either in the buck-boost section [Eq. (1-143), just replace L by L_p and R_{load} by R_{load}/N^2] or in the DCM voltage-mode section, a few lines away.

7.3 FLYBACK WAVEFORMS WITH PARASITIC ELEMENTS

As perfection is not of this world, all our devices are affected by parasitic elements:

- The transformer features various capacitors, split between the windings and the primary inductance. We can lump all the capacitors in a single capacitor C_{lump} connected from the drain node (node 8) to ground.
- The coupling between the primary side and the secondary side is imperfect. Not all the stored energy in the primary flies to the secondary side. The symbol of such a loose coupling is the perfidious leakage inductance, a real plague of all flyback designs. In the example, we arbitrarily selected it to be 2% of the primary inductance, a rather poor transformer construction.
- The secondary diode also includes a certain amount of capacitance, especially if you use a Schottky. Otherwise, in CCM, the t_{rr} of a standard PN diode acts as a brief short-circuit seen from the primary side as a sharp current spike. The Schottky capacitance is reflected to the primary and included in C_{lump}.

Let us update Fig. 7-3a with the aforementioned parameters. Figure 7-4a shows the new converter. The simulation results are shown in Fig. 7-4b. We can see a lot of parasitic oscillations, playing

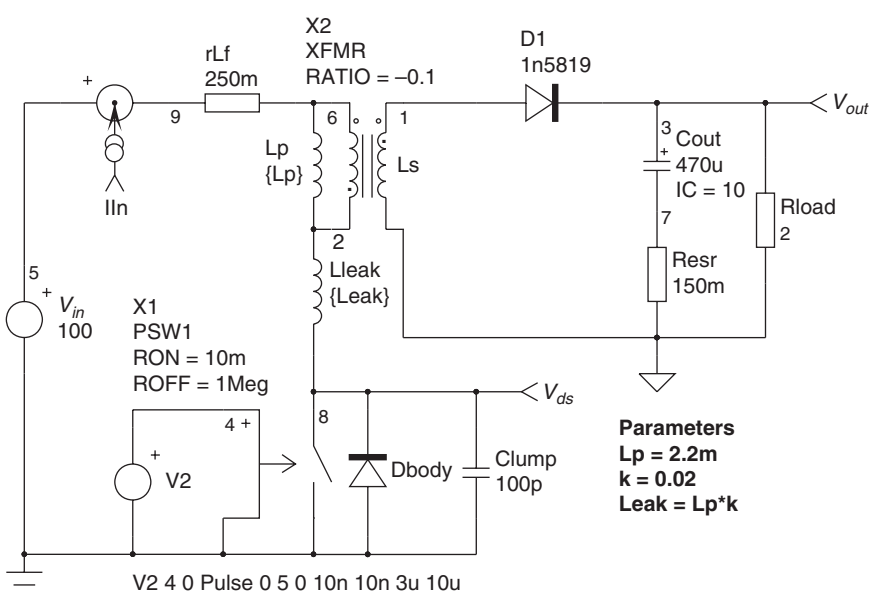

FIGURE 7-4a The updated flyback converter with a few parasitic elements.

SIMULATIONS AND PRACTICAL DESIGNS OF FLYBACK CONVERTERS

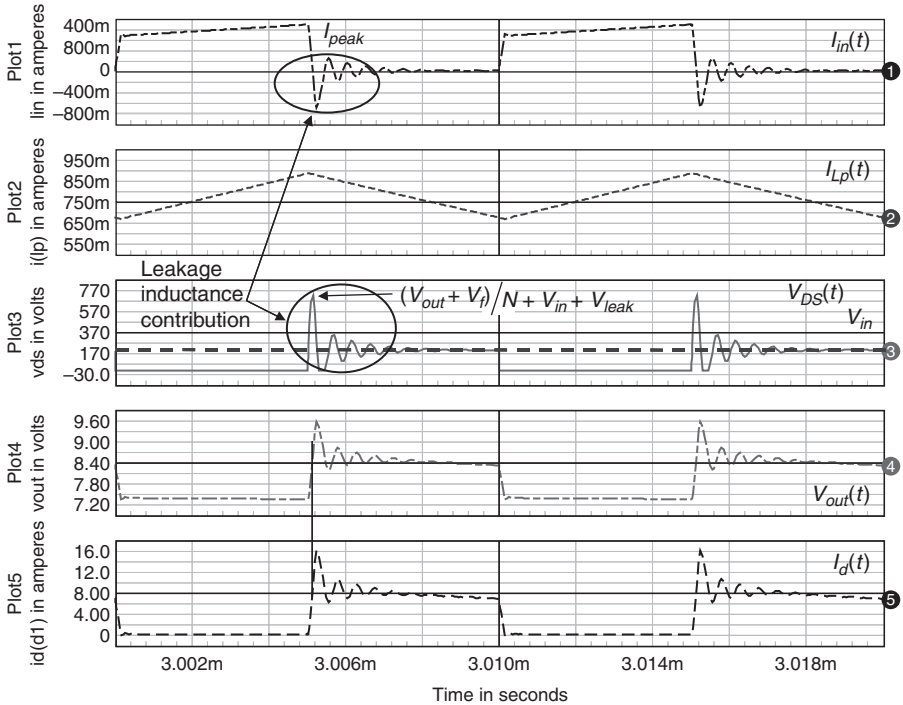

FIGURE 7-4b The updated flyback converter with a few parasitic elements, CCM operation.

an obvious role in the radiated EMI signature. Depending on their amplitude, these ringing waveforms often need to be attenuated by dampers. The output voltage now includes the capacitor ESR contribution, an effect of the current discontinuity at the switch opening. The reflected voltage includes the diode forward drop, as it sums up with the output voltage on the secondary side upper terminal. When the PWM controller biases the switch, the primary current also flows in the leakage inductance where energy is stored. When the PWM controller blocks the switch, this current needs to flow somewhere until this leakage inductance gets reset: it flows in the lump capacitor C_{lump} and makes the voltage very high. If no precautions are taken, the power switch (usually a MOSFET) can be destroyed by voltage breakdown. As we combine an inductor (the leakage term) and a capacitor, we obtain an oscillating *LC* network. This is the ringing you can see superimposed on all the internal signals. Very often, you need to clamp the voltage excursion, and also the oscillating wave amplitude, by an external damper. The leakage also delays the current flow into the output; this is seen as slowed-down edges on the diode current.

By increasing the load resistance and slightly shifting down the switching frequency, we can force a DCM operation. Figure 7-4c depicts the signals. They are very similar to those in the previous shot. As the peak current decreases, the voltage excursion on the switch is also reduced. Once the leakage ringing has gone, we enter the plateau region. During this time, as the core demagnetization has started, the primary inductance current drops. When it reaches zero, the secondary diode naturally blocks ($I_d = 0$). An oscillation takes place, involving the lump capacitor and the primary inductance L_p. The drain voltage freely rings from peaks to valleys, and when the switch closes again, the voltage brutally goes back to ground. If we wait to be in a valley before activating the switch, the converter is told to operate in "valley switching" mode. This is also called *borderline control*, which has several drawbacks such as frequency variations and noise inherent to valley jumping hesitations.

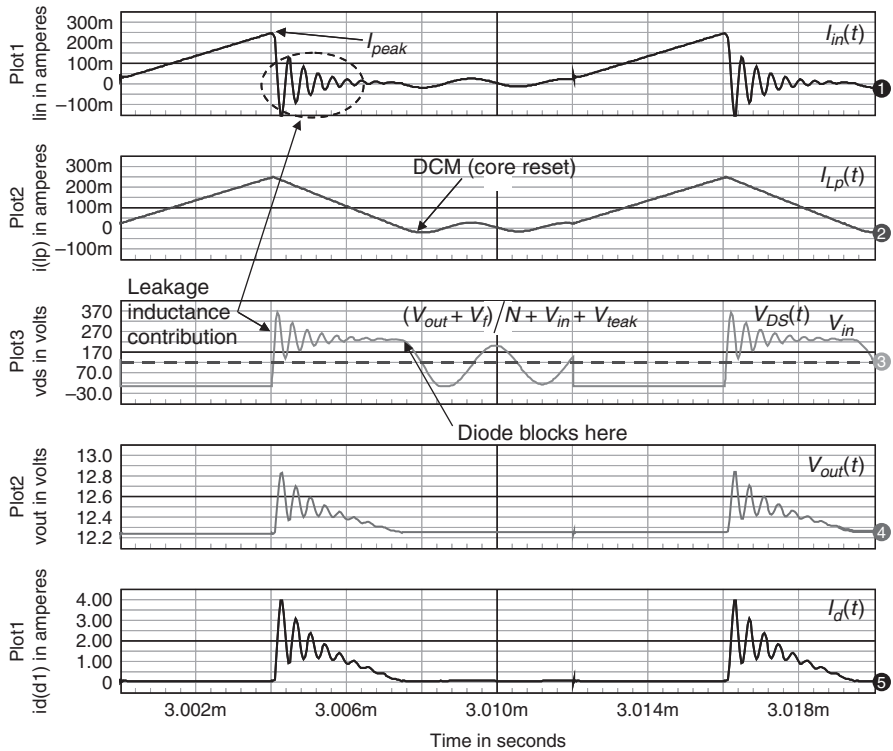

FIGURE 7-4c The updated flyback converter with a few parasitic elements, DCM operation.

7.4 OBSERVING THE DRAIN SIGNAL, NO CLAMPING ACTION

As shown in Fig. 7-5a, when a current flows in the primary inductance, it also circulates in the leakage inductance. During the on time, the current builds up in both terms until the PWM controller stops the switch: the primary current has reached its value I_{peak}. The secondary side circuit does not appear as the diode is blocked.

Immediately after the switch opening, Fig. 7-5b shows a simplified equivalent network. Both inductors are energized, and we assume here that the secondary diode has immediately started to conduct. The primary inductor is therefore replaced by a current source, in parallel with a voltage source whose value equals the reflected level from the secondary side. The leakage inductance is modeled by a source of I_{peak} value, routing its current through the lump capacitor. The capacitor upper terminal voltage quickly rises at a slope depending on I_{peak} and the capacitor value. On the rising edge of the signal, the slope is classically defined by

$$\frac{dV_{DS}(t)}{dt} = \frac{I_{peak}}{C_{lump}} \tag{7-16}$$

The maximum voltage at which the capacitor voltage will ring depends on the *LC* network characteristic impedance Z_0. This term is made of the leakage inductance and the lump capacitor. Measured from the ground node, the drain will thus undergo the capacitor voltage in series

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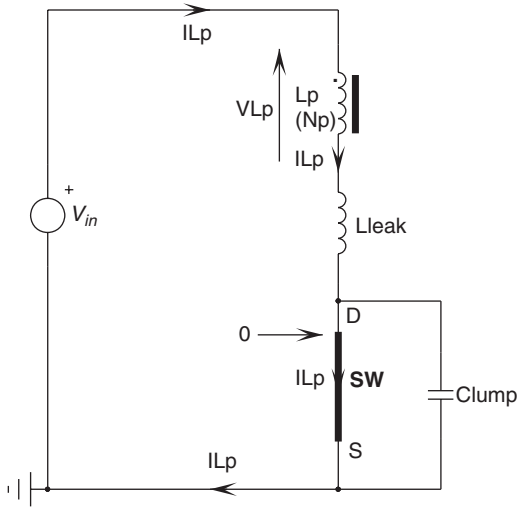

FIGURE 7-5a When the switch closes, the current flows through both the magnetizing inductor and its associated leakage term.

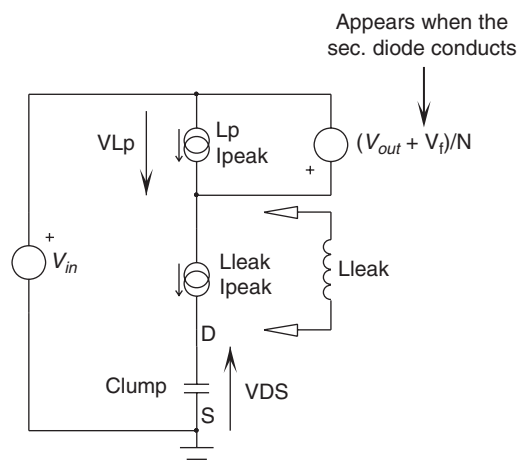

FIGURE 7–5b The leakage inductance charges the lump capacitor and makes the drain voltage abruptly go up.

with the sum of the reflected voltage (V_r, now considering the diode V_f) and the input source level V_{in}:

$$V_{DS,max} = V_{in} + V_r + I_{peak}Z_0 = V_{in} + \frac{V_{out} + V_f}{N} + I_{peak}\sqrt{\frac{L_{leak}}{C_{lump}}} \tag{7-17}$$

If no precaution is taken, risks exist to avalanche the power MOSFET by exceeding its BV_{DSS} and destroy it through an excess of dissipated heat. Artificially increasing the lump capacitor offers a simple way to limit the excursion at the switch opening and to protect the semiconductor (see the third design example). To illustrate this method, Fig. 7-5c depicts a flyback converter

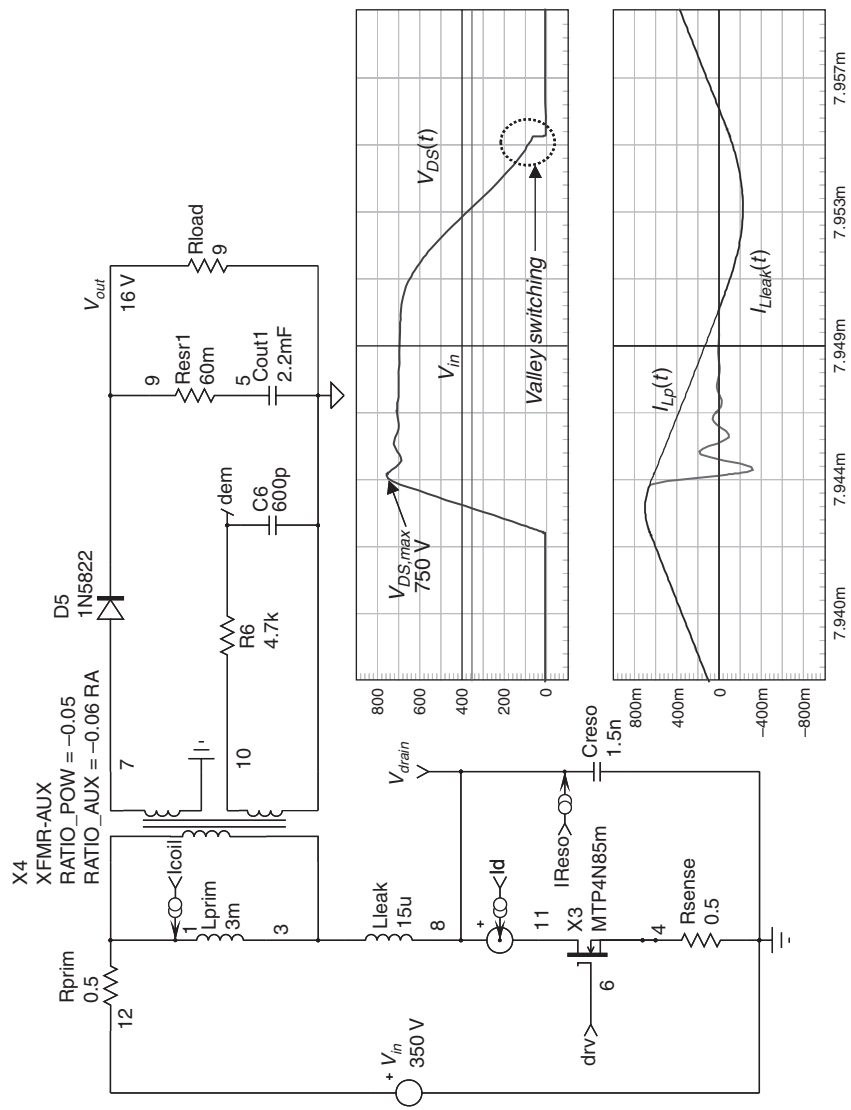

FIGURE 7-5c When a large capacitor connects to the drain node, it naturally limits the voltage excursion and softens the drain–source voltage.

operated in quasi-resonance (QR), also called borderline or valley switching operation. In this mode, the controller detects the valley in the drain voltage waveform and turns on the MOSFET, right in the minimum. Thus all capacitive losses are greatly diminished (if not removed) since a natural discharge of the lump capacitor occurs. Artificially increasing the capacitive term, here up to 1.5 nF, brings several advantages: (1) it slows down the rising voltage for a weakly radiating signal (a soft wave, low dV/dt) and (2) it limits the maximum excursion, allowing the use of an 800 V MOSFET at high line. As the graphs demonstrate, the drain voltage peaks to 751 V, as Eq. (7-17) predicted:

$$V_{DS,max} = 350 + \frac{16.6}{0.05} + 0.695\sqrt{\frac{15u}{1.5n}} = 751\,\text{V} \tag{7-18}$$

A 1.5 nF capacitor connected to the drain does not come for free since it must accommodate high-voltage pulses and accept a certain level of rms current. Furthermore, if valley switching is not properly ensured by the controller, unacceptable CV^2 losses will degrade the converter efficiency.

In low-power applications, some designers adopt this method to limit the voltage excursion and do not use a standard clamping network. The solution, in certain conditions, offers a cost advantage, but care must be taken to respect the MOSFET breakdown limit, especially in high-surge input conditions. Low-cost cell phone travel chargers that typically run less than $1 do not really care about it.

Another solution is to use a more traditional clamping network.

7.5 CLAMPING THE DRAIN EXCURSION

The clamping network safely limits the drain amplitude by using a low-impedance voltage source V_{clamp}, hooked via a fast diode to the high-voltage input voltage rail V_{in} (Fig. 7-6a). In practice, the low-impedance voltage source is made by an *RCD* clamping network or a *transient voltage suppressor* (TVS). For the sake of the current explanation, we will consider the V_{clamp} source as a simple voltage source.

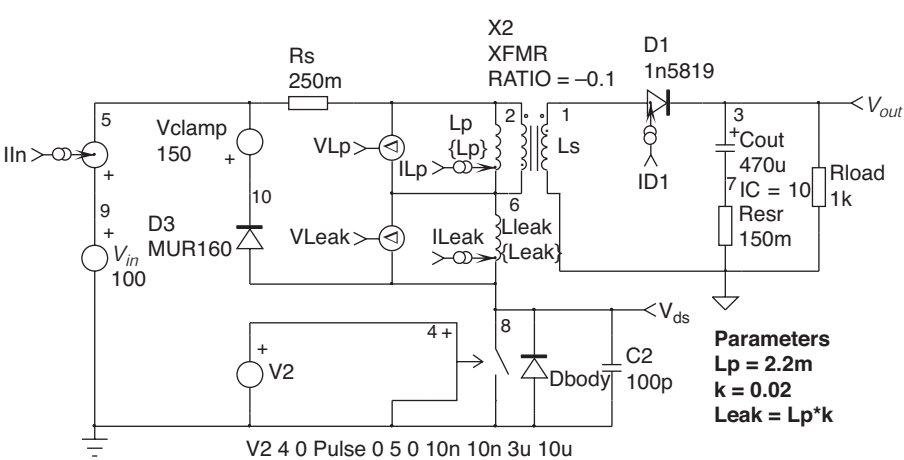

FIGURE 7-6a A clamping network (D_3, V_{clamp}) efficiently protects the power MOSFET against lethal voltage excursions.

When the switch opens, the voltage sharply rises, solely curbed by the drain lump capacitor. When the drain reaches a voltage equal to the sum of the input voltage and the clamping source, the series diode conducts and sharply cuts the drain-source excursion. Given a carefully selected clamping source level, the maximum excursion stays below the MOSFET breakdown voltage and ensures a reliable operation in worst-case conditions.

When the diode conducts, the equivalent schematic looks like that of Fig. 7-6b. Figure 7-6b is a more complex representation than Fig. 7-6a, as we consider the secondary diode not immediately conducting at the switch turn-off time. When the switch opens, all the magnetizing current also flows through the leakage inductance and equals I_{peak}. Both primary and leakage voltages reverse, in an attempt to keep the ampere-turns constant: the voltage across the drain starts to quickly rise, solely limited in growth speed by the lump capacitor [Eq. (7-16)]. On the secondary side, the voltage on the rectifying diode anode transitions from a negative voltage (the input voltage reversed and translated by the turns ratio N) to a positive voltage. When the drain exceeds the input voltage by the flyback voltage V_r, the secondary diode is forward biased. However, as drawn in Fig. 7-6b, the leakage current subtracts from the primary inductor current. The secondary side diode, despite its forward bias, cannot instantaneously attain a current equal to I_{peak}/N, since the initial primary current subtraction leads to zero ($I_{leak} = I_{peak}$). The current on this secondary side diode can only increase at a rate imposed by the leakage inductance and the voltage across it (Fig. 7-6c). Following its rise, the drain voltage quickly reaches a level theoretically equal to $V_{in} + V_{clamp}$ (neglecting the clamp diode forward drop and its associated overshoot): diode D_3 conducts and blocks any further excursion. The lump capacitor current goes to zero as its upper terminal voltage (the drain) is now fixed. The graph update appears in Fig. 7-6d. A reset voltage now applies across the leakage inductor terminals. Considering all voltages constant, we have

$$V_{reset} = V_{clamp} - \frac{V_{out} + V_f}{N} \tag{7-19}$$

The current flowing through the leakage inductor immediately starts to decay from its peak value at a rate given by

$$S_{L_{leak}} = \frac{V_{reset}}{L_{leak}} = \left[V_{clamp} - \frac{V_{out} + V_f}{N} \right] \frac{1}{L_{leak}} \tag{7-20}$$

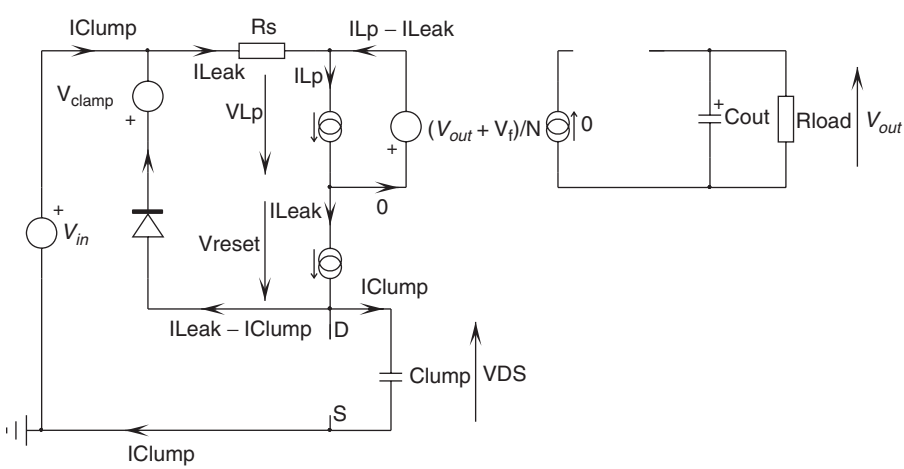

FIGURE 7-6b The leakage inductor diverts the current away from the primary inductor L_p.

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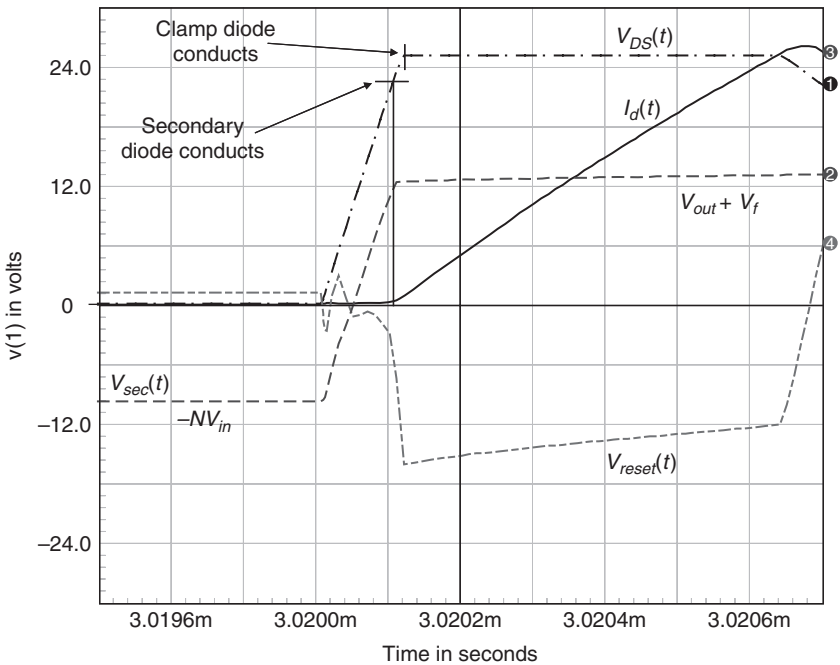

FIGURE 7-6c At the switch opening, the secondary voltage rises at a similar pace to that of the drain. The secondary diode is forward biased, and the secondary current starts to circulate.

The secondary current is no longer null and follows the equation

$$I_{sec}(t) = \frac{I_{L_p}(t) - I_{leak}(t)}{N} \tag{7-21}$$

When the leakage inductance current reaches zero, the clamp diode blocks: the secondary current is at its maximum, slightly below the theoretical value at the switching opening. Why?

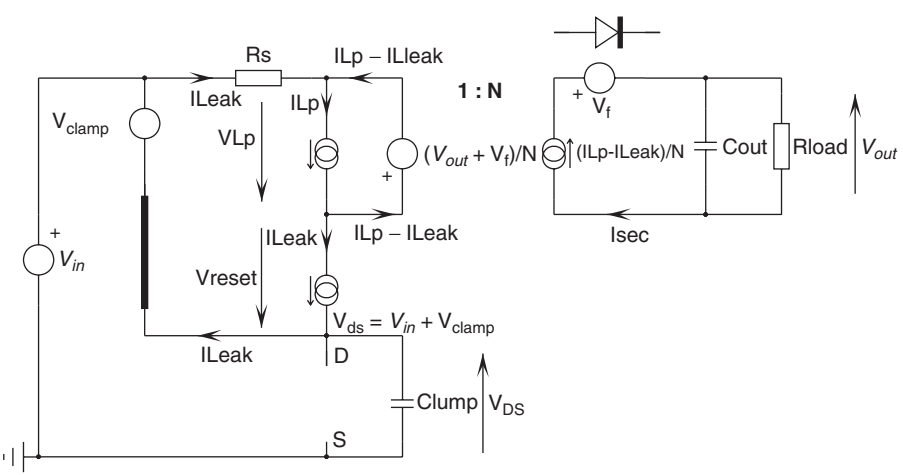

FIGURE 7-6d When the clamp diode conducts, a voltage is applied over the leakage inductor and resets it.

Because as long as the leakage inductor energy decays, it diverts current from the primary inductor. Figure 7-6e shows a representation of the currents in play, precisely at the switch turn-off.

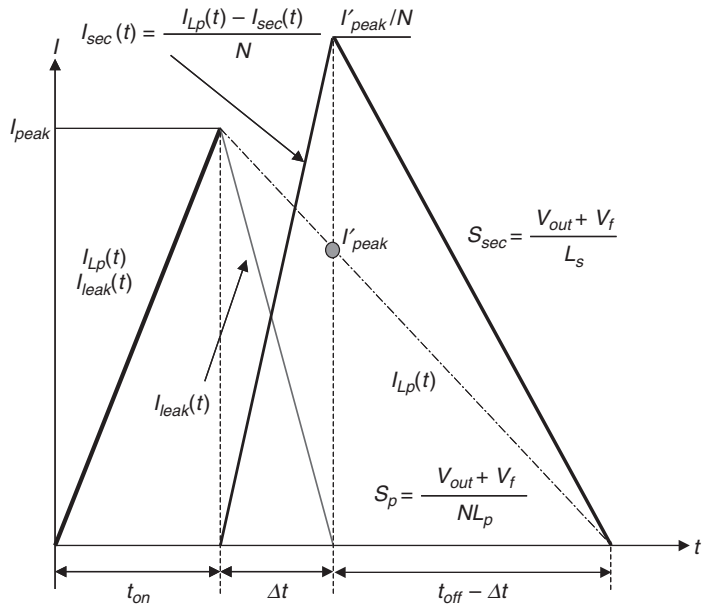

FIGURE 7-6e At turn-off, the leakage inductance delays the occurrence of the secondary side current.

In other words, the secondary diode current does not peak to I_{peak}/N, as it should with a zero leakage term, but to another value I'_{peak} reached when the leakage inductor is reset. This current value, on the primary side, can be calculated as follows, where S_p is the primary reset slope:

$$I'_{peak} = I_{peak} - S_p \Delta t = I_{peak} - \frac{V_{out} + V_f}{NL_p} \Delta t \tag{7-22}$$

Now Δt corresponds to the time needed by the leakage inductor current to fall from I_{peak} to zero. Thus, we have

$$\Delta t = \frac{I_{peak}}{S_{L_{leak}}} = I_{peak} \frac{L_{leak}}{V_{reset}} = \frac{NL_{leak} I_{peak}}{NV_{clamp} - (V_{out} + V_f)} \tag{7-23}$$

If we substitute Eq. (7-23) into (7-22), we obtain

$$I'_{peak} = I_{peak} - \frac{V_{out} + V_f}{NL_p} \frac{NL_{leak} I_{peak}}{NV_{clamp} - (V_{out} + V_f)} = I_{peak} \left[1 - \frac{L_{leak}}{L_p} \frac{1}{\frac{NV_{clamp}}{V_{out} + V_f} - 1} \right] \tag{7-24}$$

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A good design indication can be obtained from the ratio I'_{peak}/I_{peak}:

$$\frac{I'_{peak}}{I_{peak}} = \left[1 - \frac{L_{leak}}{L_p} \frac{1}{\dfrac{NV_{clamp}}{V_{out} + V_f} - 1} \right] \tag{7-25}$$

To obtain a ratio close to 1, the obvious way is to reduce the leakage inductance term in comparison with the primary inductor. We can also speed up the leakage reset by satisfying the following equation:

$$V_{clamp} > \frac{V_{out} + V_f}{N} \tag{7-26}$$

Thus, by allowing a higher drain-source voltage excursion, within safe limits of course, you will naturally (1) reset the leakage inductor more quickly and (2) reduce the stress on the clamping network, both results leading to an overall better efficiency.

Following Eq. (7-24), the peak current seen by the diode on the secondary side is simply

$$I_{sec} = \frac{I'_{peak}}{N} = \frac{I_{peak}}{N} \left[1 - \frac{L_{leak}}{L_p} \frac{1}{\dfrac{NV_{clamp}}{V_{out} + V_f} - 1} \right] \tag{7-27}$$

To test our analytical study, Fig. 7-6f portrays the simulated results of Fig. 7-6a. The peak current at the switch opening reaches 236 mA, and the secondary current at the end of the

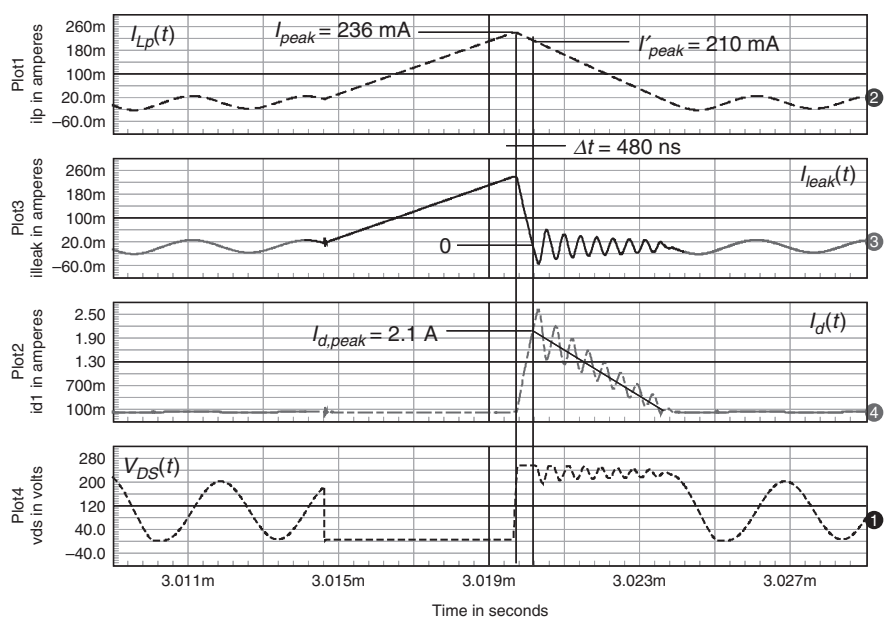

FIGURE 7-6f The simulation involving the leakage inductance confirms the delay brought by this term.

leakage reset time is approximately 2.1 A. Without the leakage term, the theoretical secondary current would have been 2.36 A. The reduction in current is thus around 11%, or 1.2% in power (I_{peak}^2), compensated by the feedback loop driving a slightly larger duty cycle. The converter efficiency obviously suffers from this situation.

Using Eq. (7-23), we can calculate the delay introduced by the leakage inductance, or its reset time:

$$\Delta t = \frac{NL_{leak}I_{peak}}{NV_{clamp} - (V_{out} + V_f)} = \frac{0.1 \times 44u \times 235m}{0.1 \times 150 - 13} = 520\,\text{ns} \tag{7-28}$$

At the leakage inductor reset point, the primary current has fallen to

$$I'_{peak} = I_{peak}\left[1 - \frac{L_{leak}}{L_p}\frac{1}{\dfrac{NV_{clamp}}{V_{out} + V_f} - 1}\right] = 0.235 \times \left[1 - \frac{44u}{2.2m}\frac{1}{\dfrac{15}{13} - 1}\right] = 204\,\text{mA} \tag{7-29}$$

The results delivered by the simulator are in good agreement with our calculations, despite slight discrepancies. They are mainly due to the clamp diode recovery time and the nonconstant reset voltage over the leakage inductor (reflected output ripple). If we reduce the clamping voltage to 140 V, the reset time increases to 800 ns, confirming the prediction of Eq. (7-26).

When the clamp diode blocks, the leakage inductor is completely reset. The new schematic becomes as shown in Fig. 7-7. At the diode turn-off point, the drain should normally drop to the reflected voltage plus the input voltage. However, the lump capacitor being charged to the clamp voltage, it cannot instantaneously go back to the plateau level. An oscillating energy

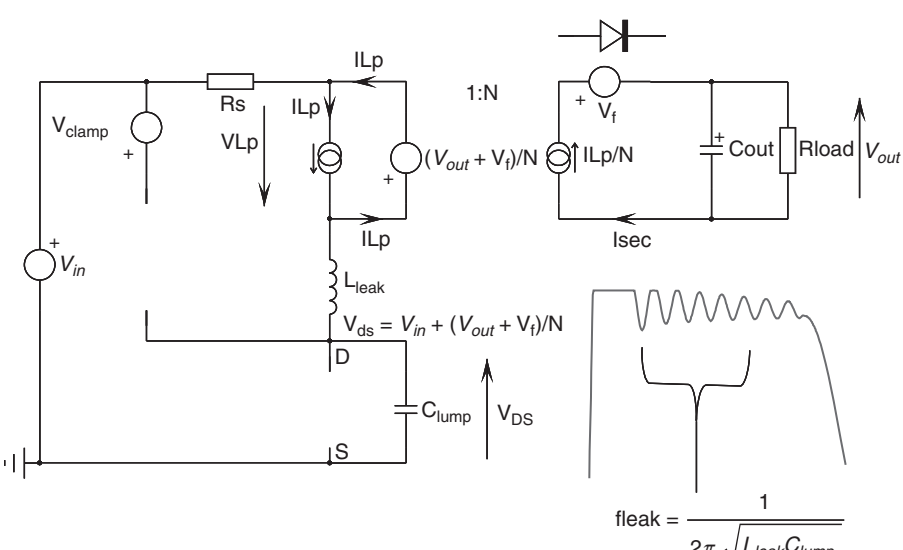

FIGURE 7-7 When the clamp diode blocks, a resonance occurs between the leakage inductor and the lump capacitor.

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exchange takes place between L_{leak} and C_{lump}, making the drain freely oscillating at a frequency imposed by the network:

$$f_{leak} = \frac{1}{2\pi\sqrt{L_{leak}C_{lump}}} \tag{7-30}$$

Given the values indicated in Fig. 7-6a, the network rings at 2.4 MHz. Thanks to the ohm losses in the oscillating path, we have an exponentially decaying waveform which can radiate EMI. By inserting a resistor in the clamping network, we have a chance to damp these oscillations, as we will see later. Sometimes, the ringing is so severe that it falls below ground and forward biases the MOSFET body diode, resulting in additional losses. An *RC* network must then be installed across the primary side to damp these oscillations.

7.6 DCM, LOOKING FOR VALLEYS

As long as the secondary diode conducts, a reflected voltage appears across the primary inductor and brings its current down. If a new switching cycle occurs, whereas current still flows in the secondary, the primary inductor enters CCM and the rectifying diode gets brutally blocked as the switch closes. Depending on the technology of this diode, the sudden blocking engenders losses such as those related to t_{rr}. If the diode is a PN junction type, it is seen as a short-circuit reflected to the primary, with a big spike on the current-sense element (hence the need for a leading edge blanking (LEB) circuitry — see Chap. 4 for this), until it recovers its blocking capabilities. If this is a Schottky, there is no recovery time but there is an equivalent nonlinear large capacitor across the diode terminals. This capacitor also brings primary losses but to a lesser extent. As an aside, you have read that a Schottky diode does not feature t_{rr} but sometimes data sheets still specify it for these diodes. How can it be? In this case, t_{rr} actually occurs because the so-called guard rings, placed to avoid arcing on the diode die corners, are activated when the Schottky forward drop reaches the guard-ring equivalent PN forward voltage. In that case, these rings get activated, and this is the t_{rr} you see on the scope. It usually occurs at a high forward current.

Now, if the flyback enters DCM, the secondary diode will naturally turn off, without significant losses. At that point, the reflected voltage on the primary side disappears. Figure 7-8 depicts the new circuit. The lump capacitor is left charged to the reflected voltage plus the input voltage. However, we again have a resonating network made up of the inductors $L = L_p + L_{leak}$ and the lump capacitor. A decaying oscillation thus takes place between C_{lump} and L and lasts until all the stored energy has been dissipated in the inductor and capacitor ohmic terms (the resistor R_s in the circuit). The waveform temporal evolution can be described by using Eq. (1-171a). In our case, the drain node "falls" from the lump capacitor voltage and converges toward the input voltage:

$$V_{DS}(t) \approx V_{in} + V_r \frac{e^{-\zeta\omega_0 t}}{\sqrt{1-\zeta^2}}\cos(\omega_0 t) \tag{7-31a}$$

where

$$\omega_0 = \frac{1}{\sqrt{(L_p + L_{leak})C_{lump}}} \tag{7-31b}$$

is the undamped natural oscillation and

$$\zeta = R_s\sqrt{\frac{C_{lump}}{4(L_p + L_{leak})}} \tag{7-31c}$$

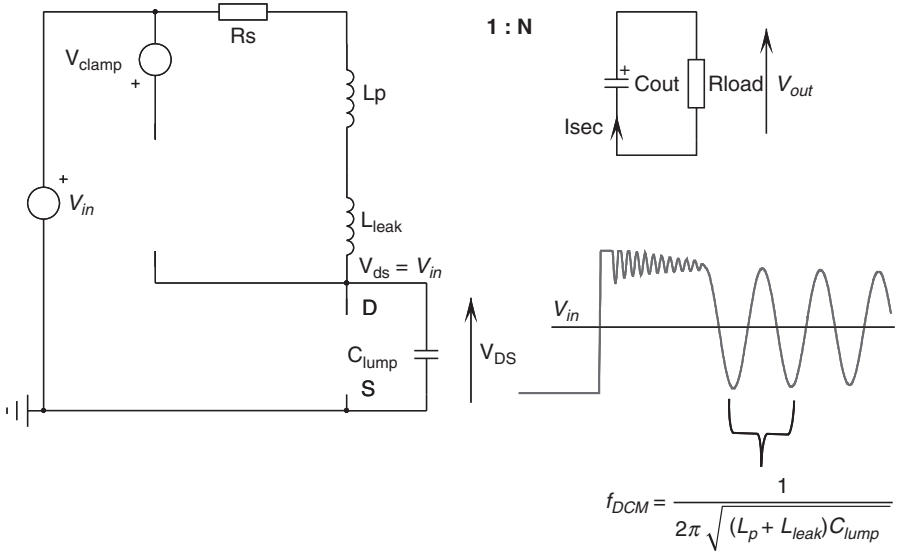

FIGURE 7-8 As DCM occurs, the drain rings to a frequency depending on the primary inductor in series with the leakage term and the lump capacitor.

represents the damping factor. V_r is the reflected voltage already seen and equals

$$V_r = \frac{V_{out} + V_f}{N} \tag{7-31d}$$

If we replace zeta in Eq. (7-31a) by its definition via Eq. (7-31c), then considering the damping factor small enough compared to 1 in the numerator, we can rewrite Eq. 7-31a in a more readable form:

$$V_{DS}(t) \approx V_{in} + V_r e^{-\frac{R_s}{2L}t} \cos(\omega_0 t) \tag{7-32}$$

with $L = L_p + L_{leak}$. The oscillating frequency comprises the leakage term plus the primary inductor as both devices now appear in series:

$$f_{DCM} = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{(L_p + L_{leak})C_{lump}}} \tag{7-33}$$

Figure 7-9 depicts the drain waveform in a more comprehensive form. We can see the leakage effect, with its associated ringing signal, followed by the plateau region, which is evidence for the secondary diode conduction. As the diode blocks, implying the core reset, an exponentially decaying oscillation takes place, alternating peaks and valleys. In quasi-resonance (QR) operation, the controller is able to detect the occurrence of these valleys. When in such valley, the drain level is minimum. If by design the reflected voltage equals the input voltage, then the waveform rings down to the ground. Assuming the PWM controller turns the MOSFET on right at this moment, *zero voltage switching* (ZVS) is ensured, removing all drain-related capacitive losses. This is what Fig. 7-5c already showed. The point at which the first valley occurs can be easily predicted by observing a −1 polarity of

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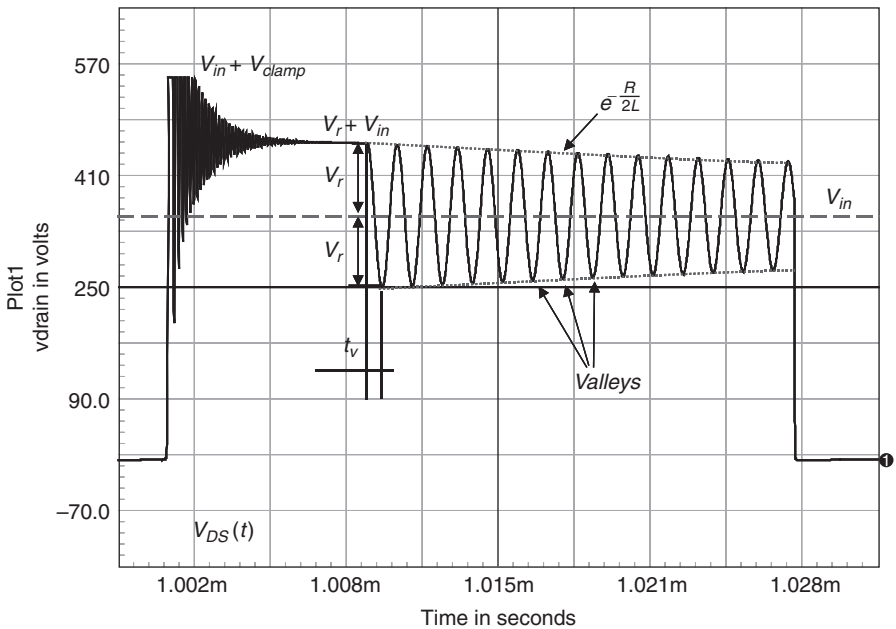

FIGURE 7-9 A drain-source waveform in DCM where the leakage ringing clearly shows up at the switch opening.

the cosine term in Eq. (7-32):

$$\cos(\omega_0 t_v) = \cos(2\pi f_0 t_v) = -1 \tag{7-34}$$

Solving this equation implies that $2\pi f_0 t_v = \pi$. Extracting t_v, gives

$$t_v = \frac{1}{2f_0} = \frac{2\pi\sqrt{(L_p + L_{leak})C_{lump}}}{2} = \pi\sqrt{(L_p + L_{leak})C_{lump}} \tag{7-35}$$

Thus, in a quasi-square wave resonant design, if a delay of t_v μs is inserted at the DCM detection point, the controller will turn the MOSFET on right in the minimum of its drain-source voltage.

By observing these parasitic ringings, it is possible to derive the transformer main element values. Appendix 7A shows how to do it.

7.7 DESIGNING THE CLAMPING NETWORK

The clamping network role is to prevent the drain signal from exceeding a certain level. This level has been selected at the beginning of the design stage, given the type of MOSFET you are going to use and the derating your quality department (or yourself!) imposes. Figure 7-10a depicts a waveform observed on the drain node of a MOSFET used in a flyback converter. The voltage sharply rises at the switch opening and follows a slope already defined by Eq. (7-16).

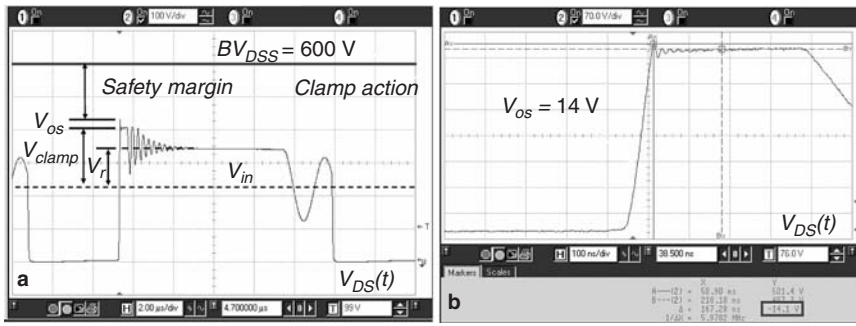

FIGURE 7-10 A typical DCM drain voltage showing the various voltage levels and the required safety margin.

In this particular example, the total drain node capacitor was measured at 130 pF, and the peak current at turn-off was 1.2 A. Equation (7-16) predicts a slope of

$$\frac{dV_{DS}(t)}{dt} = \frac{I_{peak}}{C_{lump}} = \frac{1.2}{130p} = 9.2 \text{ kV/}\mu\text{s} \tag{7-36}$$

This is exactly what is shown in Fig. 7-10b with a voltage swing of nearly 500 V in 50 ns. The clamp diode needs a certain amount of time before it actually conducts and blocks the drain excursion. It is interesting to note that the turn-on time of a PN diode can be extremely fast, whatever its type. A few nanoseconds is a typical number. What differs a lot between PN diodes is the blocking mechanism that can take several hundreds of nanoseconds (even microseconds for the 1N400X series) to let the crystal recover its electrical neutrality. (The recovery time is denoted by t_{rr}.) Here, zooming on the top of the waveform reveals an overshoot V_{os} of only 14 V, obtained with an MUR160. Later we will see different overshoots resulting from slower diodes such as the 1N4937 or even the 1N4007.

Accounting for this spike, we can now select the clamping voltage. Suppose we selected a MOSFET affected by a 600 V BV_{DSS} that is going to be used in a flyback converter supplied by a 375 Vdc (265 Vrms maximum) input source. Applying a derating factor k_D of 15% to the acceptable drain-source voltage (see App. 7B), we have the following set of equations, actually based on Fig. 7-10a indications.

- $BV_{DSS}k_D = 600 \times 0.85 = 510\,\text{V}$ — maximum allowable voltage in worst case
- $V_{os} = 20\,\text{V}$ — estimated overshoot attributed to the diode
- $V_{clamp} = BV_{DSS}k_D - V_{os} - V_{in} = 115\,\text{V}$ — selected clamping voltage (7-37a)

The 115 V clamping level is fixed and must be respected to keep the MOSFET operating in a safe area.

Now, let us define the transformer turns ratio. Equation (7-26) instructs to keep the clamping level well above the reflected voltage to authorize the quickest leakage term reset. In practice, satisfying this equation would imply high drain excursions (hence a more expensive 800 V component) or very low reflected voltages. Experience shows that a clamping voltage selected to be between 30 and 100% (the parameter k_c varying between 1.3 to 2) of the reflected voltage gives good results on efficiency figures. Let us assume we have a 12 V output adapter together with a rectifying diode featuring a V_f of 1 V and a clamp coefficient k_c of 2 (100%). To carry on with the design example, the transformer turns ratio N would simply be

$$V_{clamp} = k_c \frac{V_{out} + V_f}{N} \tag{7-37b}$$

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Solving for N yields

$$N = \frac{k_c(V_{out} + V_f)}{V_{clamp}} = \frac{2(12 + 1)}{115} = 0.226 \tag{7-38}$$

We now have an idea of the clamping voltage and the turns ratio affecting the transformer. Building of a low-impedance source connected to the bulk capacitor can be achieved via several possibilities, among which the *RCD* clamp represents the most popular solution.

7.7.1 The *RCD* Configuration

Figure 7-11 depicts the popular *RCD* clamping network. The idea behind such a network is to create a low-impedance voltage source of V_{clamp} value hooked to the bulk capacitor. This is a familiar structure, already depicted by Fig. 7-6a. The resistor R_{clp} dissipates power linked to the stored leakage energy, whereas the capacitor C_{clp} ensures a low ripple equivalent dc source. The clamping network dissipated power will increase as V_{clamp} approaches the reflected voltage. It is thus important to carefully select the clamping factor k_c, as you will see below.

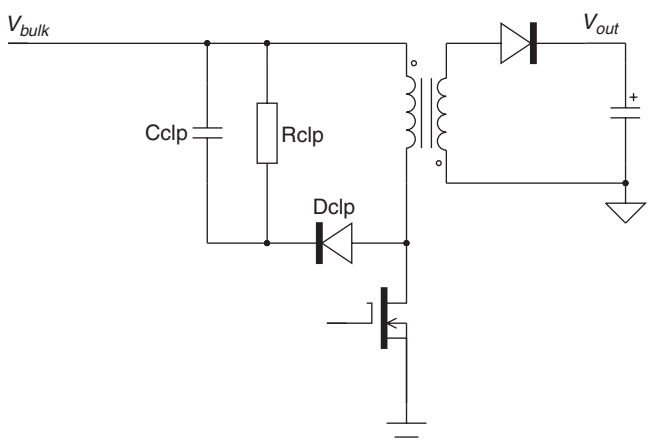

FIGURE 7-11 A typical clamping network made of a diode and two passive elements.

Looking back to Fig. 7-6d and 7-6e, we see the current circulating in the diode D_{clp} when it conducts (therefore when the drain voltage hits the clamp) can be expressed as

$$I_d(t) = I_{peak}\frac{\Delta t - t}{\Delta t} \tag{7-39}$$

This current circulates until the leakage inductance is fully reset. The time needed for the reset is denoted by Δt and was already described by Eq. (7-23). If we now consider the clamping voltage constant (actually our dc source V_{clamp} previously used) during Δt, the average power dissipated by the clamping source is

$$P_{V_{clamp},avg} = F_{sw}\int_0^{\Delta t} V_{clamp}I_d(t)\cdot dt = F_{sw}V_{clamp}\int_0^{\Delta t} I_{peak}\frac{\Delta t - t}{\Delta t}\cdot dt \tag{7-40}$$

Solving this integral gives us the power dissipated over a switching cycle

$$P_{V_{clamp},avg} = \frac{1}{2} F_{sw} V_{clamp} I_{peak} \Delta t \tag{7-41}$$

Now using Eq. (7-23) and substituting it into Eq. (7-41), we obtain a more general formula showing the impact of the reflecting voltage and the clamp level:

$$P_{V_{clamp},avg} = \frac{1}{2} F_{sw} L_{leak} {I_{peak}}^2 \frac{V_{clamp}}{V_{clamp} - \dfrac{V_{out} + V_f}{N}} = \frac{1}{2} F_{sw} L_{leak} {I_{peak}}^2 \frac{k_c}{k_c - 1} \tag{7-42}$$

Our dc source is made of a resistor and a capacitor in parallel. As all the average power is dissipated in heat by the resistor, we have the following equality:

$$\frac{{V_{clamp}}^2}{R_{clp}} = \frac{1}{2} F_{sw} L_{leak} {I_{peak}}^2 \frac{V_{clamp}}{V_{clamp} - \dfrac{V_{out} + V_f}{N}} \tag{7-43}$$

Extracting the clamp resistor from the above line leads us to the final result:

$$R_{clp} = \frac{2 V_{clamp} \left[V_{clamp} - \dfrac{V_{out} + V_f}{N} \right]}{F_{sw} L_{leak} {I_{peak}}^2} \tag{7-44}$$

The capacitor ensures a low-ripple ΔV across the *RCD* network. Figure 7-12 depicts the capacitor waveforms, its current, and voltage. If we assume all the peak current flows in the capacitor

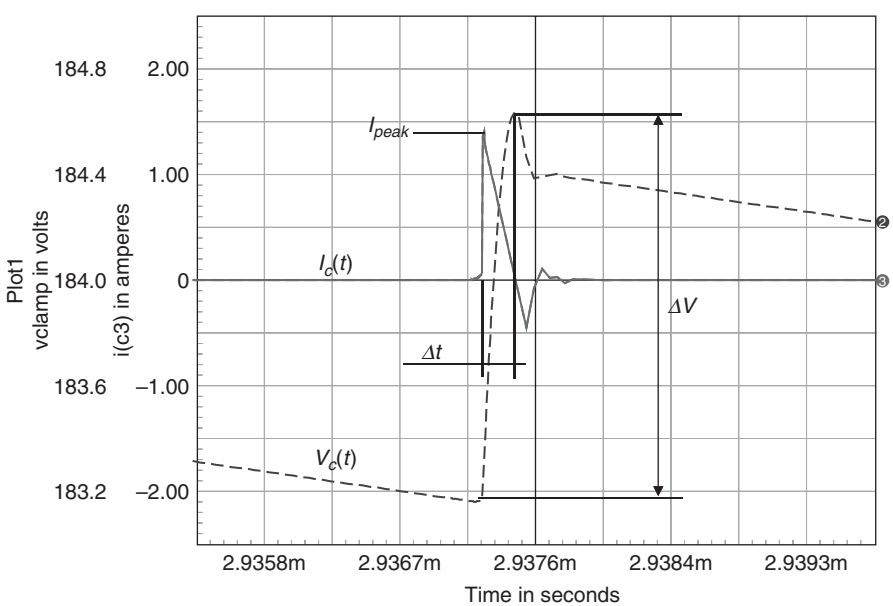

FIGURE 7-12 The clamp capacitor voltage and current waveforms.

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during the reset time, the voltage developed across its terminal is obtained by first deriving a charge equation

$$Q_{C_{clp}} = I_{peak}\frac{\Delta t}{2} \tag{7-45}$$

Then the voltage ripple seen by the clamping network is simply

$$I_{peak}\frac{\Delta t}{2} = C_{clp}\,\Delta V \tag{7-46}$$

Solving for C_{clp} and replacing Δt by its definition [Eq. (7-23)], we obtain an equation for the clamp capacitor:

$$C_{clp} = \frac{I_{peak}^2 L_{leak}}{2\Delta V(V_{clamp} - V_r)} \tag{7-47}$$

If now extract L_{leak} from Eq. (7-44) and replace it in Eq. (7-47), we reach a simpler expression:

$$C_{clp} = \frac{V_{clamp}}{R_{clp}F_{sw}\,\Delta V} \tag{7-48}$$

Since this capacitor will handle current pulses, it is necessary to evaluate its rms content to help select the right component. The rms current can be evaluated by solving the following integral:

$$I_{clp,rms} = \sqrt{\frac{1}{T_{sw}}\int_0^{\Delta t}\left[I_{peak}\frac{\Delta t - t}{\Delta t}\right]^2 dt} = I_{peak}\sqrt{\frac{\Delta t}{3T_{sw}}} \tag{7-49}$$

Based on the above example, we have the following design elements:

$I_{peak,max} = 2.5$ A—maximum current the controller allows in fault or overload situations
$F_{sw} = 65$ kHz
$L_{leak} = 12$ µH
$V_{clamp} = 115$ V

From Eq. (7-44), we calculate the clamp resistor value

$$R_{clp} = \frac{2 \times 115\left[115 - \dfrac{12 + 1}{0.226}\right]}{65k \times 12u \times 6.25} = 2.7\,\text{k}\Omega \tag{7-50}$$

The power dissipated by the resistor reaches 4.9 W at full power, as delivered by the left term in Eq. (7-43). If we select a voltage ripple of roughly 20% of the clamp voltage, Eq. (7-48) leads to a capacitor value of

$$C_{clp} = \frac{V_{clamp}}{R_{clp}F_{sw}\Delta V} = \frac{115}{2.7k \times 65k \times 0.2 \times 115} = 28\,\text{nF} \tag{7-51}$$

According to Eq. (7-49), the rms current reaches 266 mA.

7.7.2 Selecting k_c

Equation (7-42) lets us open the discussion regarding k_c. Its selection depends on design choices. The author recommends to keep it in the vicinity of 1.3 to 1.5 times the reflected voltage, in order to give greater margin on the turns ratio calculation. As indicated by Eq. (7-3), lower N ratios let the designer pick up lower V_{RRM} secondary diodes. Schottky diodes are common in either 100 V or 200 V V_{RRM} values, but 150 or 250 V is starting to appear also. Adopting diodes featuring high-reverse-voltage capabilities affects the efficiency: the V_f usually increases (sensitive to the average current) as well as the dynamic resistance R_d (sensitive to the rms current).

On the other hand, the choice of k_c depends on the amount of leakage inductance brought by the transformer. Poorly designed flyback transformers exhibit leakage terms in the vicinity of 2 to 3% of the primary inductance. Excellent designs bring less than 1%. The greater the leakage inductance, the larger the difference between the clamp level and the reflected voltage, implying k_c coefficients close to twice the reflected voltage or above. If you keep k_c low (1.3 to 1.5) in spite of a large leakage term, you will pay for it through a higher power dissipation on the clamping network. In case the transformer still suffers from high leakage despite several redesigns, bring k_c to 2 and select higher V_{RRM} secondary diodes. This is what was done in the design example given the leakage term value (1.5% of L_p).

Based on the example, we have plotted the clamp resistor dissipated power versus the clamp coefficient k_c. As the clamp level approaches the reflected voltage, we can see a dramatic increase in the clamp dissipated power (Fig. 7-13).

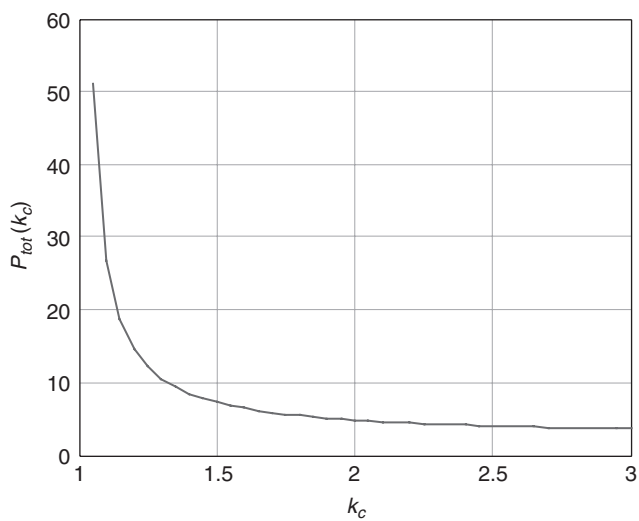

FIGURE 7-13 The dissipated power in the clamp resistor dramatically increases as the reflected voltage approaches the clamp voltage.

This plot stresses the need to push for a low leakage inductance, especially at high power levels. In the example, the 12 μH leakage term corresponds to 1.5% of the primary inductance. Several calculations were performed while assuming various transformer coupling qualities and trying to arbitrarily keep the average power on the clamp below 4 W. (The MOSFET breakdown voltage is fixed to 600 V.) Results are presented in the table below and show how other parameters are affected.

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L_{leak} (% of L_p)	0.5	0.8	1	2
k_c	1.3	1.5	1.7	2
N	0.15	0.17	0.19	0.23
PIV (V)	67	76	84	97
V_{RRM} (V)	150	150	200	200
P_{clamp} (W)	3.4	3.8	3.8	6

In summary, if the leakage term is low, you can accept lower k_c factors (1.3) and thus reduce the voltage stress on the secondary diode, as explained. When the leakage inductance increases, keeping a reasonable dissipated power on the clamp implies an increase of N and the selection of higher voltage diodes with the associated penalties.

7.7.3 Curing the Leakage Ringing

Figure 7-10 showed some ringing appearing when the diode abruptly blocks. These oscillations find their roots in the presence of stray elements such as the leakage inductance, the lump capacitor, and all associated parasitic elements. Damping the network consists of artificially increasing the ohmic losses in the oscillating path. The damping resistor value can be found through a few simple equations pertinent to *RLC* circuits. The quality coefficient of a series *RLC* network is defined by

$$Q = \frac{\omega_0 L_{leak}}{R_{damp}} \tag{7-52}$$

To damp the oscillations, a coefficient of 1 can be the goal, implying that the damping resistor equals the leakage inductor impedance at the resonant frequency:

$$\omega_0 L_{leak} = R_{damp} \tag{7-53}$$

In our case, on the power supply prototype, we measured a ringing frequency f_{leak} of 3.92 MHz together with a leakage inductance of 12 μH. Thus, the damping resistor value must be

$$R_{damp} = 12u \times 6.28 \times 3.92\text{Meg} = 295\,\Omega \tag{7-54}$$

A first possibility exists to dampen the *RCD* clamp itself as shown on Figure 7-14. This solution offers a simple nonpermanent dissipative way to help reducing the oscillations at the diode opening: once the diode D_{clp} is blocked (at the leakage inductor reset), this resistor no longer undergoes a current circulation. Unfortunately, the addition of this resistor affects the voltage peak associated with the current value at turn-off. This voltage increase ΔV simply equals

$$\Delta V = I_{peak} R_{damp} \tag{7-55}$$

Given the above result, care must be taken to not degrade the original diode overshoot ΔV by the insertion of the damping resistor. Start on the prototype with values around 10 ohms and increase the resistor to find a point where the overshoot and the ringing are acceptable. After several tweaks, a 47 Ω resistor brought the needed improvement. Figures 7-15a and b shows the result after the installation of the damping resistor. We can see in Fig. 7-15b that the ringing amplitude has been slightly reduced while the overshoot remains acceptable. Please note that R_{damp} acts on the oscillating network $L_{leak}C_{lump}$ through the diode recovery capacitance C_{rr}.

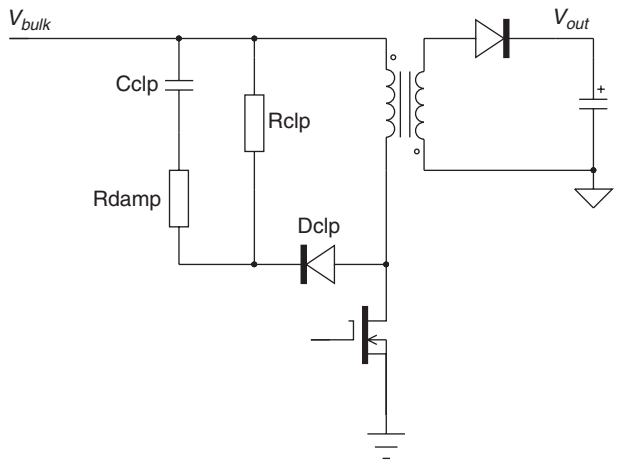

FIGURE 7-14 A resistor in series with the clamping capacitor helps to damp the parasitic oscillations.

Given its small value, the damping is less efficient than the solution described below. However, thanks to its effect on the overshoot itself, industrial applications, such as notebook adapters, make an extensive use of this technique which improves the radiated EMI signature.

Another possibility consists of damping the transformer primary side alone. It no longer touches the clamping network, but as it directly connects to the drain, it can impact the efficiency. Figure 7-16 represents this different option. The design procedure remains similar, and Eq. (7-53) still applies. The differences lies in the series capacitor, placed here to avoid a big resistive power dissipation as the switch closes. Reference 1 recommends a capacitor impedance equal to the resistor value at the resonant frequency of concern:

$$C_{damp} = \frac{1}{2\pi f_{leak} R_{damp}} \tag{7-56}$$

Again, you might want to adjust this value a little to avoid overdissipation on the damping network. Figure 7-17a gathers some waveforms obtained on a flyback featuring a 22 μH leakage

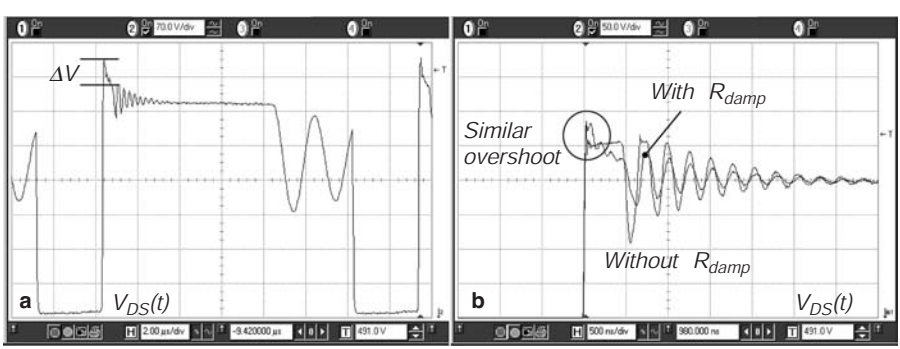

FIGURE 7-15 Installing the adequate damping resistor keeps the overshoot almost constant but reduces the ringing amplitude.

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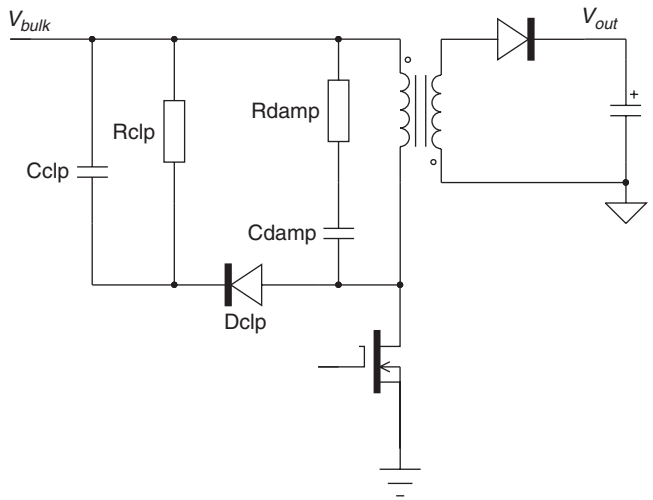

FIGURE 7-16 The *RC* damper connects on the transformer primary rather than on the clamping network.

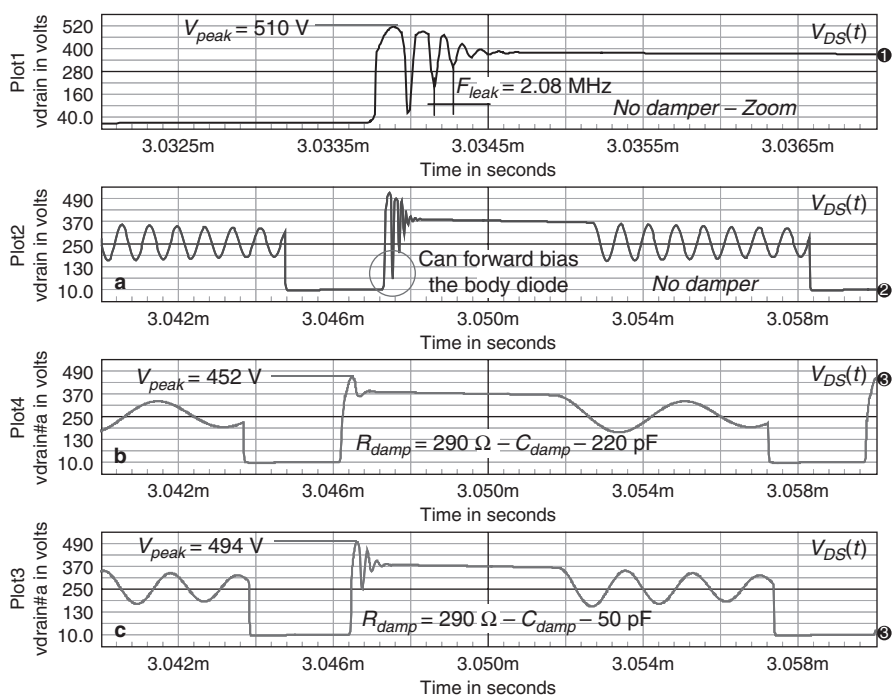

FIGURE 7-17a Damping the primary side also brings nice-looking waveforms!

inductor. The upper curves (a) describe the waveforms obtained without damping at all. The ringing becomes so severe that the body diode of the MOSFET can be forward biased, engendering further losses. If a discrete MOSFET can easily handle that, we do not recommend this forward biasing on a monolithic switcher where substrate injection could occur and damage the part through erratic behavior. A damper is mandatory in this case. Curve b in Fig. 7-17a depicts the fully damped waveform obtained from a resistor of 295 Ω and a capacitor of 220 pF, respectively, recommended by Eqs. (7-54) and (7-56). Despite the nice overall shape, where all the ringing has gone, the total loss budget has increased by 1.25 W. To reduce the heat, we decreased the damping capacitor down to 50 pF, and curve (c) appeared, still showing some ringing, but less severe than in the original waveform. The efficiency was almost left unaffected by this change.

The power dissipated by the resistor depends on the voltage stored by the damping capacitor during the switching events. During the on time, the capacitor charges to the input voltage V_{in}. During the off time, the capacitor jumps to the flyback voltage and stays there until the primary inductance resets (in DCM). Figure 7-17b depicts these events and shows the energy in play. If we suppose the capacitor is discharged to 0 at the beginning of the on time, then the needed energy to bring it up to the input voltage is (event 1)

$$E_{on} = \frac{1}{2} C_{damp} V_{in}^2 \tag{7-57a}$$

Then, to charge the damping capacitor to the reflected voltage at the switch opening, you need to first bring the same energetic level as described by Eq. (7-57a) (discharge the capacitor down to zero, event 2) to which you add another jump equal to (event 3)

$$E_{off} = \frac{1}{2} C_{damp} \left[\frac{V_{out} + V_f}{N} \right]^2 \tag{7-57b}$$

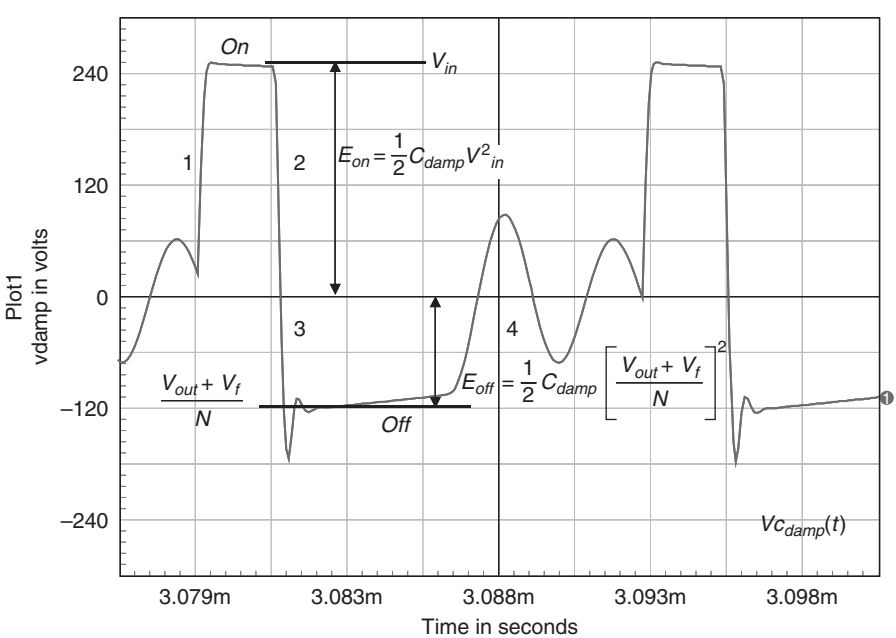

FIGURE 7-17b The damping capacitor voltage during the switching events.

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Then, in DCM, the capacitor voltage rings and goes back to zero, releasing the energy also described by Eq. (7-57b) (event 4). As the capacitive current flows through the damping resistor, the total dissipation seen by this element is simply

$$P_{R_{damp}} = 2\left(\frac{1}{2}C_{damp}V_{in}^2 + \frac{1}{2}C_{damp}\left[\frac{V_{out}+V_f}{N}\right]^2\right)F_{sw} = C_{damp}\left[V_{in}^2 + \left(\frac{V_{out}+V_f}{N}\right)^2\right]F_{sw} \quad (7\text{-}57c)$$

In the above example, the input voltage was 250 V, the reflected voltage was 120 V, and there was a 71 kHz switching frequency. This leads to a theoretical dissipated power of

$$P_{R_{damp}} = C_{damp}\left[V_{in}^2 + \left(\frac{V_{out}+V_f}{N}\right)^2\right]F_{sw} = 220p \times [250^2 + 120^2] \times 71k = 1.2\ \text{W} \quad (7\text{-}57d)$$

Simulation gave 1.15 W. This damping technique, compared to the previous one, does hamper the light/no-load efficiency and might not represent a good option for power-sensitive projects.

When you install dampers as in the above example, a simple diagram such as Fig. 7-17b helps to figure out the power dissipated in the damping resistor.

7.7.4 Which Diode to Select?

The above example showed curves obtained with an ultrafast diode, the MUR160. (A UF4006 would have given similar results.) This diode being rather abrupt when it turns off, the equivalent $L_{leak}C_{lump}$ network rings a lot and requires a damping action as we just described. Some slower diodes can also be used, such as the 1N4937 or even the 1N4007. Yes, you have read it correctly, the 1N4007! This diode actually presents a rather lossy blocking mechanism which heavily damps the leakage ringing and just makes it disappear. As Fig. 7-18 shows, it

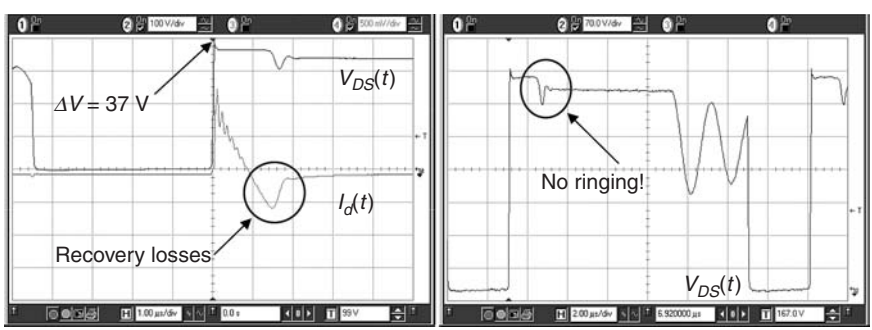

FIGURE 7-18 The 1N4007 offers adequate performance in low-power applications, below 20 W. Note the lack of ringing given the lossy mechanism.

gives excellent results, especially in radiated EMI. The 4007 has the reputation of being a slow diode, which is true when it starts to block. However, you can see the small overshoot of 37 V only, given the slope of 9.2 V/ns. As the diode recovers, it remains a short-circuit until it has fully swept away the minority carriers: this occurs at the negative peak. At this point, the diode recovers its blocking capability, and the current goes down slowly, naturally damping the leakage network. I have seen 1N4007 diodes used in high-power designs, well above 20 W (!), something I would absolutely not recommend.

There are other solutions known to help damp parasitic waveforms. They include lossy ferrite beads, widely used in the industry.

7.7.5 Beware of Voltage Variations

The *RCD* clamp network is unfortunately subject to voltage variations as the peak current changes. As a result, it is important to check that worst-case conditions do not jeopardize the MOSFET. Worst-case conditions are as follows:

1. *Start-up sequence, highest input level, full load*: Monitor $V_{DS}(t)$ by either directly observing the waveform or synchronizing the oscilloscope on the V_{cc} pin. The crucial point lies precisely when the feedback starts to take control. This is where the output voltage is at its peak and the primary peak current has not yet been reduced by the feedback loop.
2. *Highest input voltage, short-circuit*: Place a short-circuit on the secondary side (a real small piece of metal and not a long wire or the electronic load) and start the power supply. If the protection operates well, the converter should enter hiccup mode, trying to start up. As the auxiliary voltage does not show up (because of the output short-circuit), the controller quickly detects an *undervoltage lockout* (UVLO) and stops driving pulses. However, in the short period during which it drives the MOSFET, the peak current set point is pushed to its maximum limit and induces a large leakage kickback voltage. Make sure $V_{DS}(t)$ stays under control.

Figure 7-19 is a plot of the clamp voltage variations as the peak current changes. The design variable for Eq. (7-44) shall be the maximum peak current that the primary inductance can see. This is the maximum sensed voltage the controller can authorize over a given resistor, affected

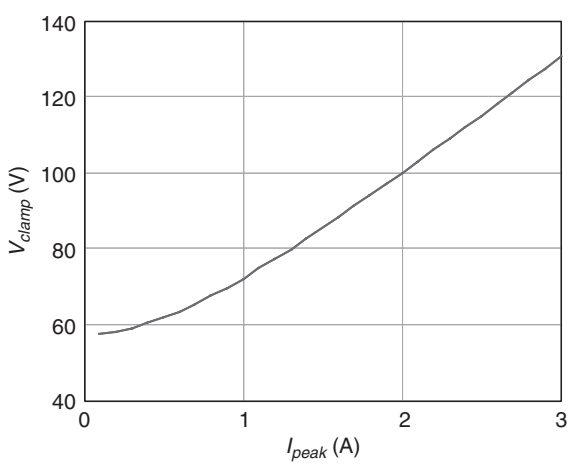

FIGURE 7-19 Clamp voltage changes due to primary peak current variations.

by the propagation delay t_{prop}. This propagation delay actually corrupts the current level imposed by the controller in short-circuit or in start-up conditions. Why? Because in either case, the feedback is lost and the peak current limit solely relies on the internal maximum set point. On a UC384X member, the maximum set point is 1.1 V. That is, when the current-sense

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comparator detects a voltage of 1.1 V, it immediately instructs the latch to reset and shuts the driver off. Unfortunately, it takes time for the turn-off order to propagate to the drive output and block the MOSFET. The propagation delay therefore includes the controller itself (internal logic delays) but also the driving chain to the MOSFET gate. Until it actually occurs, the primary current keeps growing and it overshoots. The overshoot depends on the primary slope and the propagation delay. Figure 7-20 illustrates this phenomenon.

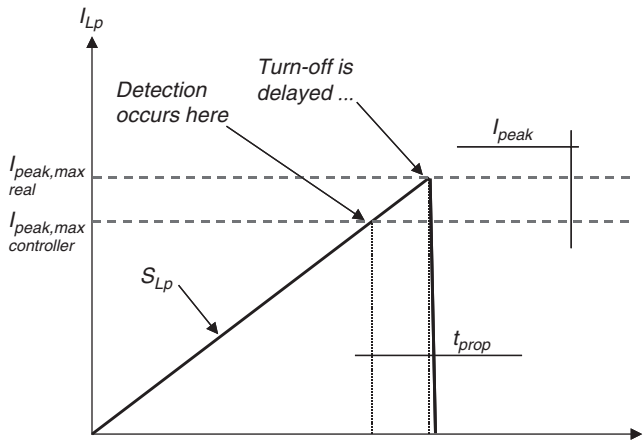

FIGURE 7-20 Propagation delay effects create primary current overshoot.

Suppose we have a primary inductance L_p of 250 μH and a maximum peak current set point of 1.1 V. The sense resistor equals 0.44 Ω, and the total propagation delay t_{prop} reaches 190 ns. Of course, if you insert a resistor in series with the drive, in an attempt to alter the EMI signature, you naturally introduce further delays which degrade the controller reaction time. The final peak current is obtained at the highest input voltage, 375 Vdc in this example:

$$I_{peak,max} = \frac{V_{sense,max}}{R_{sense}} + \frac{V_{in,max}}{L_p} t_{prop} = \frac{1.1}{0.44} + \frac{375}{250u} 190n = 2.8\,\text{A} \qquad (7\text{-}58)$$

In this example, the overshoot reaches almost 200 mA at high line. Suppose you have selected the clamp resistor based on 1.1 V developed over the 0.44 Ω sense element (2.5 A) to reach a clamp level of 115 V. You end up with a 124 V clamping level (8% more). But the worst is yet to come.

The worst situation arises when you have a really low primary inductance and a minimum t_{on} clamped down to 350 ns, for instance. The minimum t_{on} is made of the leading edge blanking (LEB) duration (if the controller features such circuitry, of course) added to the total propagation delay. If the controller features a 250 ns LEB with a 120 ns propagation delay, it will be impossible to reduce the on time below 370 ns. Why? Simply because at the beginning of each driving pulse, the controller is blind for 250 ns (to avoid a false tripping due to spurious pulses—diodes t_{rr} for instance) and takes another 120 ns to finally interrupt the current flow. During this time, the gate is held high and the MOSFET conducts. In short-circuit situations, not only does the primary current overshoot as explained above, but also it does not decrease during the off time: the converter enters a deep CCM mode because of the lack of reflected

voltage. Actually, there is a reflected voltage, the diode forward drop divided by the transformer turns ratio:

$$V_r = \frac{V_f}{N} \tag{7-59}$$

Since this reflected voltage is so low, it cannot bring the primary current back to its level at the beginning of the on time and so the current builds up at each pulse. In a short-circuit situation, either the clamp voltage runs away and the MOSFET quickly blows up, or the transformer saturates, leading to the same explosion! Figure 7-21 describes the situation.

In a start-up sequence, before the current reaches a high value, the output voltage rises and the reflected voltage starts to demagnetize the primary inductance. However, until a sufficient voltage imposes a proper downslope on the primary inductance, the current envelope peaks as described above. As predicted by Fig. 7-19, the clamping level goes out of control and the drain voltage dangerously increases. This is one of the major causes of power supply destruction at start-up. Figure 7-22 shows this behavior which must be seriously monitored when you design a high-power converter with a low primary inductance. In the presence of such difficulty, the solution lies in increasing the primary inductance, a choice which naturally limits peak current overshoots at high line. Another option consists of selecting a transient voltage suppressor.

7.7.6 TVS Clamp

A transient voltage suppressor (TVS) is nothing other than an avalanche diode (remember, zener effect occurs below 6.2 V; above, this is called the avalanche effect) able to take high-power pulses thanks to its large die size. The connection to the drain remains similar to that of the *RCD* clamp, as Fig. 7-23a shows. The TVS will clamp the voltage excursion of the drain, dissipating all the power as the clamp resistor would do. The TVS dynamic resistance being

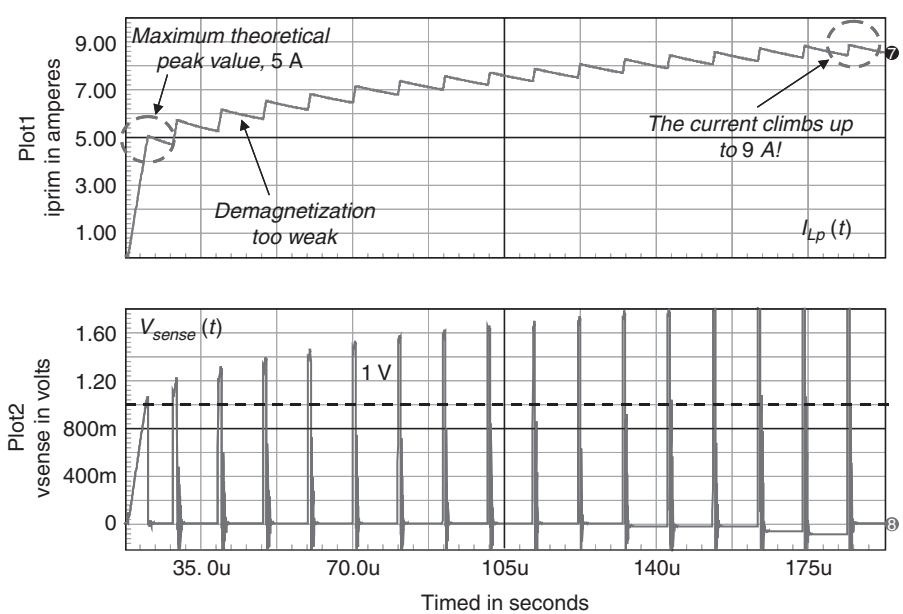

FIGURE 7-21 In short-circuit conditions, the current escapes from the PWM chip vigilance and runs out of control.

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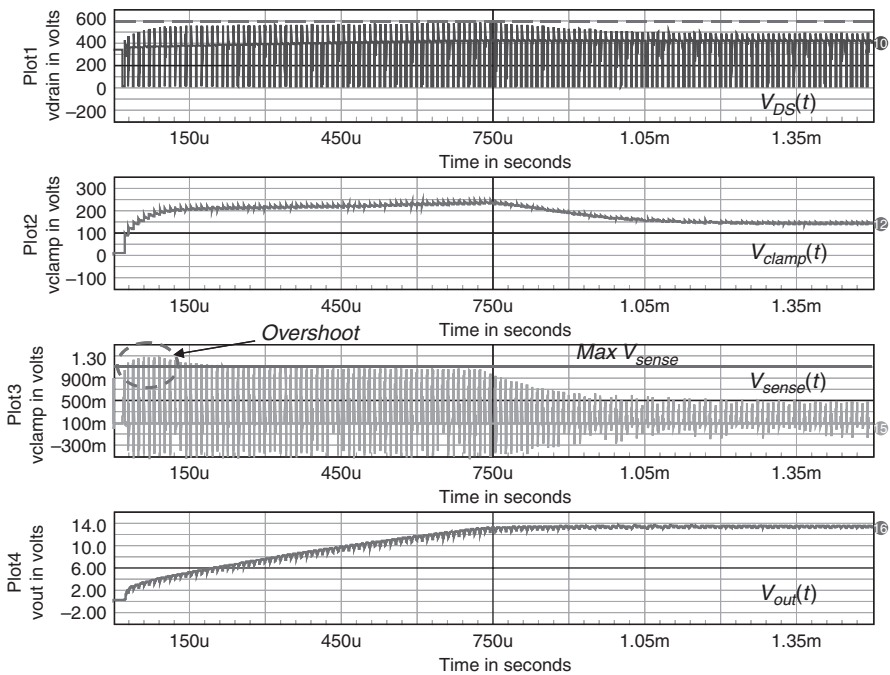

FIGURE 7-22 At start-up the peak current envelope can quickly increase, possibly engendering an increase of the clamp voltage. Carefully check this out once the design is finalized!

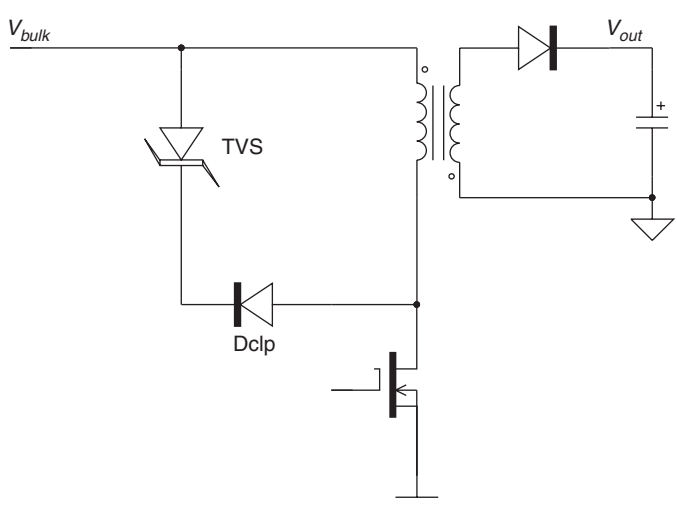

FIGURE 7-23a The TVS connects like an *RCD* clamp, offering a low-impedance clamping effect, which is less sensitive to current variations.

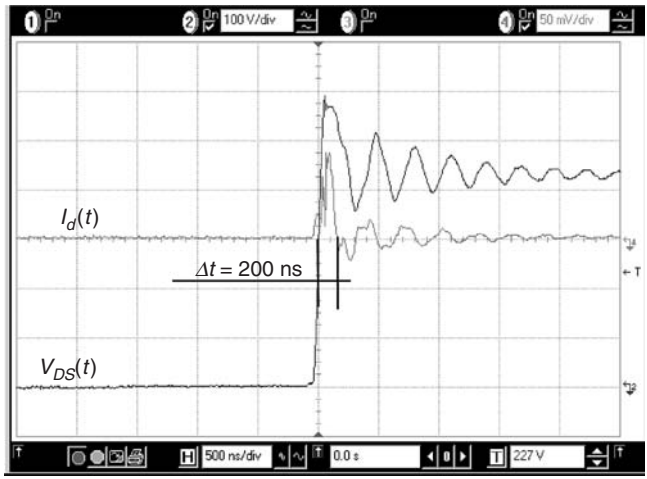

FIGURE 7-23b The TVS signature reveals an extremely brief conduction time, potentially radiating EMI noise.

small, its clamping voltage keeps rather constant despite large current variations. The dissipated power remains an important parameter to assess when the voltage selection is done. Capitalizing on the previously derived equations, the power dissipated by the TVS can be expressed as

$$P_{TVS} = \frac{1}{2} F_{sw} L_{leak} I_{peak}^2 \frac{V_z}{V_z - \frac{V_{out} + V_f}{N}} \tag{7-60a}$$

where V_z represents the TVS breakdown voltage. Figure 7-23b shows a TVS typical signature, on the same converter we used for the Fig. 7-18 shots. As one can see, the TVS sharply clamps for a short time, 200 ns in the example. This narrow pulse can often radiate a wide spectrum of noise, and this is a reason (besides its cost) why the TVS is not very popular in high power applications. Make sure all connections are kept short, and place the TVS and its diode (here an MUR160) close to the transformer and the MOSFET. In rather leaky designs, some designers even place a 10 nF in parallel with the TVS to help absorb the current pulses.

The TVS offers one big advantage: in standby or in light-load conditions, the peak current remains low and the leakage kick is often not sufficient to reach the TVS breakdown voltage. It thus stays transparent, and the converter efficiency benefits from this operation. Without TVS, as the converter enters light load via skip cycle (a very common technique these days), the capacitor in the *RCD* network cannot keep up the clamp voltage as the recurrence between switching bursts goes down. Hence, the capacitor being discharged at each new switching bunch of pulses, it enters into action and dissipates a bit of power: the no-load standby power suffers from the situation.

7.8 TWO-SWITCH FLYBACK

One of the major limits in power delivery that the flyback suffers from can be linked to the presence of the leakage inductor. We have seen that classical single-switch solutions deal with this problem by routing the leakage energy to an external network: the energy is lost in heat, and the efficiency suffers. To use the flyback in higher power configurations, the two-switch structure might represent a possible solution. Figure 7-24a shows the application circuit. The architecture

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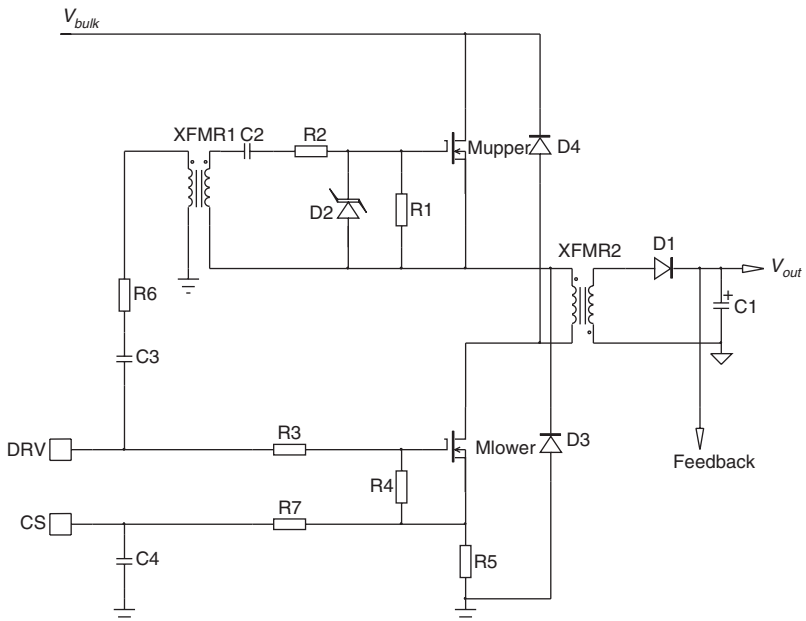

FIGURE 7-24a A two-switch flyback converter recycles the leakage energy at the opening of switches.

now uses two high-voltage MOSFETs but of smaller BV_{DSS}, compared to the single-switch approach. For instance, on a 400 V rail (assuming a PFC front-end stage), 500 V types can be implemented, implying a slightly better $R_{DS(on)}$ than their 600 V counterparts. The MOSFETs are turned on and off at the same time (same control voltage applied on the gate, the upper side floating with respect to ground). When both switches are conducting, the primary winding "sees" the bulk voltage. As the primary current reaches the peak limit, the controller classically instructs the switches to open. The current keeps circulating in the same direction and finds a path through the freewheel diodes D_3 and D_4. The transformer primary inductor immediately clamps to the reflected output voltage, and the leakage inductance resets with the following slope:

$$S_{leak} = \frac{V_{bulk} - \dfrac{V_{out} + V_f}{N}}{L_{leak}} \tag{7-60b}$$

If you carefully observe Fig. 7-24b, the current circulates via the bulk capacitor, naturally recycling the leakage energy: the efficiency clearly benefits from this fact. The secondary-side diode current ramps up at a pace imposed by the leakage reset, rather slow given the longer leakage reset time inherent to the structure. Yes, you have guessed it; if you reflect more voltage than the input voltage, your colleagues are going to applaud at the first power-on!

Figure 7-24c offers a way to simulate the two-switch flyback using a dedicated current-mode controller. You could also try to reproduce the Fig. 7-24a transformer-based driving circuit, but it would take a longer simulation time. By the way, best practice would be to use a transformer made of two secondary windings for a perfect propagation delay match between the two transistors. If you understand the sentence "cost down!" then you understand why it becomes a single winding based. A bootstrapped solution could be used, but at the expense of a small refresh circuitry for the capacitor. We will come back to this with the two-switch forward example. Figure 7-24d collects all pertinent waveforms obtained from the simulator. As you can see on

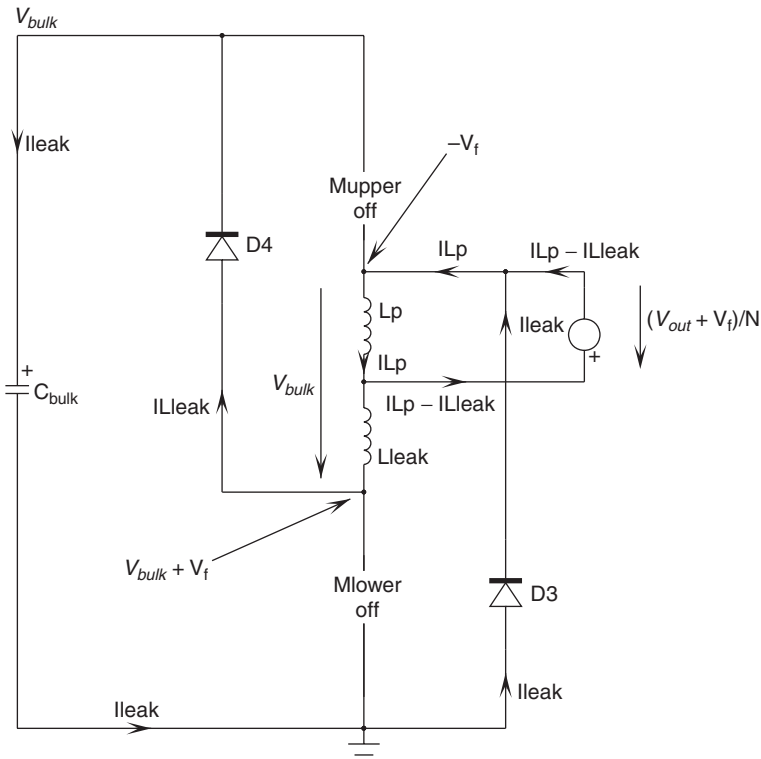

FIGURE 7-24b At the switch opening, the leakage current circulates through the freewheeling diodes, giving energy back to the bulk capacitor.

the upper trace, the leakage reset is rather smooth, something immediately seen on the secondary side diode current. However, this time, the reset duration does not generate losses dissipated in heat, but it brings the energy back to the bulk capacitor (see the positive jump on the source current, trace 10).

Despite its numerous benefits, such as leakage recycling, the two-switch flyback application has less success in the power supply industry than its two-switch forward counterpart.

7.9 ACTIVE CLAMP

The flyback with active clamp is currently gaining in popularity thanks to the ATX world requiring more efficient power supplies at a lower cost. The single-switch flyback with active clamp offers a possible alternative to the classical two-switch forward which can have difficulties in meeting the new ATX efficiency requirements: the total power supply efficiency is not allowed to drop below 80% for a loading ranging from 20 to 100% of the nominal power, thus its name, the 80+ initiative. The next step is to increase from 80 to 85%.

The principle behind the idea of active clamp still implies a capacitor storing the leakage energy at turn-off. However, rather than being simply dissipated in heat, the stored energy

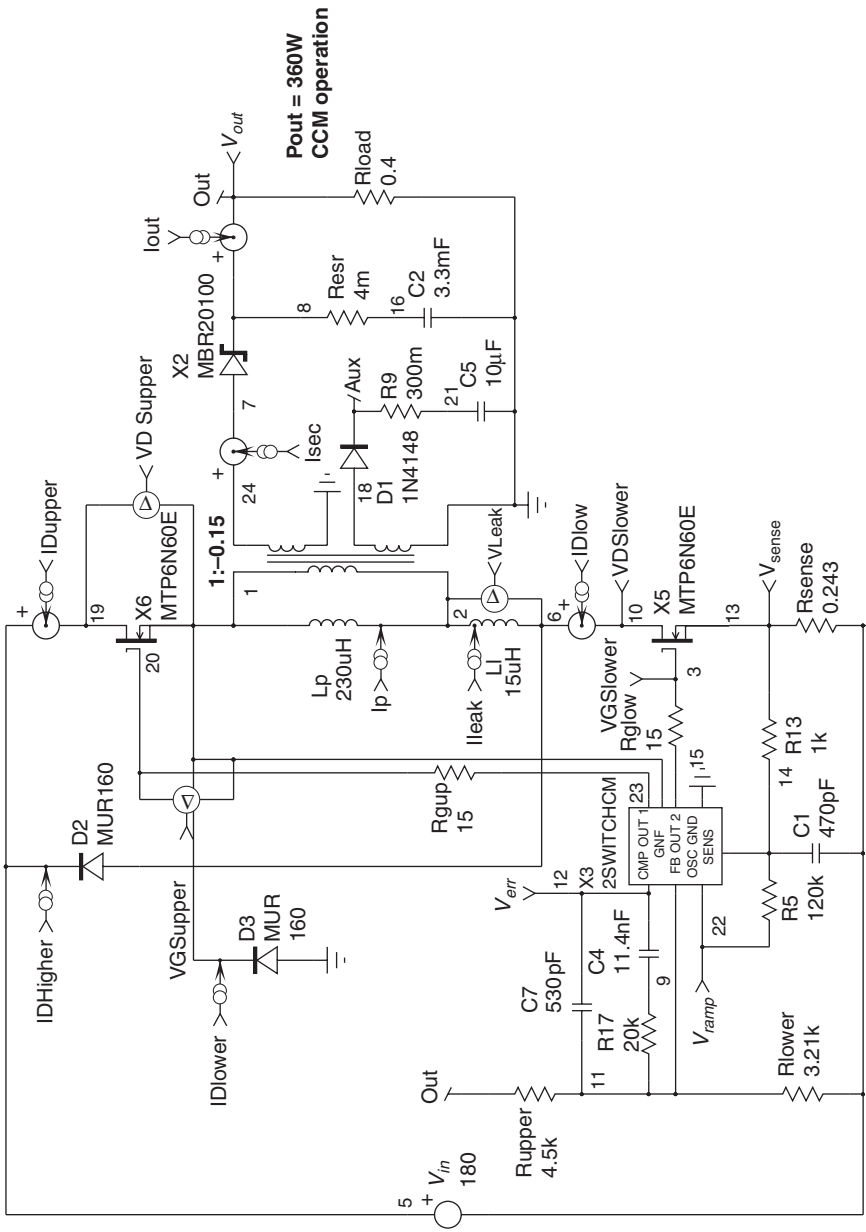

FIGURE 7-24c The SPICE simulation of the two-switch flyback converter, here a 360 W example.

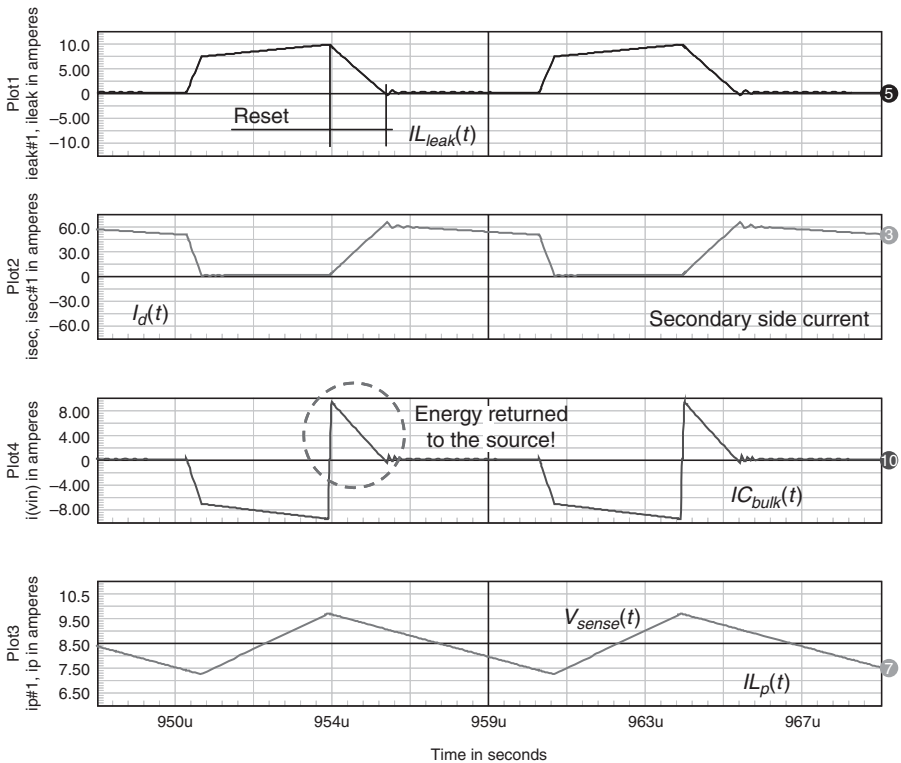

FIGURE 7-24d The simulation waveforms show the reset time slowing down the secondary side current.

is recycled to bring the drain voltage down to zero, naturally ensuring ZVS operation. This helps to (1) expand the use of the single-switch flyback beyond 150 W without paying switching losses incurred by the *RCD* clamp technique and (2) significantly increase the operating switching frequency, leading to the selection of lower size magnetic elements. This topic has been the subject of many comprehensive papers [3, 4, 5, and 6], and we will only scratch the surface here.

Figure 7-25 shows the flyback converter to which an active clamp circuit has been added. The system associates a capacitor (connected either to the bulk rail or to the ground) to a bidirectional switch made of SW and the diode D_{body}. This role can be played by a MOSFET, an N- or a P-channel, depending on the adopted reset scheme. To understand the operation, it is necessary to segment the various events in separate sketches and time intervals. Figure 7-26a and b gathers all these sketches, we comment on them one by one with illustrating graphics at the end.

In Fig. 7-26a, sketch a, the power switch has been turned on, as in any flyback operation. The current rises linearly with a slope dependent upon the input voltage and the combination of the leakage element with the primary inductance:

$$S_{on} = \frac{V_{in}}{L_p + L_{leak}} \tag{7-61}$$

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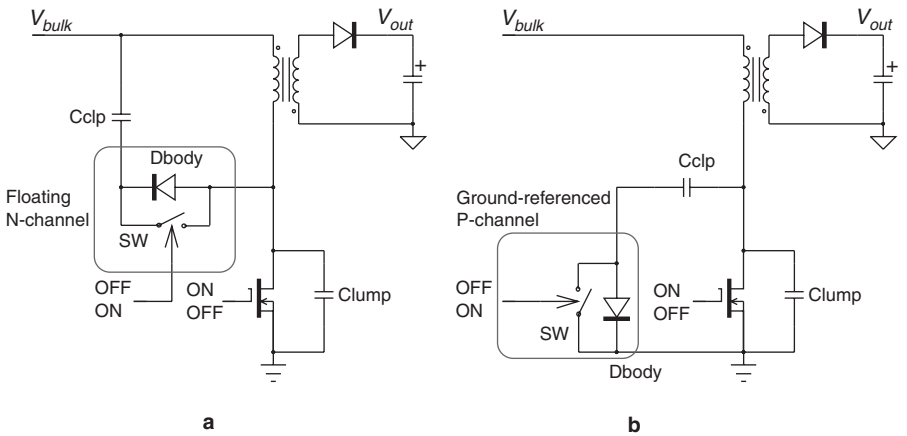

FIGURE 7-25 An active clamp circuit around a flyback converter uses a capacitor and a bidirectional switch.

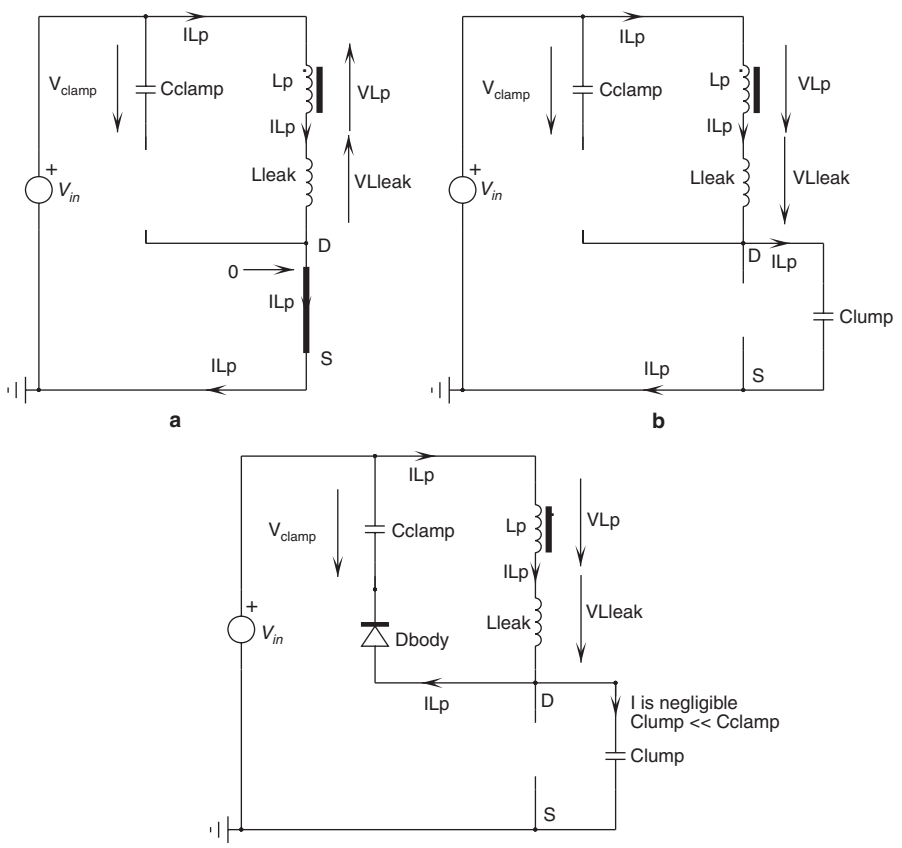

FIGURE 7-26a Different phases of the active clamp flyback converter. Here the secondary side diode still does not conduct.

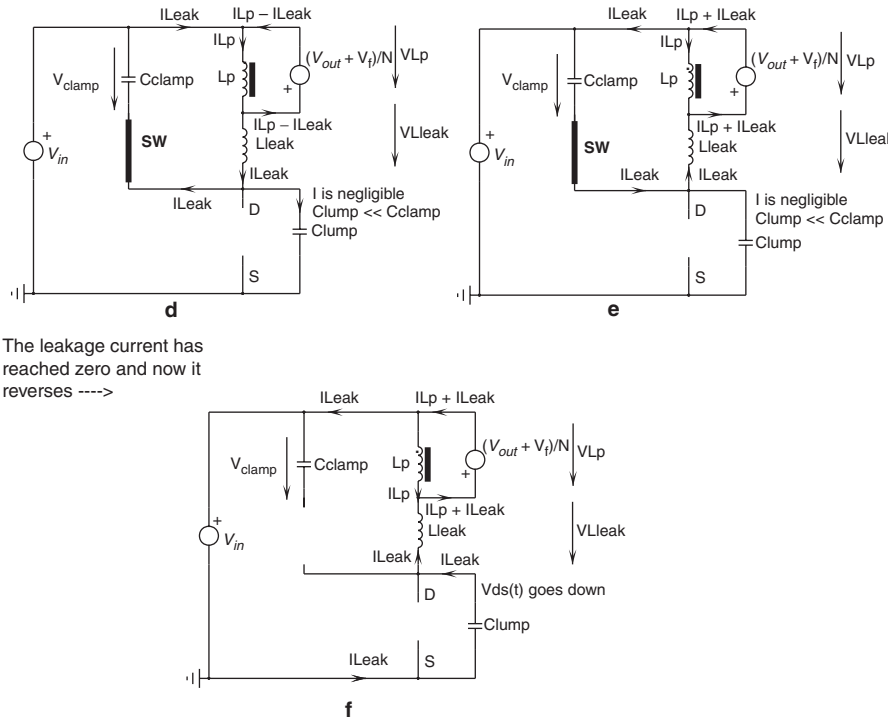

FIGURE 7-26b As the secondary diode conducts, the voltage across the primary inductance L_p is fixed to reflected voltage.

During this time, the input voltage splits between both terms as follows:

$$V_{L_p} = V_{in}\frac{L_p}{L_p + L_{leak}} \tag{7-62}$$

$$V_{L_{leak}} = V_{in}\frac{L_{leak}}{L_p + L_{leak}} \tag{7-63}$$

When the peak current reaches the set point imposed by the feedback loop ($I_{L,peak} = I_{peak}$), the power switch opens and the magnetizing current charges the lump capacitor. We are observing sketch b. The drain voltage immediately rises at a rate defined by Eq. (7-64):

$$\frac{dV_{DS}(t)}{dt} = \frac{I_{peak}}{C_{lump}} \tag{7-64}$$

The voltage increases until it reaches the level imposed by the stored voltage present across the clamping capacitor V_{clamp} plus the input voltage V_{in}. At this time, the upper-switch body diode starts to conduct, and we are looking at sketch c. As the lump capacitor is much smaller than the clamp capacitor, it no longer diverts current and we can consider all the magnetizing current flowing through C_{clamp}. Note that we already had a resonant transition at the switch opening between C_{lump} and the total inductance made up of $L_{leak} + L_p$, but since its duration is short, you almost observe a linear waveform.

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The clamp capacitor now fixes the voltage across both inductors $L_{leak} + L_p$ which act as a voltage divider. The voltage splits as follows:

$$V_{L_p} = -V_{clamp}\frac{L_p}{L_p + L_{leak}} \tag{7-65}$$

When the primary voltage has fully reversed to a point where the secondary diode conducts, we are now observing Fig. 7-26b, sketch d. Since the body diode is conducting ($V_{DS} = 0$), we can safely turn on the upper switch SW to benefit from zero voltage conditions across it. A small delay is thus necessary to let this body diode first conduct before activating the upper-side switch. The primary current classically decays at a slope imposed by the reflected voltage:

$$S_{off} = -\frac{V_{out} + V_f}{NL_p} \tag{7-66}$$

The leakage inductor now resonates with the clamp capacitor, and a sinusoidal waveform arises. The resonant frequency involves the leakage inductance and the clamp capacitor (neglecting the lump capacitor):

$$f_{reso1} = \frac{1}{2\pi\sqrt{L_{leak}C_{clamp}}} \tag{7-67}$$

The secondary side current is made up of the difference between the linear current delivered by the primary inductance [Eq. (7-66)] and the sinusoidal waveform drawn by the leakage term:

$$I_d(t) = \frac{I_{L_p}(t) - I_{L_{leak}}(t)}{N} \tag{7-68}$$

In a classical flyback, this period of time, where the leakage inductance diverts current, would be kept small as we want to reset the leakage term as quickly as possible. With the active clamp technique, on the contrary, the leakage term diverts current during the whole off time and actually turns on the secondary diode very smoothly.

When the resonant current waveform reaches zero, the current reverses and starts to flow in the other direction. It can do so thanks to the presence of the upper-side switch, still kept closed for the event. We are looking at sketch e. At a certain time, the leakage inductor current will reach a negative peak. The stored energy at this moment is simply

$$E_{L_{leak}} = \frac{1}{2}L_{leak}I_{peak}^2 \tag{7-69}$$

If we now open the upper-side switch, the leakage inductance current still flows in the same direction but now returns via the lump capacitor, creating a new resonance:

$$f_{reso2} = \frac{1}{2\pi\sqrt{L_{leak}C_{lump}}} \tag{7-70}$$

The current flowing through the lump capacitor now from the ground contributes to discharge it. The minimum of the voltage is reached at one-quarter of the period. Hence, if a delay is added to let the voltage swing to its valley, we can ensure zero voltage switching on the power MOSFET. This delay should be adjusted to

$$t_{del} = \frac{2\pi\sqrt{L_{leak}C_{lump}}}{4} = \frac{\pi}{2}\sqrt{L_{leak}C_{lump}} \tag{7-71}$$

The necessary condition to bring the lump capacitor down to zero implies that the energy stored in the leakage inductance at the switch opening [Eq. (7-69)] equals or exceeds the energy stored in the lump capacitor. Otherwise stated,

$$\frac{1}{2}L_{leak}I_{peak}^2 \geq \frac{1}{2}C_{lump}\left[V_{in} + \frac{V_{out} + V_f}{N}\right]^2 \tag{7-72}$$

Capitalizing on this equation, we can extract a design law to obtain the resonant/leakage inductor value:

$$L_{leak} \geq \frac{C_{lump}\left(V_{in} + \frac{V_{out} + V_f}{N}\right)^2}{I_{peak}^2} \tag{7-73}$$

In the above equation, the peak current at the switch opening is approximated by the peak current imposed by the controller at the end of the on time. In practice, given the damping action (ohmic losses), the final value slightly differs from this value. If the current at the upper-side switch opening moment is too low, the lump capacitor cannot properly discharge down to zero because Eq. (7-72) will not be satisfied. To solve this problem, you will need to either artificially increase the leakage term by inserting an inductor connected in series with the transformer primary or weaken the coupling between both primary and secondary windings, for instance, by using a different bobbin architecture. The peak current in Eq. (7-73) can be derived using equations already seen in Chap. 5 in the buck-boost section [Eqs. (5-99) and (5-100)]. Combining them leads to the definition of this peak current level

$$I_{peak} \approx I_{L,avg} + \frac{\Delta I_{L_p}}{2} = P_{out}\left(\frac{1}{\eta V_{in}} + \frac{N}{V_{out}}\right) + \frac{V_{in}D}{2L_pF_{sw}} \tag{7-74}$$

Since the leakage inductance is defined, we can calculate the value of the clamp capacitor. Its value depends on the off-time duration at high line such that one-half of the resonant period always remains larger than the largest off-time duration. Otherwise, the negative peak in the resonance waveform might no longer correspond to the upper-side switch opening event, losing the relationship described by Eq. (7-72). Hence, the design obeys the following equation:

$$\frac{t_{res1}}{2} \geq (1 - D_{min})T_{sw} \tag{7-75}$$

Replacing t_{res1} with its definition [Eq. (7-67)] and extracting the clamp capacitor value, we have

$$\pi\sqrt{L_{leak}C_{clamp}} \geq (1 - D_{min})T_{sw} \tag{7-76}$$

$$C_{clamp} \geq \frac{(1 - D_{min})^2}{F_{sw}^2\pi^2L_{leak}} \tag{7-77}$$

7.9.1 Design Example

To capitalize on the above equations, it is time to verify our assumptions with a simulated example. We can start from an initial flyback design to which we apply the active clamp

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technique. The design procedure difference between a flyback operated with or without active clamp is minor as long as we consider the leakage term negligible compared to the magnetizing inductor.

$$L_{leak} << L_p \tag{7-78}$$

Reference 6 calculates the duty cycle on a nonactive clamp flyback and compares it to an active clamp-operated converter. The difference remains about a few percent. What changes, however, concerns the maximum drain excursion at the switch opening. In a normal flyback operated with a classical *RCD* clamping network, the drain remains theoretically blocked below

$$V_{DS} = V_{in} + \frac{V_{out} + V_f}{N} + V_{clamp} \tag{7-79}$$

With an active clamp, the voltage developed across the leakage inductance during its resonating phase comes in series with the two first terms of Eq. (7-79). The excursion thus follows Eq. (7-80) [6]:

$$V_{DS} \approx V_{in} + \frac{V_{out} + V_f}{N} + \frac{2L_{leak}P_{out}}{\eta V_{in,max} D_{min}(1 - D_{min})} \tag{7-80}$$

The normal procedure would be to first fix the drain-source excursion desired (given the selected MOSFET) and then calculate the remaining elements. Unfortunately, the leakage term already appears in Eq. (7-80). However, as expressed by Eq. (7-78), we can arbitrarily pick up a value around 10% of the magnetizing inductance and see what turns ratio is authorized in relation to the MOSFET breakdown voltage. Later on, once the final leakage term is calculated, you have the possibility of rechecking the result of Eq. (7-80) and going for another pass if necessary.

The flyback we want to use features the following parameters:

$L_p = 770\ \mu H$
$L_{leak} = 12\ \mu H$
$1{:}N = 1{:}0.166$
$V_{in,max} = 370$ Vdc
$V_{in,min} = 100$ Vdc
$V_{out} = 19$ V
$I_{out,max} = 4$ A
$P_{out,max} = 76$ W
$F_{sw} = 65$ kHz
$C_{lump} = 220$ pF (measured according to App. 7A principles)
$\eta = 85\%$ (considered constant at low and high line for simplicity)

The duty cycle variations are computed first:

$$D_{max} = \frac{V_{out}}{V_{out} + NV_{in,min}} = \frac{19}{19 + 0.166 \times 100} = 0.534 \tag{7-81}$$

$$D_{min} = \frac{V_{out}}{V_{out} + NV_{in,max}} = \frac{19}{19 + 0.166 \times 370} = 0.236 \tag{7-82}$$

The high- and low-line peak currents reach [Eq. (7-74)]

$$I_{peak,high-line} \approx 76 \times \left(\frac{1}{0.85 \times 370} + \frac{0.166}{19}\right) + \frac{370}{2 \times 770u \times 65k} \times 0.236 = 1.8\,\text{A} \quad (7\text{-}83)$$

$$I_{peak,low-line} \approx 76 \times \left(\frac{1}{0.85 \times 100} + \frac{0.166}{19}\right) + \frac{100}{2 \times 770u \times 65k} \times 0.534 = 2.1\,\text{A} \quad (7\text{-}84)$$

With this information in hand, let us determine the needed resonating inductor:

$$L_{leak} \geq \frac{C_{lump}\left(V_{in} + \dfrac{V_{out} + V_f}{N}\right)^2}{I_{peak}{}^2} \geq \frac{220p \times \left(370 + \dfrac{19 + 1}{0.166}\right)^2}{1.8^2} = 16.3\,\mu\text{H} \quad (7\text{-}85)$$

Allowing a bit of margin, we add a small inductor of 8 μH in series with the transformer since the original leakage term already totals 12 μH (L_{leak} total = 20 μH). The rms current flowing into the added leakage inductor combines the main magnetizing current and the circulating clamp current. Reference 6 gives the following formula, reaching its maximum at low line:

$$I_{L_{leak},rms} = \sqrt{\frac{\left(\dfrac{P_{out}}{\eta V_{in,min} D_{max}}\right)^2 (2D_{max} + 1) + \dfrac{P_{out}}{\eta L_p F_{sw}}(1 - D_{max}) + \dfrac{1}{4}\left(\dfrac{V_{in,min} D_{max}}{L_p F_{sw}}\right)^2}{3}} = 1.52\,\text{A} \quad (7\text{-}86)$$

Its maximum peak current is of course similar to that of Eqs. (7-83) and (7-84). Equation (7-87) now helps us to calculate the clamping capacitor value.

$$C_{clamp} \geq \frac{(1 - D_{min})^2}{F_{sw}{}^2 \pi^2 L_{leak}} \geq \frac{(1 - 0.236)^2}{65k^2 \times 3.14^2 \times 20u} \geq 699\,\text{nF} \quad (7\text{-}87)$$

The voltage rating for this capacitor must exceed the reflected voltage plus the voltage developed across the leakage inductor. Using Eq. 7-80, we simply remove the first term:

$$V_{C_{clamp},max} \approx \frac{V_{out} + V_f}{N} + \frac{2L_{leak} P_{out}}{\eta V_{in,max} D_{min}(1 - D_{min})}$$

$$= \frac{19 + 1}{0.166} + \frac{2 \times 20u \times 76}{0.85 \times 370 \times 0.236 \times (0.764)} = 120\,\text{V} \quad (7\text{-}88)$$

Finally, the ripple current circulates during the off time and obeys Eq. (7-89) [6]. The worst case occurs at low line:

$$I_{C_{clamp},rms} = I_{peak,max}\sqrt{\frac{1 - D_{max}}{3}} = 2.1\sqrt{\frac{1 - 0.534}{3}} = 0.83\,\text{A} \quad (7\text{-}89)$$

As a final check, Eq. (7-80) predicts a voltage excursion of 490 V. Our MOSFET breaks at 600 V, so we are safe.

Now that we have all resonant elements on hand, we can evaluate the upper-switch opening delay necessary to obtain ZVS on the MOSFET drain:

$$t_{del} = \frac{\pi}{2}\sqrt{L_{leak}C_{lump}} = 1.57 \times \sqrt{20u \times 220p} = 104\,\text{ns} \tag{7-90}$$

7.9.2 Simulation Circuit

The circuit we used for the simulation example appears in Fig. 7-27. It implements the generic controller already developed for a synchronous rectification application. Output 1 drives the main switch whereas output 2 goes to the upper-side switch. Since its source floats, a real application would require a transformer or a high-voltage high-side driver such as the NCP5181 from ON Semiconductor. We removed any isolation circuit to reduce the complexity.

The controller switches at 65 kHz, and a 100 ns delay is inserted between both outputs. In theory, the first delay should be independently adjusted to let the body diode ensure ZVS on the upper-side switch. The second delay should then match the result of Eq. (7-90). Practically, a similar dead time is inserted without known operating problems. Figure 7-28a gathers a series of operating plots at high line. In this figure, we can see on the upper plot that both magnetizing current and resonant current are following the same shape at turn-on, but they diverge during the off time: the magnetizing current decreases linearly whereas the leakage current resonates with the clamp capacitor. Note that the secondary current smoothly

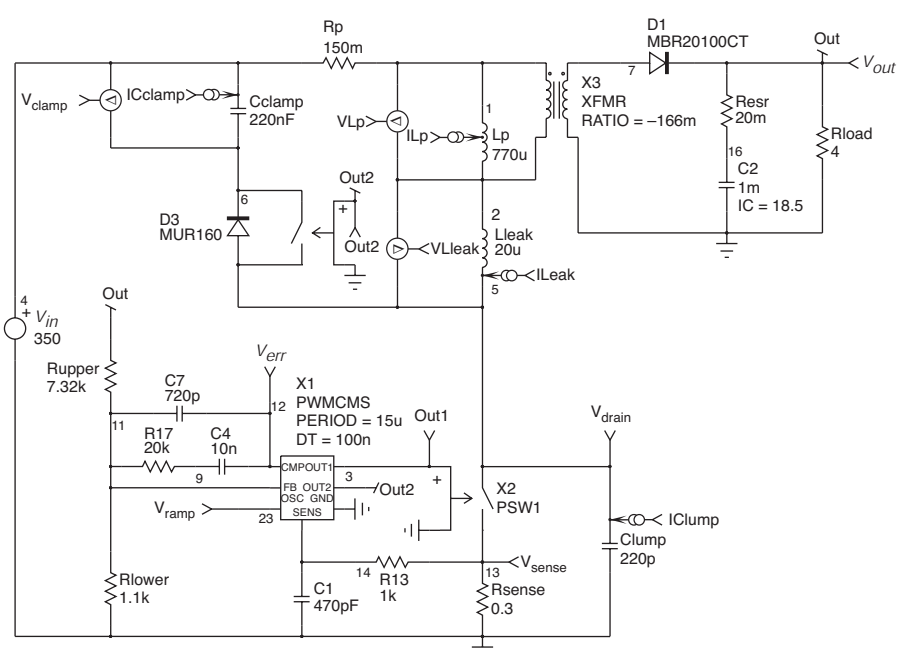

FIGURE 7-27 The active clamp simulation circuit using the synchronous generic controller.

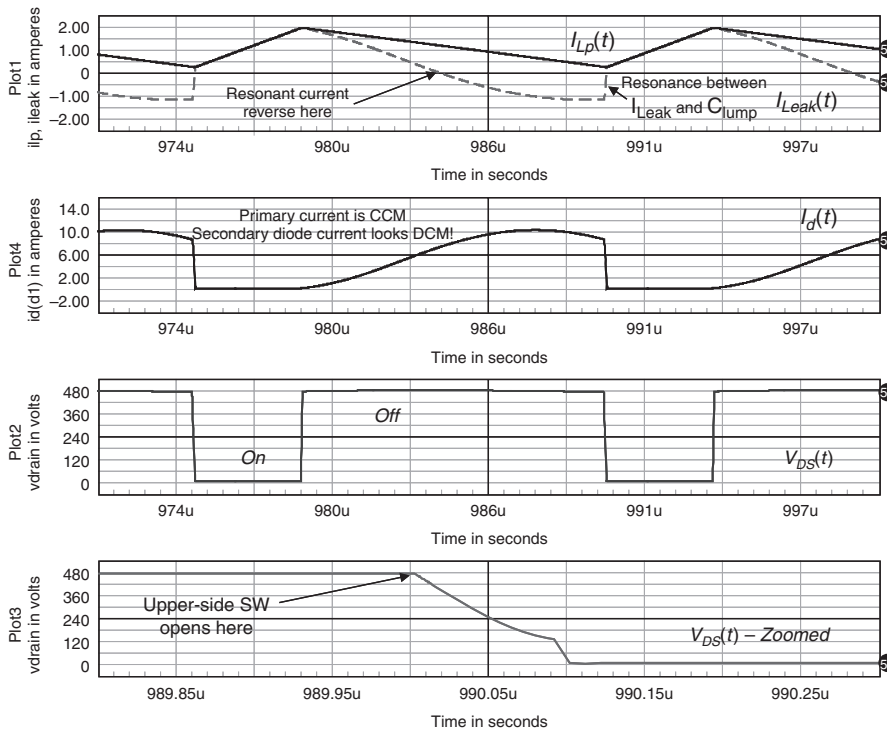

FIGURE 7-28a Typical signals of the active clamp flyback converter with an input voltage of 350 Vdc.

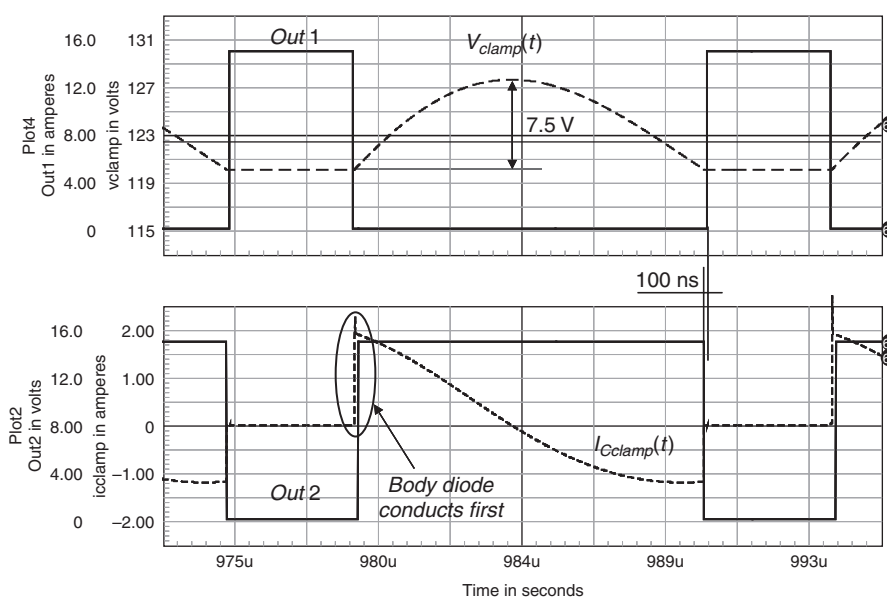

FIGURE 7-28b The clamp capacitor voltage does not significantly increase during the off time.

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increases in the diode and looks as if it was DCM despite CCM on the primary side! This implies a higher peak current compared to a similar CCM flyback without active clamp, but switching losses on the diode are greatly reduced. The middle and last plots depict the drain voltage which stays almost flat on the plateau. On the zoom, you can clearly see the valley jump as soon as the upper-side switch opens. The delay seems well adjusted on this simulation. We should probably be able to force the wave farther down by increasing the leakage term.

Figure 7-28b focuses on the clamp voltage and shows that its voltage stays relatively constant during the transformer core reset. The bottom plot represents the clamp capacitor current and shows that it starts to flow before output 2 biases the upper-side switch: ZVS is ensured.

Figure 7-28c gathers plots where the clamp capacitor has been changed. Swept values are 220 nF, 680 nF, and 1 µF. When the capacitor no longer satisfies Eq. (7-77), C_{clamp} = 220 nF, the valley turn-on is lost on the main power MOSFET. However, the drain voltage excursion does not suffer from these variations.

The small-signal characteristic of the flyback converter operated with an active clamp does not significantly change compared to a traditional converter, as long as the clamp capacitor remains small compared to the reflected output capacitor.

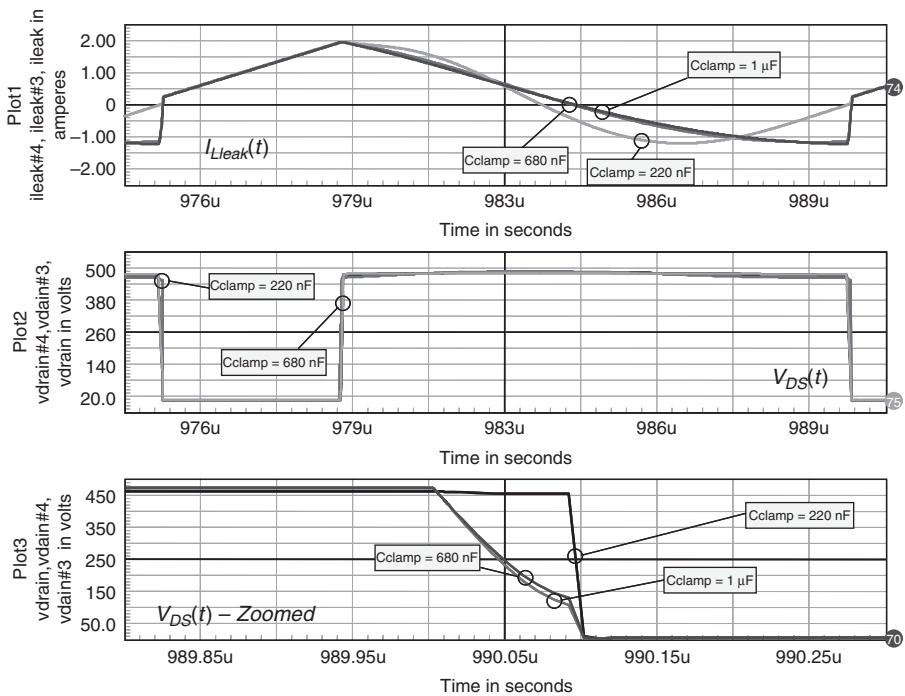

FIGURE 7-28c Three different clamp capacitor values have been swept: 220 nF, 680 nF, and 1 µF. If the maximum voltage excursion on the drain remains almost unchanged, the ZVS can be easily lost at low clamp capacitor values.

7.10 SMALL-SIGNAL RESPONSE OF THE FLYBACK TOPOLOGY

The flyback converter small-signal response does not differ from that of the buck-boost converter. Its dynamic behavior is affected by the operating mode, CCM or DCM, as well as the way the duty cycle is elaborated (voltage mode or current mode). Using the autotoggling models of the PWM switch represents an interesting exercise to explore the flyback small-signal response when operated in these various modes. Figures 7-29 and 7-30 depict how to wire the model in a single-output configuration. The converter delivers 19 V to a 6 Ω load (3.2 A), and we changed its primary inductance depending on the needed mode (CCM or DCM). The value at which the operating mode changes, given a certain input voltage (here 200 V), is called the *critical inductance*. Above this value, the converter delivering its nominal power will work in CCM. Below it, the converter will enter DCM. The critical inductance value can be derived by using formulas already seen in Chap. 1, the buck-boost section:

$$L_{p,crit} = \frac{R_{load}}{N^2 2F_{sw}} \left(\frac{1}{1 + \frac{V_{out}}{NV_{in}}} \right)^2 = \frac{6}{0.166^2 \times 2 \times 65k} \left(\frac{1}{1 + \frac{19}{0.166 \times 200}} \right)^2 = 677\,\mu\text{H} \tag{7-91}$$

For the DCM converter, L_p will be fixed to 450 μH and for the CCM version, 800 μH. Let us now plot the Bode plot responses of the voltage-mode converter in both DCM and CCM (Fig. 7-29b). In DCM, the converter behaves as a first-order system in the low-frequency portion of the graph. The phase starts to drop to reach −90°, but the zero introduced by the output capacitor ESR kicks in and strives to pull the phase back to zero. However, as the frequency increases, the combined action of the high-frequency RHPZ and pole further degrades the phase. Their action is usually ignored as the cutoff frequency is often chosen way below their acting point. Note that the very first generation of models was unable to predict their presence.

In voltage-mode CCM, we can observe the peaking linked to the equivalent inductor L_e resonating with the output capacitor. We have a second-order system, degrading the phase at the resonating peak. The crossover frequency f_c must therefore be selected to be at least three times above the resonant frequency to avoid compensation difficulties when the gain crosses over the 0 dB axis. It must also stay below the worst-case RHP zero frequency to prevent further phase stress.

Figure 7-30a portrays the same converter arranged in a current-mode configuration. The modulator gain block is gone, and the loop is opened in a similar manner as before. The ac results are given in Fig. 7-30b and show that, in the low-frequency portion, the DCM and CCM operations do not differ that much in terms of Bode plots: they both exhibit first-order behavior. The CCM converter, however, turns into a third-order system after the appearance of the double pole placed at one-half of the switching frequency. Care must be taken to damp these subharmonic poles; otherwise instability can occur for a duty cycle greater than 50%. In this example, there is no ramp compensation.

7.10.1 DCM Voltage Mode

In light of the above curves, it appears obvious that stabilizing a voltage-mode converter operated in DCM looks simpler than stabilizing the same in CCM. This explains why mode transition in voltage mode often causes stability problems: a converter stabilized for only DCM cannot properly work in CCM. On the contrary, a converter stabilized for CCM might behave poorly in DCM because of an excessive compensation. Below is a summary of the voltage-mode small-signal flyback parameters pertinent to the error-to-output path.

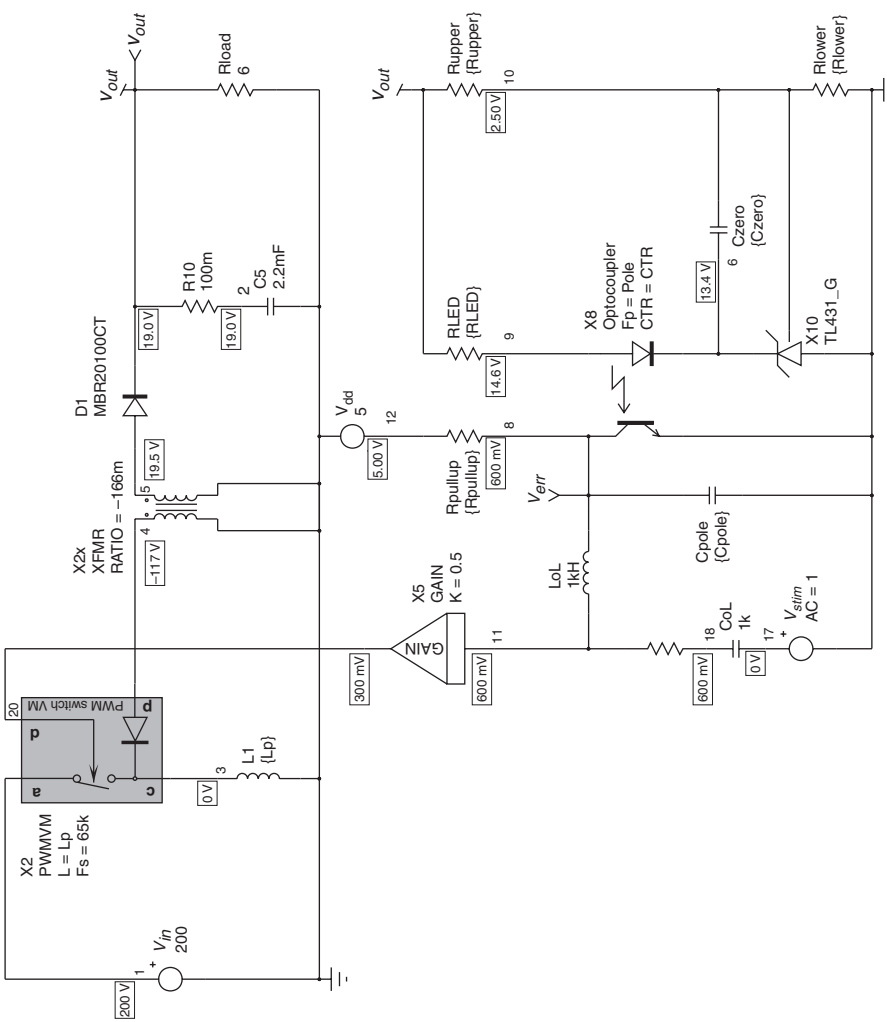

FIGURE 7-29a The flyback in a voltage-mode configuration. The –6 dB gain block brought by X_5 accounts for a 2 V peak amplitude sawtooth, and bias points are obtained after a DCM run.

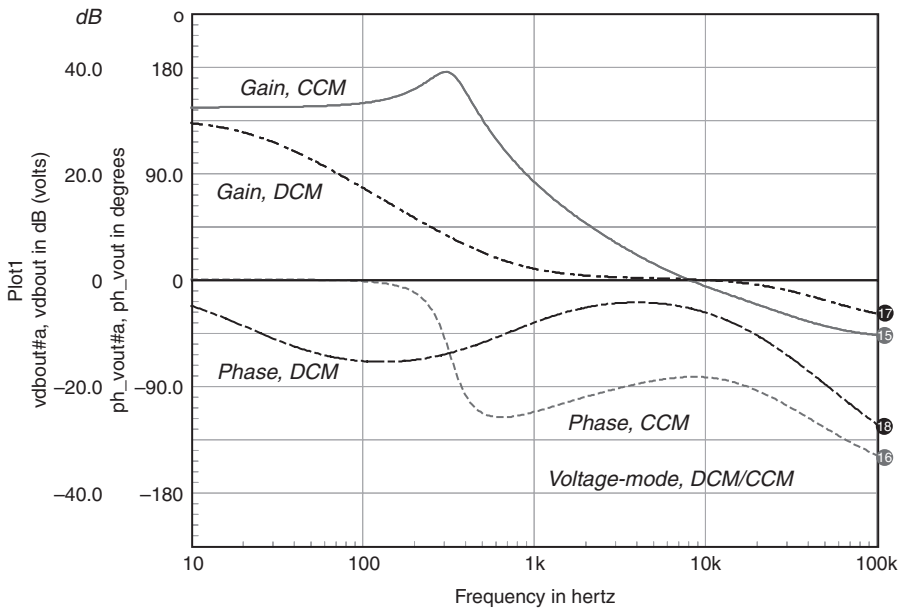

FIGURE 7-29b Bode plots of the voltage-mode converter operated in DCM or CCM. Under the same operating conditions, L_p is adjusted to change the mode. In CCM, the voltage-mode flyback behaves as a second-order system, which drops to a first-order in DCM.

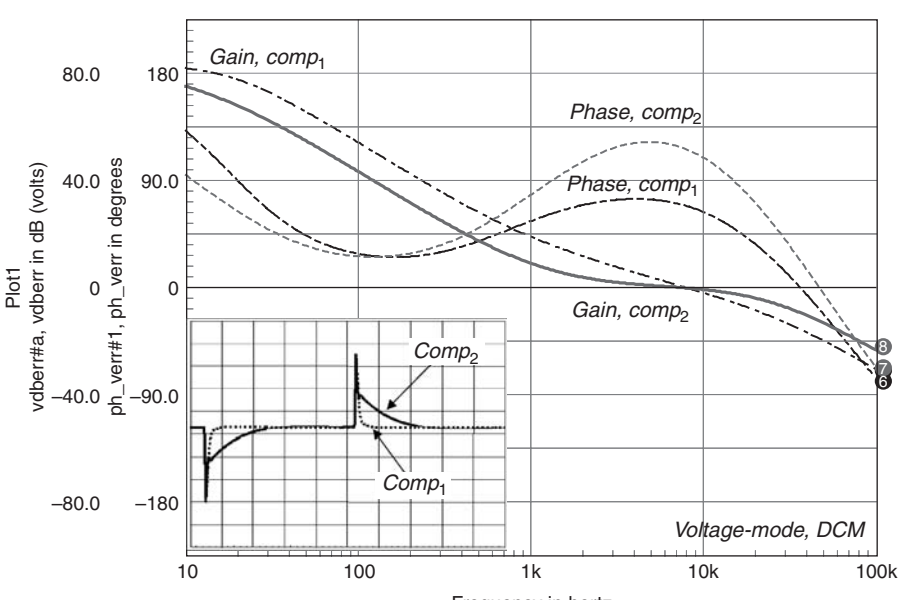

FIGURE 7-29c After compensation, despite a similar crossover frequency, the compensation featuring the zero positioned in the lower portion of the spectrum gives the slowest response (output current from 3 to 3.5 A).

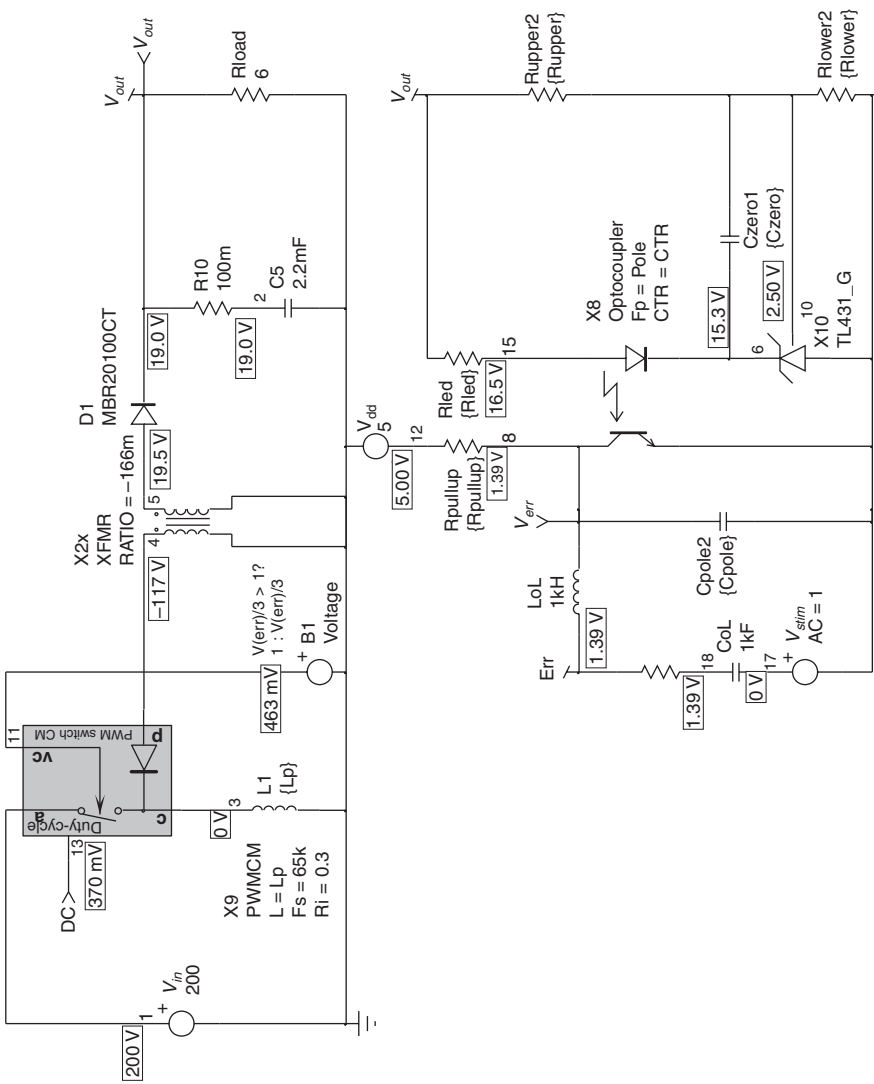

FIGURE 7-30a This is the same arrangement as before but in a current-mode configuration. The dc bias points correspond to a CCM simulation.

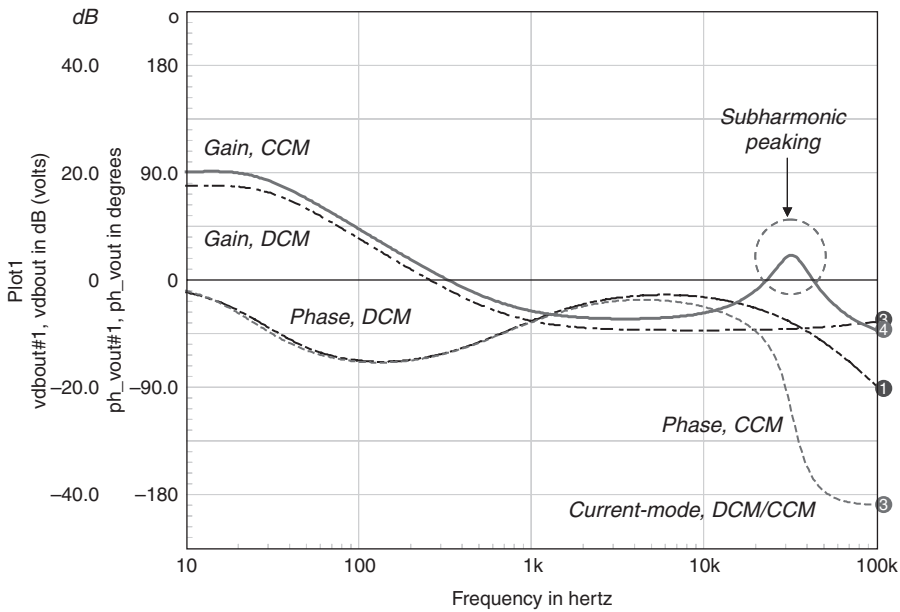

FIGURE 7-30b Bode plots of the current-mode converter operated in DCM or CCM. As previously indicated, L_p is adjusted to modify the mode.

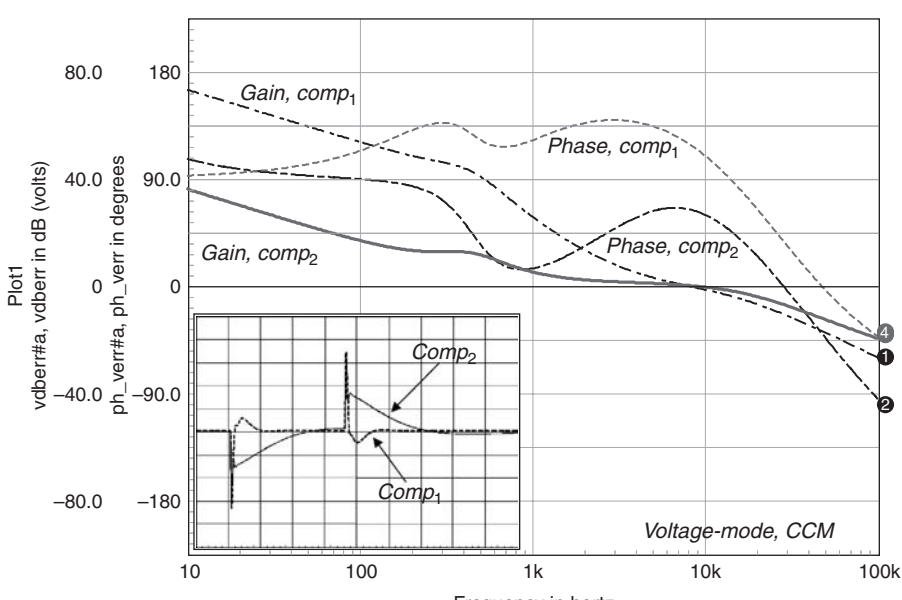

FIGURE 7-30c By changing the position of poles and zeros, conditional stability appears which can jeopardize the converter stability in some cases.

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Voltage-Mode Control

	DCM	CCM
First-order pole	$\frac{1}{\pi R_{load} C_{out}}$	—
Second-order pole	$\frac{F_{sw}}{\pi}\left(\frac{1/D}{1+\frac{NV_{in}}{V_{out}}}\right)^2$	$\frac{1-D}{2\pi N\sqrt{L_p C_{out}}}$ (double)
Left half-plane zero	$\frac{1}{2\pi R_{ESR} C_{out}}$	$\frac{1}{2\pi R_{ESR} C_{out}}$
Right half-plane zero	$\frac{R_{load}}{2\pi N\frac{V_{out}}{V_{in}}\left(1+\frac{V_{out}}{NV_{in}}\right)L_p}$	$\frac{(1-D)^2 R_{load}}{2\pi D L_p N^2}$
V_{out}/V_{in} dc gain	$\frac{V_{out}}{V_{in}}$	$\frac{V_{out}}{V_{in}}$
V_{out}/V_{error} dc gain	$\frac{V_{in}}{V_{peak}}\sqrt{\frac{R_{load}}{2L_p F_{sw}}}$	$\frac{V_{in}}{(1-D)^2 V_{peak}}$
Duty cycle D	$\frac{V_{out}}{V_{in}}\sqrt{\frac{2L_p F_{sw}}{R_{load}}}$	$\frac{V_{out}}{V_{out}+NV_{in}}$

where D = duty cycle
F_{sw} = switching frequency
R_{ESR} = output capacitor equivalent series resistance
M = conversion ratio = $M = \frac{V_{out}}{NV_{in}}$
L_p = primary inductance
R_{load} = output load
$N = \frac{N_s}{N_p}$ = transformer turns ratio
V_{peak} = PWM sawtooth amplitude

We have stabilized all converters with an 8 kHz crossover frequency and a phase margin of 70°. The DCM voltage-mode stabilization is a rather simple exercise considering the input voltage constant to 200 V and a load varying between 5 Ω (3.5 A) and 6 Ω (3 A). First, we need to calculate the position of the pole and zero inherent to this operating mode:

$$f_{p1,min} = \frac{1}{\pi R_{load,min} C_{out}} = \frac{1}{3.14 \times 5 \times 2.2m} = 29\,\text{Hz} \tag{7-92}$$

$$f_{p1,max} = \frac{1}{\pi R_{load,max} C_{out}} = \frac{1}{3.14 \times 6 \times 2.2m} = 24\,\text{Hz} \tag{7-93}$$

We now assume capacitor ESRs varying between 50 and 100 mΩ:

$$f_{z1,max} = \frac{1}{2\pi R_{ESR,min} C_{out}} = \frac{1}{6.28 \times 50m \times 2.2m} = 1.447\,\text{kHz} \tag{7-94}$$

$$f_{z1,min} = \frac{1}{2\pi R_{ESR,max} C_{out}} = \frac{1}{6.28 \times 100m \times 2.2m} = 723\,\text{Hz} \tag{7-95}$$

The high-frequency DCM RHPZ zero is evaluated; thus,

$$f_{z2} = \frac{R_{load}}{2\pi N \frac{V_{out}}{V_{in}}\left(1+\frac{V_{out}}{NV_{in}}\right)L_p} = \frac{6}{6.28 \times 0.166 \times \frac{19}{200}\left(1+\frac{19}{0.166 \times 200}\right)450u} = 85.6\,\text{kHz} \tag{7-96}$$

The second pole position depends on the DCM duty cycle. Thanks to Eq. (5-129), we can quickly obtain its value:

$$D = \frac{V_{out}}{NV_{in}}\sqrt{2\tau_L} = \frac{19}{0.166 \times 200}\sqrt{2 \times 0.138} = 0.3 \tag{7-97}$$

with

$$\tau_L = \frac{L_p N^2}{R_{load} T_{sw}} = \frac{450u \times 0.166^2}{6 \times 15u} = 0.138 \tag{7-98}$$

$$f_{p2} = \frac{F_{sw}}{\pi}\left(\frac{1/D}{1+\frac{NV_{in}}{V_{out}}}\right)^2 = \frac{65k}{3.14}\left(\frac{1/0.3}{1+\frac{0.166 \times 200}{19}}\right)^2 = 30.5\,\text{kHz} \tag{7-99}$$

The above formulas actually use results derived for a buck-boost converter but now include the transformer turns ratio for reflections on either side. The dc point in Fig. 7-29a confirms this result.

The dc gain linking the PWM input to the output stage can be obtained, given the PWM sawtooth peak amplitude (2 V in this example):

$$G_0 = 20\log_{10}\left[\frac{V_{in}}{V_{peak}}\sqrt{\frac{R_{load}}{2L_p F_{sw}}}\right] = 20\log_{10}\left[\frac{200}{2}\sqrt{\frac{6}{2 \times 450u \times 65k}}\right] = 30\,\text{dB} \tag{7-100}$$

This value is also confirmed by the Bode plot shown in Fig. 7-29b. Now that we have all in place, how do we compensate the whole thing? We can either use the k factor which gives adequate results in DCM or decide to place the corrective poles and zeros ourselves. Looking at Fig. 7-29b, we can see that an 8 kHz bandwidth requires no gain at all at the crossover point. The phase lag at this place is around −25°. A candidate for this compensator could be a simple type 1. The type 1 can work as long as the phase lag does not exceed −40° at the crossover point since no phase boost is provided by this structure. Otherwise, a type 2 can also do the job by placing the following poles and zeros:

- One pole at this origin, giving a high dc gain, thus a low dc output impedance and a good dc input rejection.
- A zero placed below the crossover frequency to bring the necessary phase boost (usually 1/5 of the crossover value gives good results).
- A pole situated at the capacitor ESR frequency (f_{z1}) or at one-half the switching frequency if the ESR value is too low. In this example, we placed it around 20 kHz.

The k factor placed a zero at 7 kHz and a pole at 8.7 kHz. As we have seen, spreading these poles and zeros apart (pushing the zero farther down the spectrum) will increase the phase boost, but the transient response might eventually suffer. Remember, the compensation zeros

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become the poles of your system in closed loop. To illustrate this, Fig. 7-29c depicts the compensated Bode plot with the following placement:

1. Compensation 1 places a zero at 7 kHz and a pole at 8.7 kHz.
2. Compensation 2 places a zero at 2 kHz and a pole at 20 kHz.

In both cases, the crossover frequency is 8 kHz, but compensation 1 gives a phase margin of 70° whereas compensation 2 increases it to 115°. The transient response in Fig. 7-29c speaks for itself; this is the slowest response. In conclusion, do not overcompensate the loop to obtain the largest phase margin. Keep it in the vicinity of 70° to 80° and always avoid going below 45° in the worst case. Of course, you also need to sweep all the parasitic parameters (ESR, for instance) and the operating conditions (input voltage, output load) to see how they affect the phase margin. Then, a compensation is required to remain stable in the worst case.

7.10.2 CCM Voltage Mode

By raising the primary inductance to 800 μH, we ensure the converter enters in CCM, as confirmed by Eq. (7-91). As we did before, we have selected a crossover frequency of 8 kHz. However, on a CCM buck-boost, boost, or flyback, what limits the bandwidth is the perfidious RHPZ. As we explained, this zero gives a boost in gain but stresses the phase rather than boosting it as a traditional left half-plane (LHP) zero would do. In other words, stabilizing the converter at a crossover frequency where the RHPZ starts to kick in represents a perilous, if not impossible, exercise. For this reason, it is advised to calculate the lowest RHPZ position and select 20 to 30% of it for the crossover frequency. In our example, let us run the exercise of assessing all pole and zero positions, as we did for the DCM case.

We first compute the duty cycle at a 200 V input voltage:

$$D = \frac{V_{out}}{V_{out} + NV_{in}} = \frac{19}{19 + 0.166 \times 200} = 0.36 \tag{7-101}$$

The right half-plane zero position is derived using the following equation:

$$f_{z2} = \frac{(1 - D)^2 R_{load}}{2\pi D L_p N^2} = \frac{(1 - 0.36)^2 \times 6}{6.28 \times 0.36 \times 800u \times 0.166^2} = 49.3\,\text{kHz} \tag{7-102}$$

In this particular case, 20% of this value is 10 kHz. We thus have a sufficient margin with the 8 kHz choice.

We know that the flyback converter operated in CCM peaks as any second-order converter would do. The double pole introduced by the resonance of L_s and C_{out} is placed at

$$f_{p2} = \frac{1 - D}{2\pi N \sqrt{L_p C_{out}}} = \frac{1 - 0.36}{6.28 \times 0.166 \times \sqrt{800u \times 2.2m}} = 462.8\,\text{Hz} \tag{7-103}$$

To have an idea how the phase will drop as we approach this point, the quality coefficient Q can also be calculated:

$$Q = \frac{(1 - D)R_{load}}{N}\sqrt{\frac{C_{out}}{L_p}} = \frac{(1 - 0.36) \times 6}{0.166} \times \sqrt{\frac{2.2m}{800u}} = 38.4 \text{ or } 31.6\,\text{dB} \tag{7-104}$$

However, given the damping brought by the diode dynamic resistance and the capacitor equivalent series resistor, the quality coefficient is reduced to 4 dB, as shown in Fig. 7-29b.

The output capacitor still brings a zero whose position is similar to its DCM counterpart as described by Eqs. (7-94) and (7-95). The dc gain of the control to output chain is obtained by applying the following formula:

$$G_0 = 20 \log_{10}\left[\frac{NV_{in}}{(1 - D)^2 V_{peak}}\right] = 20 \log_{10}\left[\frac{0.166 \times 200}{(1 - 0.37)^2 \times 2}\right] = 32.4\,\text{dB} \qquad (7\text{-}105)$$

The compensation of a CCM flyback converter operated in voltage mode requires a type 3 compensation network. The double pole present at the resonant frequency locally stresses the phase and requires the placement of a double zero right at the worst-case resonance. A possible placement could be as follows:

- One pole at this origin, giving a high dc gain, thus a low dc output impedance and a good dc input rejection.
- A double zero placed at the resonant frequency given by Eq. (7-103).
- A pole situated at the capacitor ESR frequency (f_{z1}) or at the RHPZ or at one-half the switching frequency. In our case, the RHPZ appears at 48 kHz, so placing a pole at one-half the switching frequency represents a possible choice.
- This third pole can be installed as the above definition explains. In this example, we will also place it at one-half the switching frequency.

Again, we can compare the results with the *k* factor, known to be less efficient in CCM. The *k* factor recommended to place the double zero around 3.7 kHz and a double pole at 18 kHz. It is thus very likely that the *k* factor proposal leads to a faster response given the higher position of the double zeros. In summary,

1. We have an 8 kHz crossover frequency.
2. Compensation 1 places a double zero at 3.7 kHz and a double pole at 18 kHz (*k* factor).
3. Compensation 2 places a double zero at the resonant frequency and a double pole at one-half the switching frequency.

Figure 7-30c illustrates the obtained compensated Bode plots, and the lower window shows the transient response. The *k* factor is faster, as we had already seen it in Chap. 3. However, look at the wide conditional stability area around 1 kHz. It is true that the gain margin in this zone is still about 20 dB, but some customers would not accept conditional zones at all. The placement of the double zero right at the resonant frequency gives a generous phase boost but unfortunately degrades the gain in the lower portion of the spectrum. If you now compare Figs. 7-30c and 7-29c, they offer very similar transient response despite different operating modes. The CCM with the second compensation option recovers slightly more slowly than its DCM counterpart, however.

In this example, we have used a type 3 compensation circuit based on a TL431. For flexibility purposes, we do not recommend using the TL431 in this type of configuration voltage-mode CCM. Because the LED series resistor plays a role in the gain and other pole-zero placement, it becomes difficult to combine the pole-zero positions and the right bias current when needed.

7.10.3 DCM Current Mode

The flyback operated in current mode is probably the most widely used converter. Thanks to its first-order behavior and its intrinsic cycle-by-cycle current protection, the converter lends itself very well to the design of rugged and easy-to-stabilize power supplies. The compensation is simple (first-order behavior in the low-frequency portion), and the converter naturally excels in

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input line rejection performance. As in voltage mode, the position of poles and zeros changes as the converter transitions from one mode to the other. This table summarizes their positions.

Current-Mode Control

	DCM	CCM
First-order pole	$\dfrac{1}{\pi R_{load} C_{out}}$	$\dfrac{\dfrac{D'^3}{\tau_L}\left(1 + 2\dfrac{S_e}{S_n}\right) + 1 + D}{2\pi R_{load} C_{out}}$
Second-order pole	$\dfrac{F_{sw}}{\pi}\left(\dfrac{1/D}{1 + \dfrac{NV_{in}}{V_{out}}}\right)^2$	—
Left half-plane zero	$\dfrac{1}{2\pi R_{ESR} C_{out}}$	$\dfrac{1}{2\pi R_{ESR} C_{out}}$
Right half-plane zero	$\dfrac{R_{load}}{2\pi N \dfrac{V_{out}}{V_{in}}\left(1 + \dfrac{V_{out}}{NV_{in}}\right) L_p}$	$\dfrac{(1 - D)^2 R_{load}}{2\pi D L_p N^2}$
V_{out}/V_{in} dc gain	—	$MN\dfrac{\dfrac{D'^2}{\tau_L}\left(M - 2\dfrac{S_e}{S_n}\right) - M}{\dfrac{D'^2}{\tau_L}\left(1 + 2\dfrac{S_e}{S_n}\right) + 2M + 1}$
V_{out}/V_{error} dc gain	$V_{in}\sqrt{\dfrac{R_{load} F_{sw}}{2L_p}}\dfrac{1}{S_e + S_n}$	$\dfrac{R_{load}}{R_i N}\dfrac{1}{\dfrac{D'^2}{\tau_L}\left(1 + 2\dfrac{S_e}{S_n}\right) + 2M + 1}$
Duty cycle D	$\dfrac{V_{out}}{V_{in}}\sqrt{\dfrac{2L_p F_{sw}}{R_{load}}}$	$\dfrac{V_{out}}{V_{out} + NV_{in}}$

where D = duty cycle
F_{sw} = switching frequency
R_{ESR} = output capacitor equivalent series resistance
$M = \dfrac{V_{out}}{NV_{in}}$ = conversion ratio
L_p = primary inductance
R_{load} = output load
$N = \dfrac{N_s}{N_p}$ = transformer turns ratio
$\tau_L = \dfrac{2L_p N^2}{R_{load} T_{sw}}$
$S_n = \dfrac{V_{in}}{L_p} R_{sense}$ = on-time slope, V/s
S_e = external compensation ramp slope, V/s
R_i = primary sense resistor

Our DCM power supply features the same values as above, except that it now operates in current mode with a sense resistor R_i of 300 mΩ. The low-frequency poles and zeros occupy

the positions of the DCM voltage-mode converter. Equations (7-92) to (7-99) are thus still valid. The dc gain, however, changes and obeys the following equation:

$$G_0 = 20\log_{10}\left[V_{in}\sqrt{\frac{R_{load}F_{sw}}{2L_p}}\frac{1}{S_e + S_n}\right]$$

$$= 20\log_{10}\left[200\sqrt{\frac{6\times 65k}{2\times 450u}}\times\frac{1}{0+\frac{200}{450u}\times 0.3}\right] = 30\,\text{dB} \qquad (7\text{-}106)$$

Again, the control-to-output curve looks like that of the voltage-mode DCM which requires a type 1 or type 2 amplifier, depending on the ESR help around the crossover frequency. The gain difference between Eq. 7-106 and the simulated gain relates to the internal structure of the current-mode controller. Figure 7-31a details the internal structure of a UC384X where

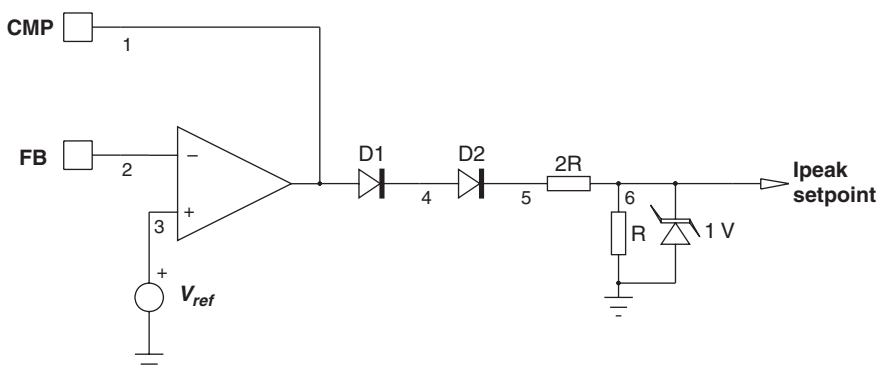

FIGURE 7-31a The internal UC384X structure includes a 1 V clamp and a divider by 3.

a divider by 3 exists after two diodes in series. This divider brings a –9.5 dB insertion loss seen on Fig. 7-30b. In an NCP120X series member, the feedback undergoes a division by 4. The two series diodes make sure the set point falls to zero, even if the op amp low excursion does not reach ground. It also ensures the same null set point when an optocoupler directly connects to the CMP pin and exhibits a high saturation voltage (see Fig. 7-31b). The compensation follows the DCM voltage-mode guidelines. We have placed the compensation zero and pole at a similar location, respectively, 2 kHz and 20 kHz. Figure 7-32 shows the compensated Bode plot with its transient response: it is difficult to distinguish it from the voltage-mode response.

7.10.4 CCM Current Mode

In current-mode CCM, the right half-plane zero really hampers the available bandwidth as in CCM voltage mode. Equation (7-102) remains valid with an RHPZ located around 50 kHz. However, this time, there is no need to place a double zero thanks to the lack of resonant frequency.

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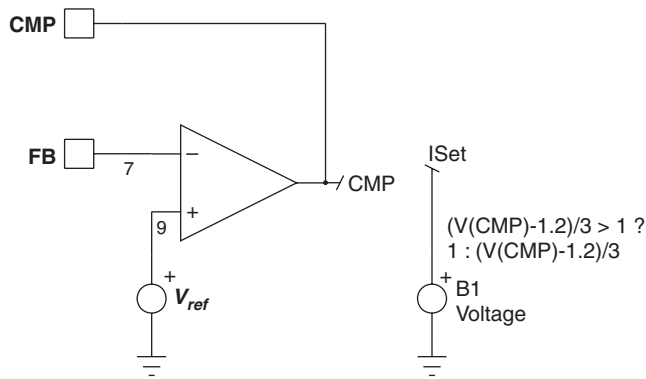

FIGURE 7-31b A possible SPICE implementation of the UC384X controller feedback section.

The main pole, whose position moves in relation to the compensation ramp, occurs at the following position:

$$f_{p1} = \frac{\frac{D'^3}{\tau_L}\left(1 + 2\frac{S_e}{S_n}\right) + 1 + D}{2\pi R_{load} C_{out}} \tag{7-107}$$

In this expression, the duty cycle is defined by Eq. (7-101) and is limited to 36%. Because of the CCM operation and the presence of subharmonic poles, it might be necessary to inject ramp

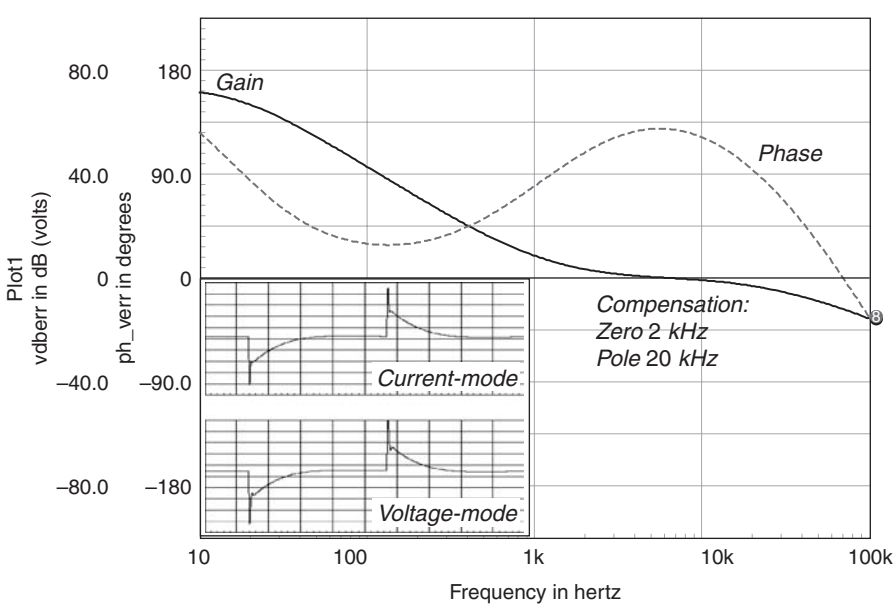

FIGURE 7-32 The transient response of the DCM current-mode converter, same scale.

compensation. A simple operation lets us assess the quality coefficient of the double poles located at one-half the switching frequency. If we go back to Chap. 2, without compensation ramp ($S_e = 0$) we have

$$Q = \frac{1}{\pi\left(D'\frac{S_e}{S_n} + \frac{1}{2} - D\right)} = \frac{1}{3.14 \times (0.5 - 0.36)} = 2.3 \tag{7-108}$$

This result suggests that we damp the subharmonic poles to bring the quality coefficient below 1. Extracting the S_e parameter leads to

$$S_e = \frac{S_n}{D'}\left(\frac{1}{\pi} - 0.5 + D\right) = \frac{V_{in}R_i}{L_pD'}\left(\frac{1}{\pi} - 0.5 + D\right)$$

$$= \frac{200 \times 0.3}{850u \times (1 - 0.36)}\left(\frac{1}{3.14} - 0.5 + 0.36\right) = 19.6\,\text{kV/s} \tag{7-109}$$

How much shall we compensate the converter? Is the suggested 19 kV/s slope enough? Well, sweeping the ramp amplitude reveals various responses, as Fig. 7-33 shows. Without any compensation at all, we can see the peaking above the 0 dB axis. This peaking is going to hurt the gain margin after compensation if it is not properly cured. When we add the external ramp, the peaking lowers and the situation improves when injecting more ramp. However, keep in mind that overcompensating the converter is not a panacea either, as its bevavior would approach that of a voltage mode.

A 19 kV/s slope means a ramp starting from 0 at the beginning of the on time and reaching 285 mV after 15 μs. We will see how to design such ramp in the next examples. In our model, we just set S_e to 19 kV and the compensation is done. Figure 7-34 gathers the compensated small-signal Bode plot and the step response it engenders. The compensation was similar to

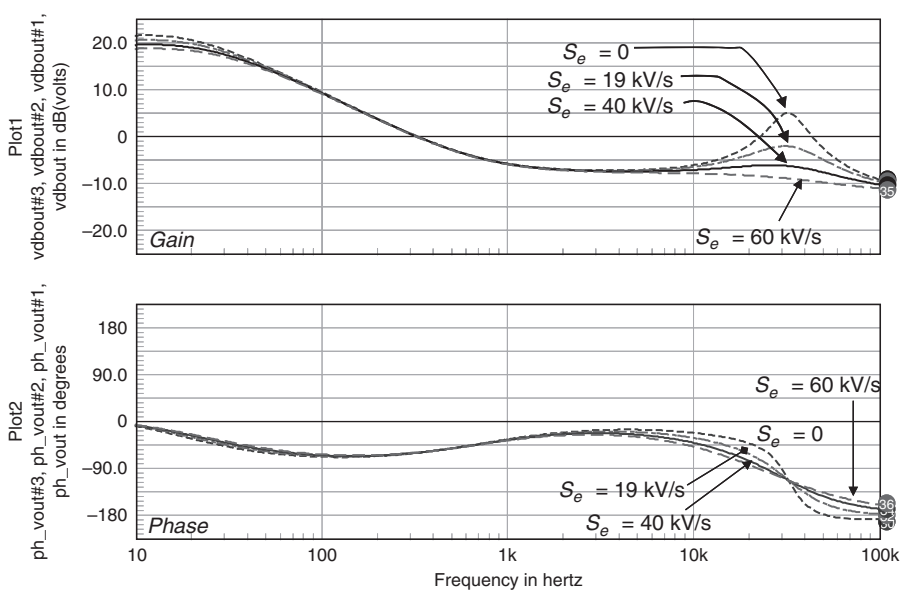

FIGURE 7-33 Effects of the ramp compensation on the CCM current-mode flyback.

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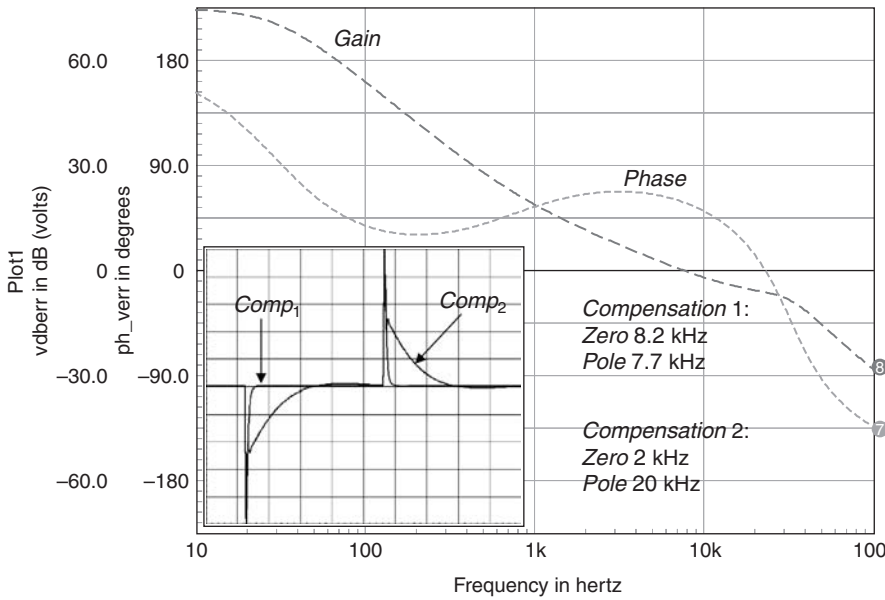

FIGURE 7-34 The CCM compensated flyback in current mode delivers almost the same transient response as that of the DCM version.

that of the DCM current-mode converter: a zero at 2 kHz and a pole placed at 20 kHz (compensation 2). Despite CCM, the step response is very close to that of the DCM version. The lack of double zero in the low-frequency spectrum clearly works in our favor. Compensation 1 is recommended by the *k* factor and places a zero and a pole at a similar location, actually canceling each other. The circuit becomes a type 1 compensator, simply placing a pole at the origin. The compensated result is the displayed Bode plot in the Fig. 7-34.

Further to these small-signal descriptions, let us summarize our observations:

- A CCM flyback converter requires a larger primary inductor compared to its DCM counterpart.
- CCM flyback converters operating in voltage mode or in current mode are subject to the same RHP zero which limits the available crossover frequency.
- A CCM voltage-mode flyback converter requires the placement of a double zero to fight the phase lag at the resonating point. The transient response is clearly affected.
- A voltage-mode CCM flyback can be stabilized using a type 3 compensation amplifier. But the classical TL431 configuration does not lend itself very well to its implementation.
- On the contrary, compensating a CCM current-mode flyback via a type 2 amplifier is an easy step.
- A DCM compensated voltage-mode flyback converter is likely to oscillate when entering CCM. Provided the RHP zero is far enough from the crossover frequency, the DCM current-mode flyback would be less sensitive to this mode transition.
- A CCM current-mode flyback converter whose duty cycle approaches 50% (or exceeds it) requires ramp compensation to avoid subharmonic oscillations. However, in certain cases, ramp compensation becomes mandatory at duty cycles as low as 35%: always compute the quality coefficient of the double to check for the necessity of compensation.

7.11 PRACTICAL CONSIDERATIONS ABOUT THE FLYBACK

Before showing how to design some flybacks converters, we need to cover a few other practical aspects, such as the start-up or the auxiliary supply of the controller.

7.11.1 Start-Up of the Controller

When you plug the power supply into the wall outlet, the bulk capacitor immediately charges to the peak of the input voltage (producing the so-called in-rush current). Since the controller is being operated from a low voltage (usually below 20 Vdc), it cannot be directly powered from the bulk, and a start-up circuitry must be installed. Figure 7-35 shows various solutions you could find on the market.

In Fig. 7-35, some initial energy is provided by the V_{cc} capacitor, charged by a start-up resistor. At power-on, when the capacitor is fully discharged, the controller consumption is zero and does not deliver any driving pulses. As V_{cc} increases, the consumed current remains below a guaranteed limit until the voltage on the capacitor reaches a certain level. This level, often called V_{CCon} or $UVLO_{high}$ (under voltage lockout) depending on the manufacturer, fixes the point at which the controller starts to deliver pulses to the power MOSFET. At this point, the consumption suddenly increases, and the capacitor depletes since it is the only energy reservoir. Its voltage thus falls until an external voltage source, the so-called auxiliary winding, takes over and self-supplies the controller. The capacitor stored energy must thus be calculated to feed the controller long enough that the auxiliary circuit takes over in time. If the capacitor fails to maintain V_{cc} high enough (because the capacitor has been set too small or the auxiliary voltage does not come), its voltage drops to a level called $UVLO_{low}$ or $V_{CC(min)}$. At this point, the controller considers its supply voltage too low and stops all operations. This safety level ensures that (1) the MOSFET receives pulses of sufficient amplitude to guarantee a good $R_{DS(on)}$ and (2) the controller internal logic operates under reliable conditions. When reaching the $UVLO_{low}$ level, the controller goes back to its original low consumption mode and, thanks to the start-up resistor, makes another restart attempt. If no auxiliary voltage ever comes, e.g., there is a broken diode or an output short-circuit, the power supply enters hiccup mode (or auto restart) where it pulses for a few milliseconds (the time the capacitor drops from $UVLO_{high}$ to $UVLO_{low}$), waits until the capacitor refuels, makes a new attempt, and so on. During the start-up event, the peak current is usually limited to a maximum value, very often 1 V developed across the sense resistor, and a brief noise can be heard in the transformer every time the controller pulses. This noise comes from the mechanical resonance of the magnetic material and the wire excitation induced by the high current pulses (remember the Laplace law).

Figure 7-36a depicts an oscilloscope shot of a power supply start-up sequence. You can see the voltage going up until it reaches the controller operating level. At this point, the voltage goes down as expected until the auxiliary voltage takes over. Figure 7-36b shows the same curve in

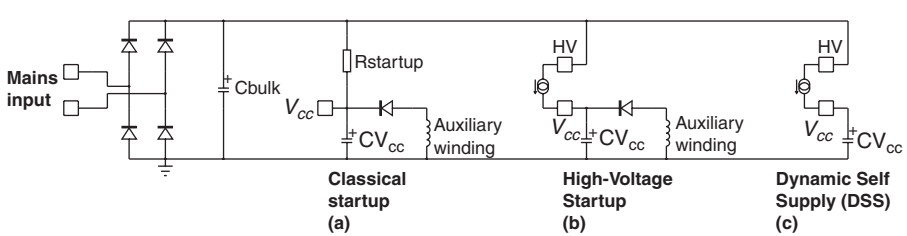

FIGURE 7-35 Several solutions are available to start up the power supply.

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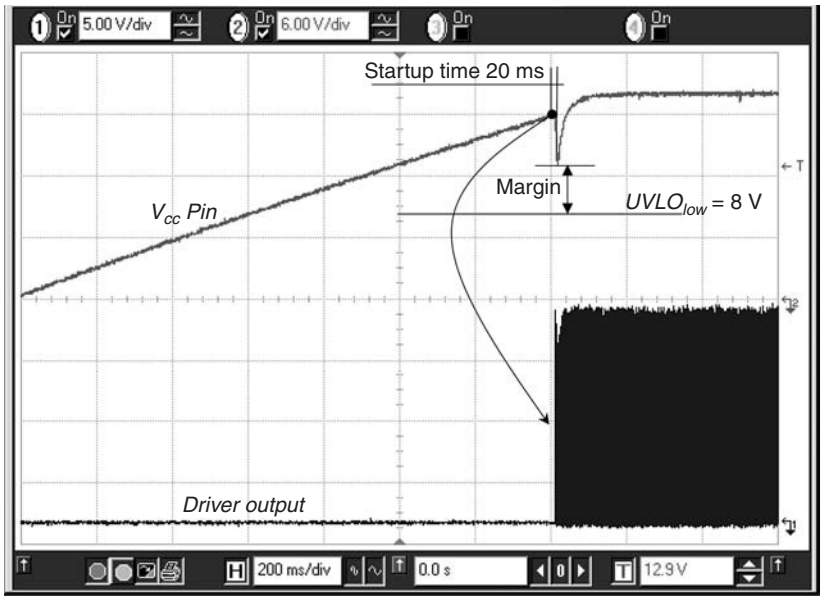

FIGURE 7-36a Start-up sequence where the auxiliary winding takes over in roughly 20 ms.

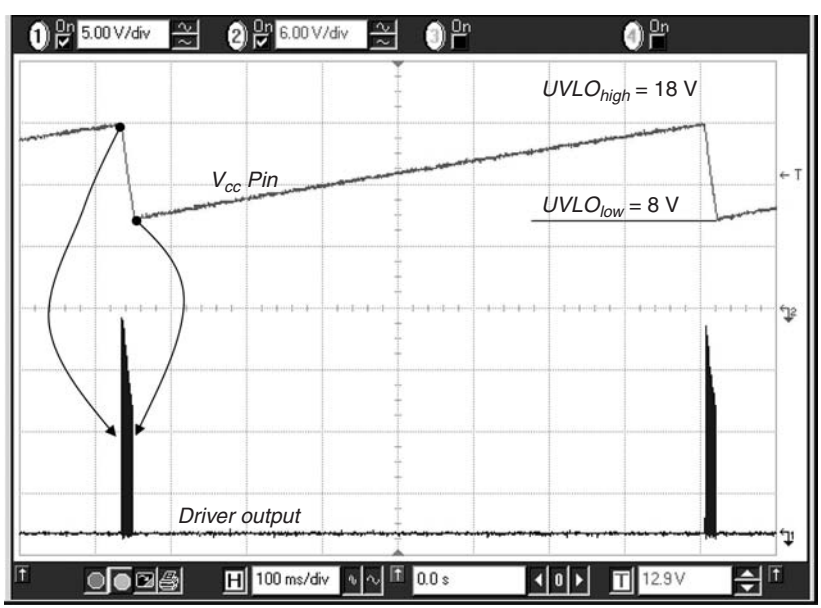

FIGURE 7-36b Same power supply where the auxiliary winding is lost at start-up.

the absence of auxiliary voltage: the controller cannot maintain its own V_{cc} and the hiccup takes place. The worst-case start-up conditions occur, as you can imagine, at the lowest input source (where the ripple on the bulk capacitor is maximum) and the highest load. A sufficient margin must exist between the point where the auxiliary winding takes over and the $UVLO_{low}$ point.

7.11.2 Start-Up Resistor Design Example

Figure 7-37 describes the current split between the start-up resistor and the V_{cc} capacitor at different events. Figure 7-37d details the associated timing diagrams.

1. At the beginning of t_1, the user plugs in the power supply: the current delivered by the start-up resistor charges the capacitor and supplies the controller. The chip is supposed to be in a complete off mode and draws a current I_{CC} equal to I_2. Actually, an internal comparator and a reference voltage are alive and observe the V_{cc} pin; hence, there is some current flowing in the chip. This current, depending on the technology, can range from 1 mA, for a UC384X bipolar controller, to a few hundred microamperes for a recent CMOS-based circuit. Always look for the maximum start-up current given in the data sheet and ignore the typical value. Make sure you have both extreme operating temperatures covered as well. (Flee these 25 °C typical values only!) Let us stick to 1 mA in this example and consider this value constant as V_{cc} elevates.

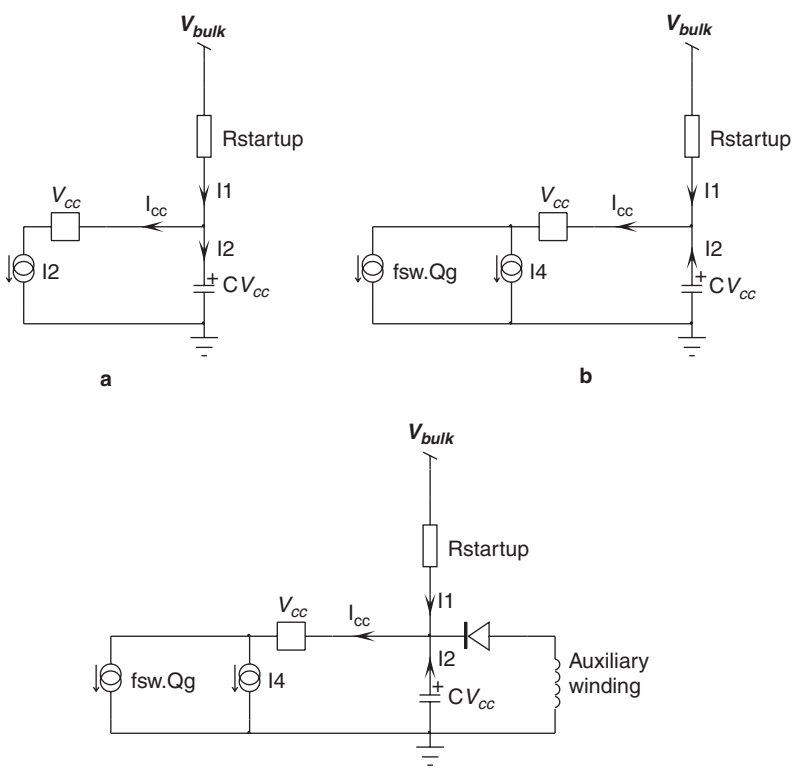

FIGURE 7-37 The three states the start-up sequence is made of.

SIMULATIONS AND PRACTICAL DESIGNS OF FLYBACK CONVERTERS

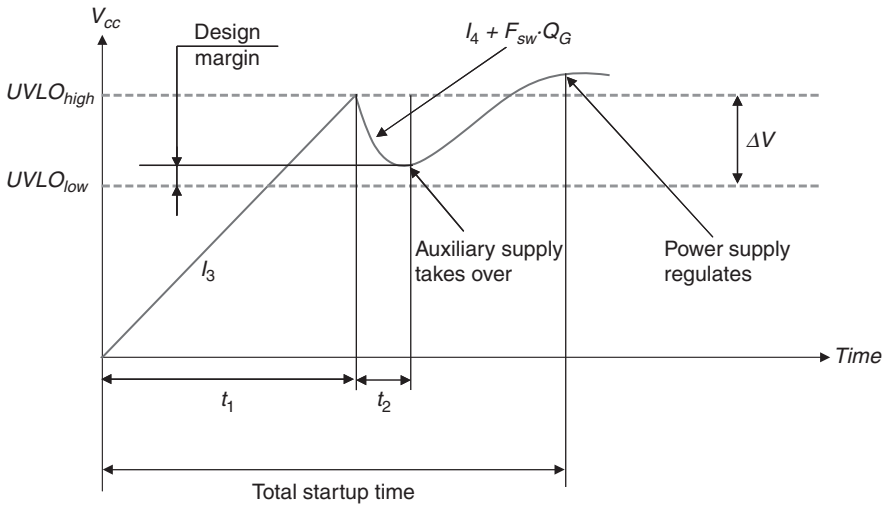

FIGURE 7-37d Timing diagram of a start-up sequence.

2. When the voltage on the V_{cc} capacitor reaches $UVLO_{high}$, the controller wakes up all its internal circuitry (the bandgap, bias currents ...) and starts to deliver driving pulses: t_2 begins. The consumption increases to a current I_4, made of the chip natural consumption plus the current drawn by the MOSFET driving pulses (neglecting the driver switching losses):

$$I_{CC} = I_4 + Q_G F_{sw} \tag{7-110}$$

where:

I_4 is the consumption current once the controller operates.
Q_G represents the maximum MOSFET gate charge (in nC).
F_{sw} is the controller switching frequency.

For a UC34X, I_4 is pretty high and goes up to 17 mA! For the sake of comparison, a NCP1200 from ON Semiconductor will only consume 1 mA at turn-on .... The parameter Q_G depends on your MOSFET type. Let us assume Q_G equals 35 nC which roughly corresponds to a 6 A/600 V MOSFET. Presuming a switching frequency of 100 kHz, the total current drawn by the controller during t_2 is simply:

$$I_{CC} = I_4 + Q_G F_{sw} = 17m + 35n \times 100k = 20.5\,\text{mA} \tag{7-111}$$

3. During this t_2 time, neglecting the start-up current brought by $R_{start\text{-}up}$, the V_{cc} capacitor supplies the total controller current on its own (I_2 now reversed on Fig. 7-37b). If the capacitor is too small, the chip low operating limit $UVLO_{low}$ will precociously be touched and the power supply will fail to start-up in one clean shot. It may then start through several attempts or not start at all. Thus, what matters now is the time t_2 taken by the auxiliary winding to take over and self-supply the controller. Experience shows that a duration of 5 ms is a reasonable number to start with. This fixes the minimum value of the V_{cc} capacitor, involving Eq. 7-111, the time t_2, and the maximum voltage swing (V over the capacitor (6 V for the UC384X):

$$C_{Vcc} \geq \frac{I_{CC} t_2}{\Delta V} \geq \frac{20.5m \times 5m}{6} = 17\,\mu\text{F} \tag{7-112}$$

Given the unavoidable dispersion on the component value, select a 33 μF capacitor whose voltage rating depends on your auxiliary winding excursion.

4. Next step, the start-up time. Let us assume the following specifications for our power supply:

   $V_{in,min}$ = 85 Vrms, $V_{bulk,min}$ = 120 Vdc (no ripple before the power supply starts-up)
   $V_{in,max}$ = 265 Vrms, $V_{bulk,max}$ = 375 Vdc
   F_{sw} = 100 kHz
   Maximum start-up time = 2.5 s

   If we consider t_1 as being the major contributor to the total start-up time, then we can calculate the necessary current to reach the $UVLO_{high}$ in less than 2.4 s, including a 100 ms safety margin:

$$IC_{V_{cc}} \geq \frac{UVLO_{high}C_{V_{cc}}}{2.4} = \frac{17 \times 33u}{2.4} = 234\,\mu A \tag{7-113}$$

   In Eq. 7-113, take the highest $UVLO_{high}$ from the data sheet again to make sure all distribution cases are covered. From this equation, we need to add the controller fixed start-up current I_3 of 1 mA. Hence, the total current the start-up resistor must deliver reaches 1.3 mA. Knowing a minimum input line of 85 Vrms, the resistor is simply defined by:

$$R_{startup} = \frac{V_{bulk,min} - UVLO_{high}}{1.3m} = \frac{120 - 17}{1.3m} = 79.3\,k\Omega \tag{7-114}$$

   Select a 82 kΩ resistor. Unfortunately, once the supply has started, the controller no longer needs the resistor. It just wastes power in heat and contributes to significantly degrade the efficiency in light load conditions. In this case, the resistor dissipates at high line (neglecting the bulk ripple):

$$P_{R_{startup}} = \frac{(V_{bulk,max} - V_{aux})^2}{R_{startup}} = \frac{(375 - 15)^2}{82k} = 1.6\,W \tag{7-115}$$

   You might need to put three 27 kΩ/1 W resistors in series to dissipate the heat and sustain the voltage.

5. Assemble the power supply with the calculated element values and connect a probe to the controller V_{cc} pin. Supply the system with the lowest ac input (85 Vrms here) and load the converter with the maximum current per your specification. Now observe the start-up sequence; you should see something close to what Fig. 7-37d illustrates. Make sure you have enough margin at the point where the auxiliary voltage takes off and the $UVLO_{low}$ level.

1.6 W represents quite a bit of power to dissipate. Furthermore, placed too close to electrolytic capacitors, they might locally increase their operating temperature and reduce their lifetime. Is there a way to reduce the consumption or get rid of this start-up resistor? The answer is yes on both cases!

7.11.3 Half-Wave Connection

To reduce the start-up resistor consumption, we can change its upper terminal connection from the bulk capacitor to the diode bridge input. Figure 7-38 shows you the way:

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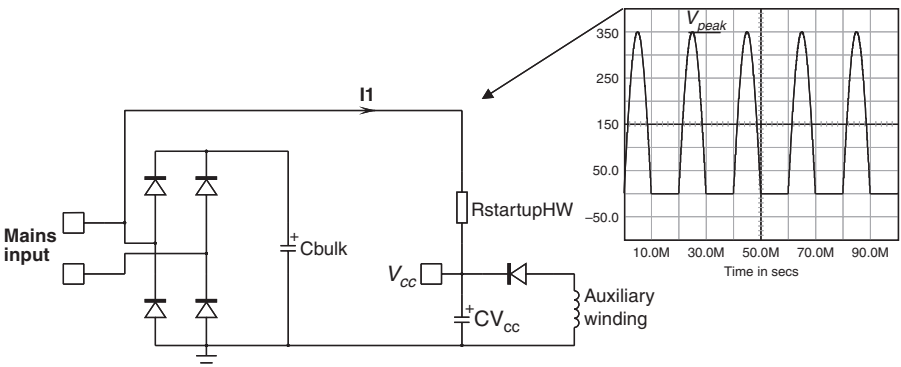

FIGURE 7-38 Connecting the start-up resistor to the diode bridge input reduces the power dissipation.

Thanks to the bridge, a half-wave rectified waveform appears on the upper terminal of $R_{start\text{-}upHW}$. The average voltage seen by the resistor:

$$V_{R_{startupHW},avg} = \frac{V_{act,peak}}{\pi} - V_{cc} \tag{7-116}$$

where $V_{ac,peak}$ represents the peak of the ac input voltage, $265\sqrt{2}$ at high line.

The charging current I_1 at V_{cc} close to $UVLO_{high}$ then becomes:

$$I_1 = \frac{\frac{V_{ac,peak}}{\pi} - UVLO_{high}}{R_{startupHW}} \tag{7-117}$$

Equation 7-114, which corresponds to a traditional bulk connection, can be rewritten highlighting the charging current definition:

$$I_1 = \frac{V_{ac,peak} - UVLO_{high}}{R_{startup}} \tag{7-118}$$

To obtain the same charging current via Fig. 7-38 suggestion, let us equate expressions 7-117 and 7-118 and extract the relationship between $R_{start\text{-}upHW}$ and $R_{start\text{-}up}$. For the sake of simplicity, the peak voltage being much larger than the V_{cc}, we will neglect the *UVLO* term present in both equations. Calculation thus gives us:

$$R_{startupHW} = \frac{R_{startup}}{\pi} \tag{7-119}$$

Following our study, we shall now evaluate the power dissipated in $R_{start\text{-}upHW}$ and see how much power the half-wave connection helps us to save. Again, we need to evaluate the power in both cases (half-wave and bulk connection) and compare the results as we did in the above lines. When the resistor connects directly to the bulk, again neglecting the V_{cc} term and the bulk ripple, the resistor dissipates:

$$P_{R_{startup}} = \frac{V_{ac,peak}^2}{R_{startup}} \tag{7-120}$$

When the resistor now connects to the half-wave signal, the resistor undergoes sinusoidal signals. Therefore:

$$P_{R_{startpHW}} = \frac{1}{T}\int_0^{T/2} I_{R_{startupHW}}(t) \cdot V_{R_{startupHW}}(t) \cdot dt = \frac{1}{T}\int_0^{T/2} \frac{V_{ac,peak}}{R_{startupHW}} \sin \omega t \cdot V_{ac,peak} \sin \omega t \cdot dt \quad (7\text{-}121)$$

Rearranging Eq. 7-121 lets us solve the integral quicker since the second term is nothing else than the rms input voltage squared, but defined over one-half the period only:

$$P_{R_{startpHW}} = \frac{1}{R_{startupHW}} \frac{1}{T}\int_0^{T/2} (V_{ac,peak} \sin \omega t)^2 \cdot dt = \frac{1}{R_{startupHW}} \frac{(V_{ac,rms})^2}{2} \quad (7\text{-}122)$$

Introducing the peak value in Eq. 7-123 definition, we finally have:

$$P_{R_{startpHW}} = \frac{1}{R_{startupHW}} \frac{\left(\frac{V_{ac,peak}}{\sqrt{2}}\right)^2}{2} = \frac{{V_{ac,peak}}^2}{4R_{startupHW}} \quad (7\text{-}123)$$

Now, it is interesting to compare the relationship between both dissipation budgets (half-wave and bulk connection) by simply dividing Eq. 7-120 by Eq. 7-123:

$$\frac{P_{R_{startup}}}{P_{R_{startupHW}}} = \frac{(V_{ac,peak})^2}{R_{startup}} \frac{4R_{startupHW}}{(V_{ac,peak})^2} = \frac{4R_{startupHW}}{R_{startup}} \quad (7\text{-}124)$$

Now using Eq. 7-119, the relationship becomes:

$$\frac{P_{R_{startup}}}{P_{R_{startupHW}}} = \frac{4R_{startup}}{\pi R_{startup}} = \frac{4}{\pi} \approx 1.27 \quad (7\text{-}125)$$

As a conclusion, if we apply the half-wave connection to our original bulk-connected start-up scheme, we gain 21% in power dissipation. Let us apply this result to our design example:

$$R_{startupHW} = \frac{R_{startup}}{\pi} = \frac{82k}{\pi} = 26\,\text{k}\Omega \quad (7\text{-}126a)$$

from Eq. 7-123:

$$P_{R_{startpHW}} = \frac{{V_{ac,peak}}^2}{4R_{startupHW}} = \frac{(265 \times \sqrt{2})^2}{4 \times 26k} = 1.35\,\text{W} \quad (7\text{-}126b)$$

In that case, two 13 kΩ/1 W resistors in series would be ok, compared to three 27 kΩ/1W in the direct connection case.

Well, we certainly reduced the dissipation lost in heat, but the best would be to get rid of it.

7.11.4 Good Riddance, Start-up Resistor!

Figure 7-39 depicts a solution involving either a bipolar or a MOSFET in an active current source. Actually, the transistor acts as a ballast whose current is limited by the same resistor calculated through Eq. 7-114. When the auxiliary voltage builds up, it simply reverse biases the transistor which disconnects the start-up resistor. D_1 in the bipolar option prevents from an

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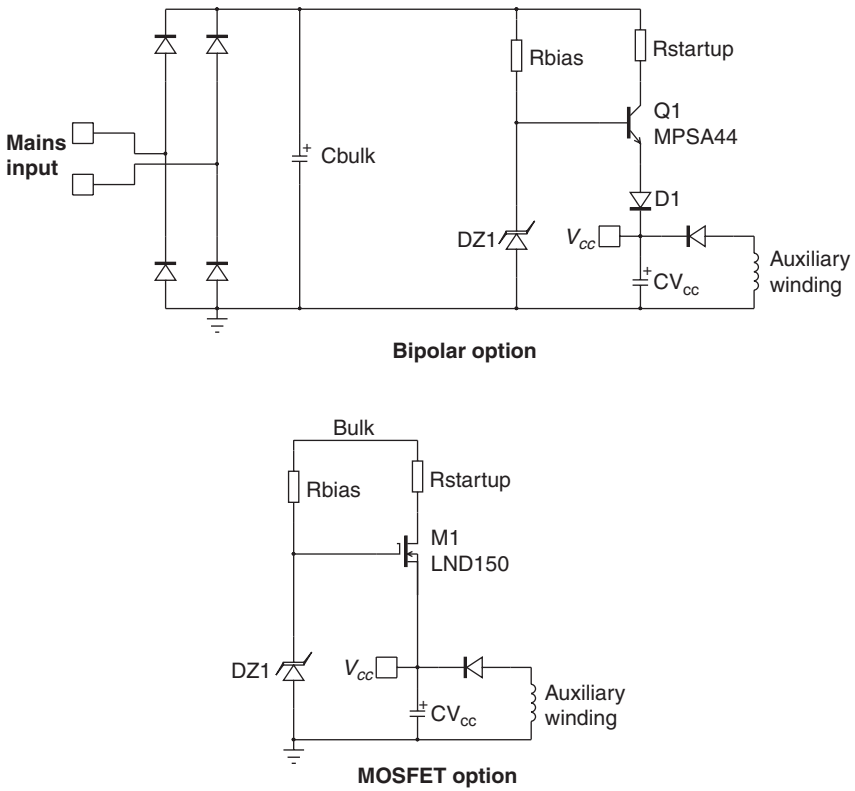

FIGURE 7-39 A simple ballast based on a high-voltage bipolar or MOSFET cancels the power dissipated by the start-up resistor.

excessive base-emitter reverse voltage. It can be omitted for the MOSFET option. In both cases, the zener voltage is selected to be at least 2 V above the maximum start-up level $UVLO_{high}$ of the concerned PWM controller: 1 V for the V_{be} drop at low temperatures and 1 V for the margin. With an UC384X featuring a 17 V start-up (UC3842/44), select a 20 V zener.

7.11.5 High-Voltage Current Source

Some semiconductor manufacturers have introduced a technology capable of a direct connection to the bulk. Known as the *very high voltage integrated circuit* (VHVIC) at ON Semiconductor, the process accepts up to 700 V and, as such, is well suited to build high-voltage current sources. Figure 7-40 shows the internal high-level circuitry of a chip including such approach (a member of the NCP120X series for instance).

At power-up, the reference level equals the $UVLO_{high}$ level, e.g. 12 V, and the source delivers a certain current (usually a few mA). When the V_{cc} voltage reaches the upper level, the comparator senses it and turns the current source off. As in the start-up resistor case, the capacitor stays on its own to supply the controller. The auxiliary winding is then supposed to take over before reaching the second level, $UVLO_{low}$. If not, the current source turns *on* and *off* at a pace imposed by the V_{cc} capacitor: this is hiccup mode.

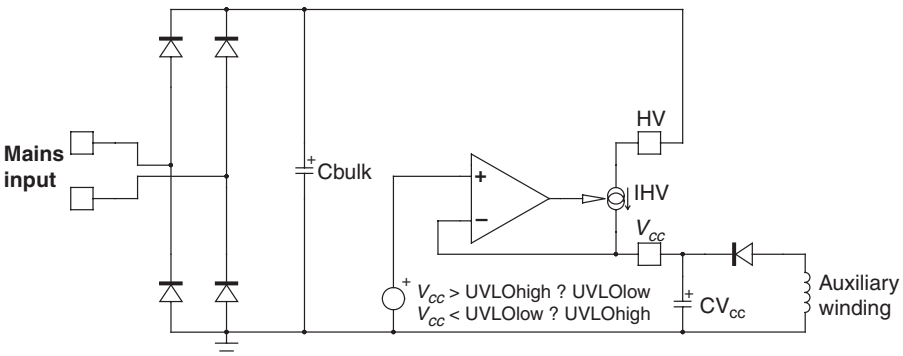

FIGURE 7-40 Thanks to a proprietary technology, the NCP120X circuits can directly connect to the bulk capacitor and saves some dissipated power.

When both *UVLO* levels are selected to be close to each others, let us say 12 V and 10 V, the start-up current source turns into a dynamic self-supply (DSS), delivering an average level of 11 V. You can thus forget the auxiliary winding! If you connect a probe to the V_{cc} pin of a NCP1200 or NCP1216, you might observe a signal as on Fig. 7-41. The HV pin is pulsating from the nominal current source value (here 4 mA) to almost zero when the source is off (the leakage lies around 30-40 μA). The regulation type of the DSS is hysteretic. In other words, the on-time duration will automatically adjust depending on the consumed current by the controller. If the controller consumes 2 mA and the source peak is 4 mA, the duty cycle will be established to 50%. The DSS type of a controller self-supply suits low-power circuits. For instance, a NCP1200 driving a 2 A MOSFET. Remember that Eq. 7-110 still holds and the

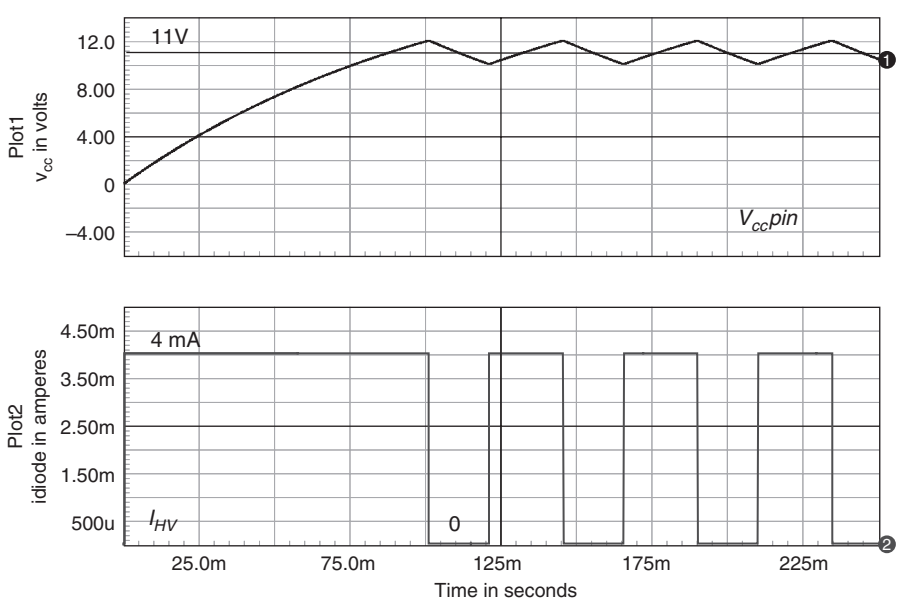

FIGURE 7-41 A typical dynamic self-supply operation from an NCP1216 controller.

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operating frequency associated to the MOSFET Q_G will quickly limit the operations by either exceeding the DSS capabilities or inducing too much heat on the die. This average power dissipation limit constrains the DSS usage to driving low Q_G MOSFETs. If we assume a 15 nC Q_G driven at a 65 kHz switching frequency, a 1 mA controller consumption, then the total DSS dissipated power reaches:

$$P_{DSS} = I_{CC}V_{bulk,max} = (I_4 + Q_G F_{sw}) = (1m + 65k \times 15n) \times 375 = 740\,\text{mW} \qquad (7\text{-}127)$$

Given the DIP8 or DIP14 power dissipation capabilities (below 1 W with a large copper area around them), the DSS usage is naturally limited to the operation of low gate-charge MOSFETs.

7.11.6 The Auxiliary Winding

The auxiliary winding is an important part of the supply since it powers the controller after the start-up sequence. Figure 7-42a represents a typical arrangement where the start-up resistor appears. A small resistor like R_1 can sometimes be inserted to limit the effect of the leakage inductance. We will see the role it plays in protecting the converter against short-circuits but also how it can defeat the auxiliary supply in standby conditions.

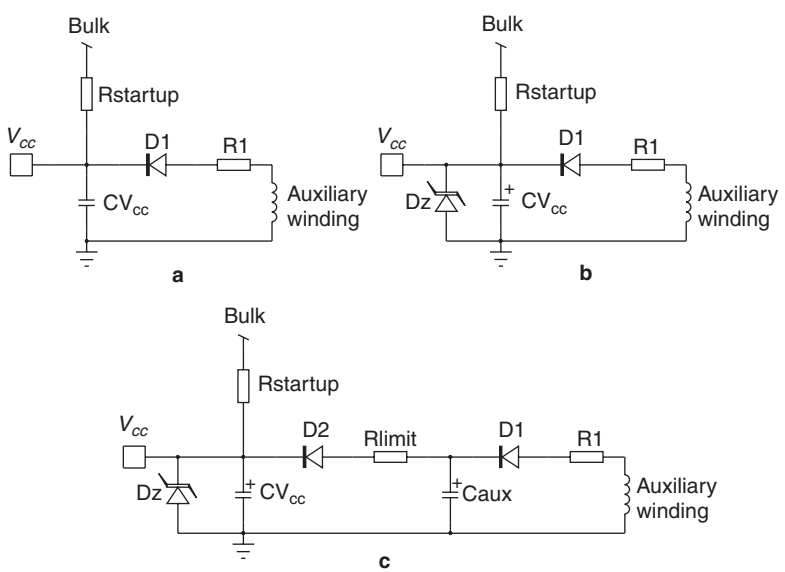

FIGURE 7-42 The auxiliary supply section.

Most of designers select a 1N4148 for the auxiliary circuit. Watch out for the reverse voltage seen by this diode:

$$\text{PIV} = \frac{N_{aux}}{N_p} V_{in} + V_{cc} \qquad (7\text{-}128)$$

where V_{cc} represents the dc cathode voltage after rectification. The 1N4148 accepts up to 100 V of repetitive reverse voltage. Other good candidates are the 1N4935 or the BAV20 which accept up to 200 V.

The voltage on the auxiliary winding depends on the controller and the selected MOSFET. Most of these devices do not accept V_{GS} levels above 20 V, though some recent components accept up to ±30 V. If you look at a MOSFET data sheet, you will see that the $R_{DS(on)}$ is specified at 10 V. If you increase the driving voltage to 15 V, you might gain a few percent in conduction losses, but not a lot. However, the power dissipated by the driver will increase. Also, the MOSFET lifetime depends on several parameters among which the driving voltage plays a significant role, so these are two good reasons to not overdrive the MOSFET! So what value then? Well, around 15 V looks like a good number, given that the effective driving voltage also depends on the sense resistor drop. Since the sense resistor appears in series with the source, when it develops 1 V, this voltage subtracts from the driving voltage.

If the driver includes a driving clamp, naturally limiting the gate-source voltage below 15 V, then there is no arm to let the driver supply swing to a higher level as long as it can sustain it (usually 20 Vdc for a CMOS-based process). On the other hand, if the auxiliary winding is subject to large variations, you might need a clamp. Figure 7-42b offers a simple means to clamp the voltage via the limiting resistor R_1. This works fine as long as you can increase the resistor to a point where the zener power dissipation stays under control. Problems start to arise in standby, where only a few pulses are present. During their presence, the capacitor C_{Vcc} must be fully replenished; otherwise the controller will stop operation. The amount of charge needed to refuel the capacitor depends on the peak current flowing in the capacitor. If you limit it via a series resistor, you store less charge and the voltage drops.

Increasing the V_{cc} capacitor remains a possible option, but it clearly hampers the start-up time. Figure 7-42c shows the so-called split supply solution where a big capacitor stores the necessary amount of charge in standby but stays isolated from the V_{cc} pin at start-up. The V_{cc} capacitor still obeys the design equations we have derived, but the auxiliary capacitor C_{aux} can be freely increased to sustain the standby: it will not delay the start-up time thanks to D_2. If necessary, the series resistor R_1 can be omitted in case of a long time difference between pulses in standby. Figure 7-43 shows how skip-cycle (see below what it means) slices a continuous PWM pattern into short pulses. In this case, the capacitor must keep the auxiliary level during 30 ms at least.

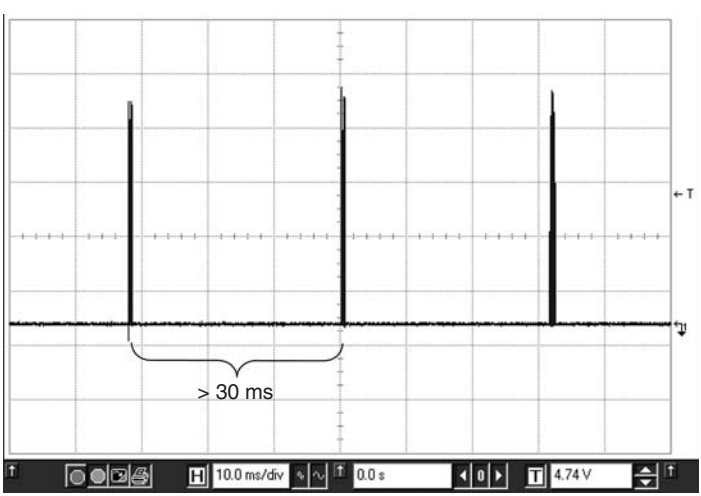

FIGURE 7-43 Typical drive pulses of a controller featuring skip-cycle. Please note the time distance between two bursts.

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7.11.7 Short-Circuit Protection

A true output short-circuit will be seen by the controller as a sudden loss of feedback information. Yes, during the start-up sequence, the system also runs open loop since no regulation has yet occurred. Circuits permanently monitoring the feedback loop have thus a means to detect this kind of event. On the market, however, some controllers do not include short-circuit protection. They rely on the collapse of the auxiliary winding when the output is short-circuited to enter a protective burst operation. Well, on paper, the idea looks great. Unfortunately, the perfidious leakage inductance sabotages the coupling between the power winding and the auxiliary winding. Figure 7-44 depicts a typical shot obtained on the anode of an auxiliary winding

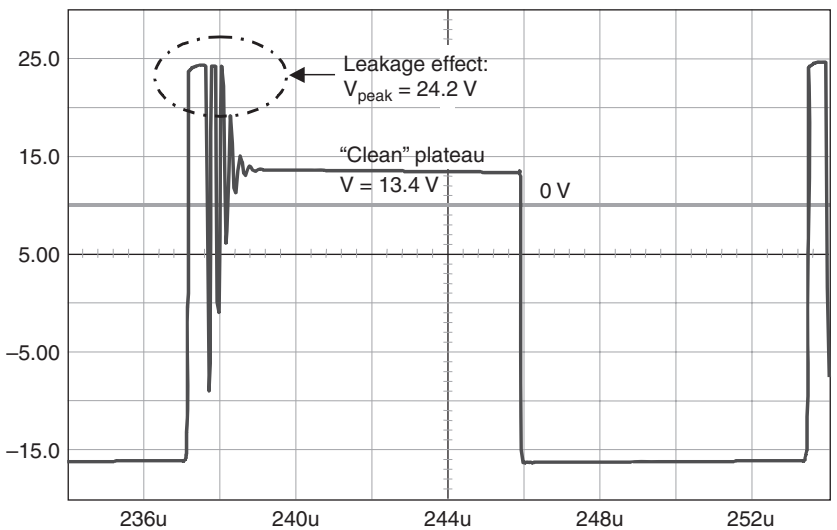

FIGURE 7-44 In this auxiliary voltage shot, the big spike confirms the presence of a large leakage inductance between the power and the auxiliary windings.

diode. As you can imagine, with the diode acting as a peak rectifier, the auxiliary voltage will go to 23.5 V whereas the plateau is at 12.7 V, considering a V_f of 0.7 V for the auxiliary diode. The plateau represents the output voltage, scaled down via the appropriate turns ratio between the power and auxiliary windings. Even if the plateau falls to a few volts because of the output short-circuit, the auxiliary supply will not collapse: the controller will keep driving the MOSFET, and the output current will probably destroy the output diode after a few minutes.

To avoid this problem, the best idea is to sense the feedback loop and make a decision regardless of the auxiliary conditions. For inexpensive controllers not implementing this method, you need to damp the ringing waveform by installing an inductor and its associated damper. A resistor can also help, but you will experience troubles in standby (V_{cc} capacitor refueling deficiency). Figure 7-45 shows how to install these passive elements on the auxiliary winding, just before the diode. (Typical values are shown here.) If you do not damp and install the inductor alone, depending on its value, it might ring so much that you could destroy the auxiliary diode by exceeding its maximum reverse biasing possibilities. It did happen. Figure 7-46a and b shows the auxiliary signals obtained without and with the *LC* filter.

This technique will help detect a real short-circuit on the secondary-side output. True overload detection is another story.

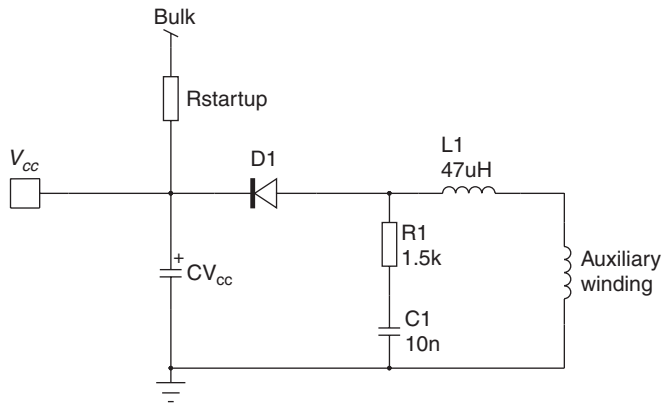

FIGURE 7-45 An *LC* network helps to tame the leakage spike at turn-off.

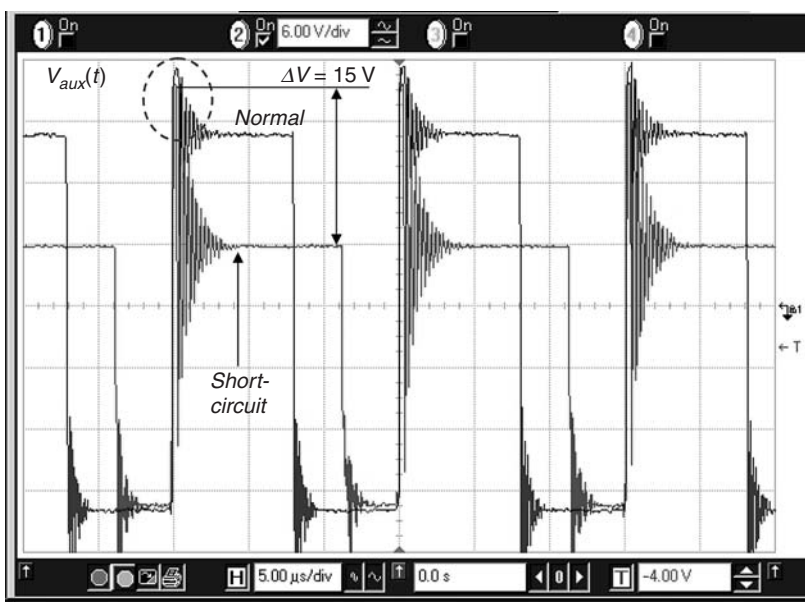

FIGURE 7-46a The auxiliary signal without a damping network (connection to the diode anode). Note the peak voltage amplitude; the auxiliary supply does not collapse.

7.11.8 Observing the Feedback Pin

An overload detection scheme could be implemented in different ways:

- The controller permanently observes the feedback signal, knowing that it should be within a certain range for regulation. If the signal escapes this range, there must be a problem: a flag is asserted.
- Rather than look at the feedback, the controller observes the current-sense pin and looks for overshoots beyond the maximum limit. If the current exceeds the limit, a flag is asserted.

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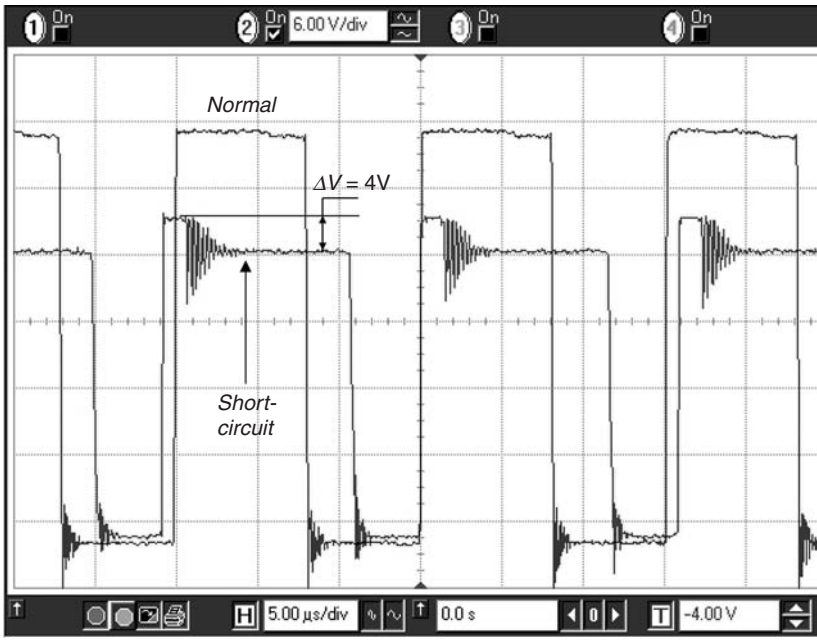

FIGURE 7-46b The auxiliary signal with a damping network (connection to the diode anode).

The first option is already implemented in a variety of controllers, such as the NCP1230 from ON Semiconductor. When the flag is asserted, a timer is started to delay the reaction to a fault. After all, a start-up sequence is also seen as a fault since no feedback signal appears prior to regulation. The timer is there to give a sufficient time for starting up. Typical values are in the range of 50 to 100 ms. Figure 7-47 describes a possible logic arrangement observing the feedback. To deliver the maximum peak current (1 V over the sense resistor), the feedback pin must be in the vicinity of 3 V. If it is above, close to the internal V_{dd} level, the PWM chip no longer has control over the converter. When this situation is detected by comparator CMP2, the switch *SW* opens and the external capacitor can charge. If the fault lasts long enough, the timer capacitor voltage will reach the V_{timer} reference level, confirming the presence of a fault. The controller can then react in different ways: go into autorecovery hiccup mode or simply totally latch off the circuit. If the fault lasts too short a time, the capacitor is reset and waits for another event. Some schemes do not fully reset the timer capacitor, but accumulate the events. This technique offers the best fault detection performance.

The precision of the overload detection depends on several factors, among which the TL431 bias plays a role. If you go back to Fig. 3-45, you can see how a badly biased TL431 degrades the squareness of the *I*/*V* characteristic. Hence, if you need a precise detection point, you should also pay attention to the secondary side circuitry.

In DSS-based controllers (NCP1200 or NCP1216), the error flag is tested as the V_{cc} voltage reaches 10 V. You thus have a natural short-circuit protection without the auxiliary winding problems.

7.11.9 Compensating the Propagation Delay

If you go back to Fig. 7-20, you understand how the primary slope affects the maximum current limit. This phenomenon will make your flyback converter deliver more power at high line

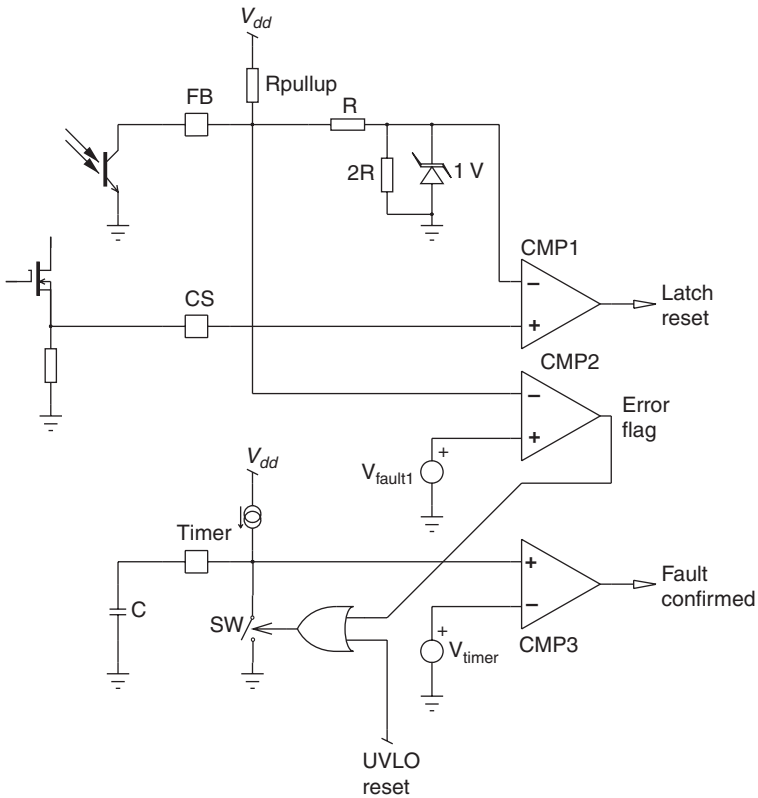

FIGURE 7-47 Monitoring the feedback brings excellent short-circuit/overload protection, regardless of the auxiliary V_{cc} state.

than at low line, explaining the difficulty to precisely react to an overload situation. To compensate this phenomenon, you need an *overpower protection* (OPP) circuit. The idea behind this solution is to offset the current-sense information to cheat the PWM controller. By increasing the voltage floor as the bulk level goes up, the current ramp reaches the maximum peak limit sooner. This, in effect, reduces the peak current excursion and clamps down the maximum available power (Fig. 7-48).

Figure 7-49a to c depicts most of the popular solutions found on the market. Figure 7-49a illustrates the simplest solution, but it clearly affects the current consumption on the bulk rail and requires high-voltage sensing. Figure 7-49b forces rotation of the diode in the auxiliary winding ground, and it can sometimes change the EMI signature. However, it does not burden the bulk rail with a permanent dc consumption. Figure 7-49c offers another option by creating an offset *ex nihilo* from a forward winding. As such, you create a voltage source solely dependent on the bulk rail.

The compensation level depends on various parameters such as the total propagation delay which also includes the driver turn-off capability: even if the controller reacts within a few hundred nanoseconds, if the driver cannot pull the gate down quickly enough, the total reaction time suffers and the current keeps increasing. A small PNP can help strengthen the pull-down action, as shown a few lines below.

The calculation of the OPP resistor requires a few lines of algebra, especially if we involve some ramp compensation. To help us in this task, Fig. 7-50 shows a simplified source arrangement

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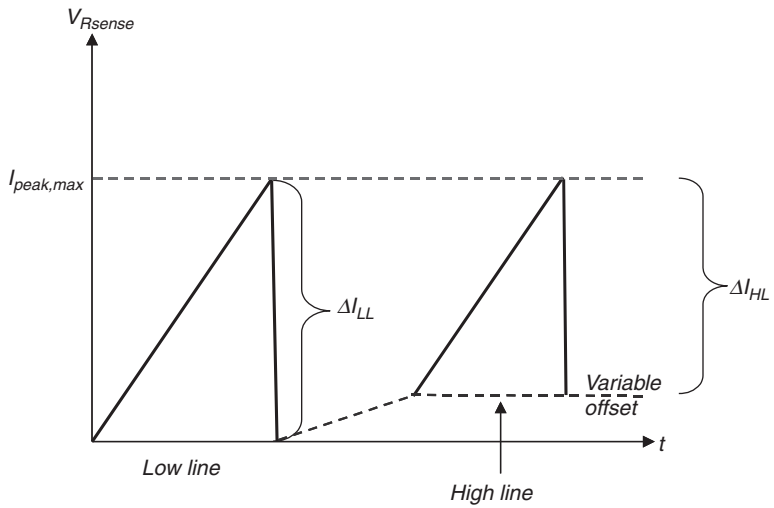

FIGURE 7-48 Offsetting the voltage floor helps to reduce the current excursion at high line.

where the ramp generator finds its place. The easiest way to solve this system is to apply the superposition theorem:

$$V_{ramp} \text{ and } V_{bulk} \text{ grounded: } V_{CS} = \frac{R_{ramp}||R_{OPP}}{R_{ramp}||R_{OPP} + R_{comp}} V_{sense} \tag{7-129}$$

$$V_{ramp} \text{ and } V_{sense} \text{ grounded: } V_{CS} = \frac{R_{ramp}||R_{comp}}{R_{ramp}||R_{comp} + R_{OPP}} V_{bulk} \tag{7-130}$$

$$V_{bulk} \text{ and } V_{sense} \text{ grounded: } V_{CS} = \frac{R_{OPP}||R_{comp}}{R_{OPP}||R_{comp} + R_{ramp}} V_{ramp} \tag{7-131}$$

From these equations, the total sense voltage V_{CS} is obtained by summing Eqs. (7-129) through (7-131). We can then extract a value for the compensation resistor we are looking for:

$$R_{OPP} = \frac{(V_{CS} - V_{bulk})R_{ramp}R_{comp}}{V_{ramp}R_{comp} + V_{sense}R_{ramp} - V_{CS}(R_{ramp} + R_{comp})} \tag{7-132}$$

To compensate a given converter, place it in the operating conditions under which you would like it to enter hiccup. For instance, our flyback delivers 3 A for the nominal power, and the maximum of the specification is 4 A. Supply the converter with the highest input level and load it with 3.7 A, including some safety margin. Now, collect the information needed to feed Eq. (7-132) with. Let us assume we have measured the following data:

$V_{bulk} = 370$ V (maximum value in this example)
$S_{ramp} = 133$ mV/µs

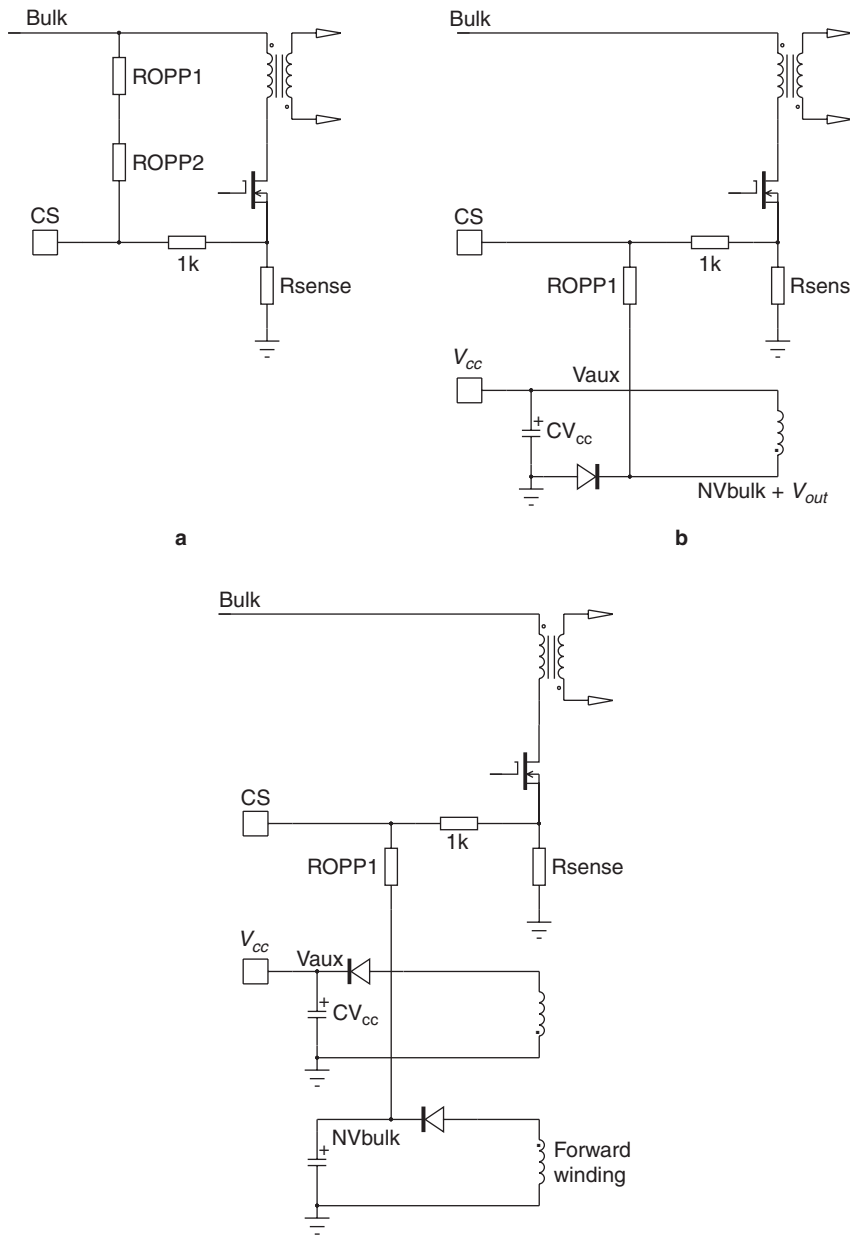

FIGURE 7-49 Compensating the controller at high line helps reduce the converter power capability.

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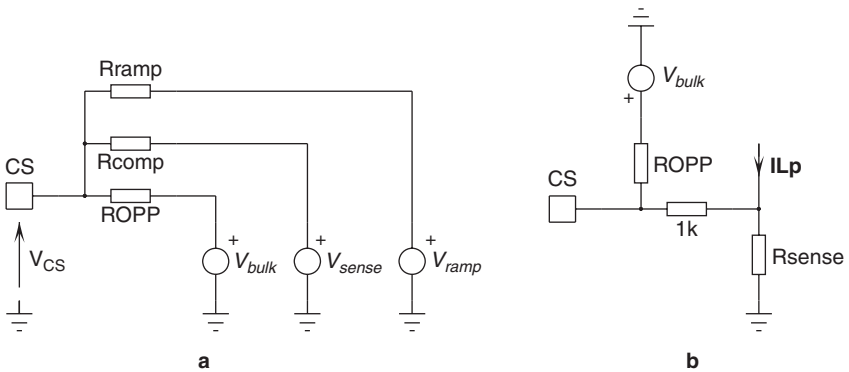

FIGURE 7-50 A simplified representation including a ramp generator if present.

$V_{sense} = 830$ mV
$F_{sw} = 65$ kHz
$t_{on} = 3.5$ µs
$R_{ramp} = 20$ kΩ
$R_{comp} = 1$ kΩ
$V_{CS,max} = 1.1$ V—from the controller data sheet, maximum current limit

V_{sense} is the peak voltage measured across the sense resistor, t_{on} is the operating on time, and S_{ramp} is the ramp compensation slope.

Beyond $P_{out,max}$, we would like to shut down the power supply. What overpower resistor must we install to follow the suggestions of Fig. 7-49a? Applying Eq. (7-132) gives

$$R_{OPP} = \frac{(V_{CS} - V_{bulk})R_{ramp}R_{comp}}{S_{ramp}t_{on}R_{comp} + V_{sense}R_{ramp} - V_{CS}(R_{ramp} + R_{comp})}$$
$$= \frac{(1.1 - 370) \times 20k \times 1k}{0.133 \times 3.5 \times 1k + 830m \times 20k - 1.1 \times (21k)} = 1.22\,\text{M}\Omega \qquad (7\text{-}133)$$

In some cases, there is no ramp compensation at all. The compensation resistor formula simplifies to

$$R_{OPP} = R_{comp}\frac{V_{bulk} - V_{CS}}{V_{CS} - V_{sense}} = 1k \times \frac{370 - 1.1}{1.1 - 0.83} = 1.36\,\text{M}\Omega \qquad (7\text{-}134)$$

To plot the effects of the OPP compensation from Fig. 7-50b, we can derive the expression of the peak current (no external ramp in this example):

$$I_{L_p}(V_{bulk}) = \frac{R_{OPP} + R_{comp}}{R_{sense}R_{OPP}}\left(V_{CS} - V_{bulk}\frac{R_{comp}}{R_{comp} + R_{OPP}}\right) + \frac{V_{bulk}}{L_p}t_{prop} \qquad (7\text{-}135)$$

Results of compensated and noncompensated converters appear in Fig. 7-51.

Despite this technique, given the dispersion on the current-sense limit, the primary inductance, and the sense elements, precisely clamping the secondary side current represents a difficult exercise. Another solution lies in directly monitoring the secondary side current and instructing the controller to shut down.

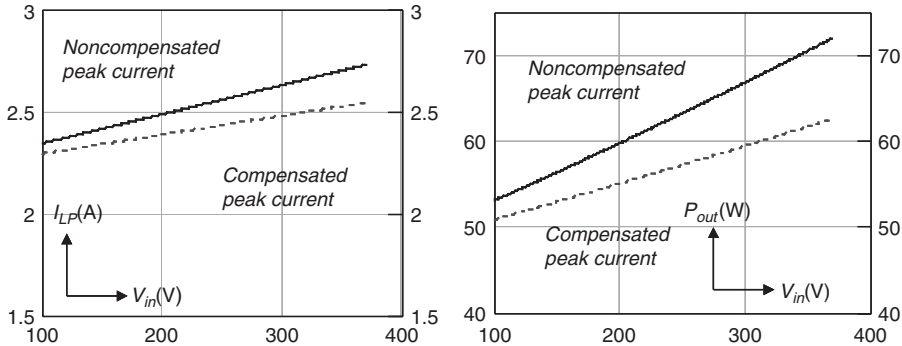

FIGURE 7-51 Comparison of a noncompensated and a compensated flyback converter operated in DCM.

7.11.10 Sensing the Secondary Side Current

In an isolated flyback, the controller uses an optocoupler to sense the output voltage and reacts accordingly depending on the power demand. Why not also use this loop to pass some information pertaining to the output current? Figure 7-52 offers a solution associating a TL431 and a bipolar transistor.

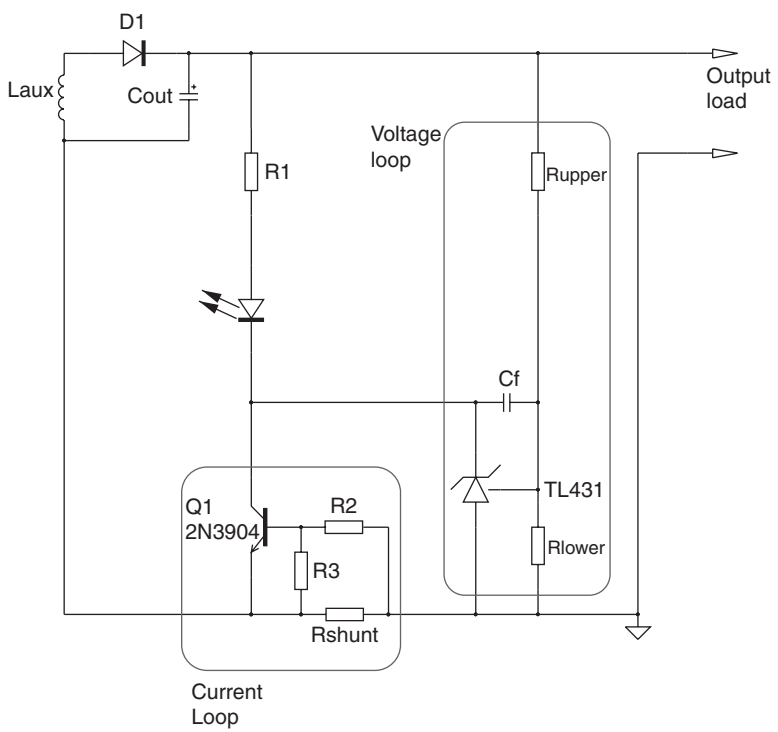

FIGURE 7-52 Adding a small bipolar transistor helps to control the direct current delivered to the load.

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When the current flowing through R_{shunt} produces a voltage across R_3 below Q_1 threshold voltage (≈650 mV at T_j = 25 °C), the TL431 controls the loop alone. When the voltage drop on R_3 reaches 650 mV, then Q_1 starts to conduct and takes over the TL431: more current flows into R_1 and the controller reduces its duty cycle. In a short-circuit condition, the TL431 leaves the picture and Q_1 makes the converter work as a constant-current generator. Figure 7-53 shows the kind of output characteristic you can get from this arrangement. This

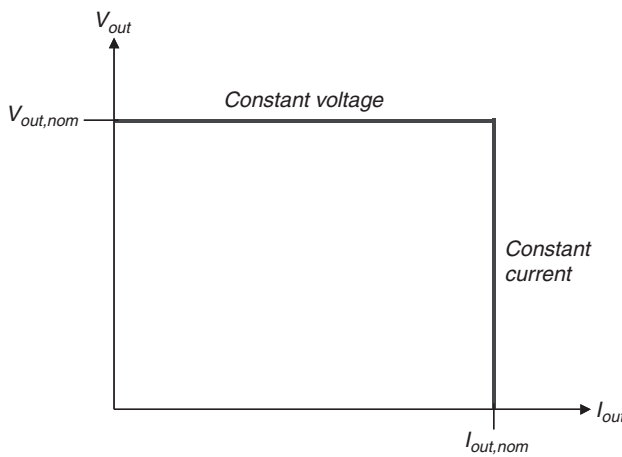

FIGURE 7-53 Below the maximum current, the converter maintains a constant output voltage. If the load consumes more current, the current loop takes over and controls the converter.

is called a *constant-current constant-voltage* (CC-CV) operation. The divider made around R_2 and R_3 helps to add a capacitor across R_3 in case a delay is necessary (for printer applications, for instance, where the load is made of short high-current bursts). If you set R_3 to 10 kΩ and R_2 to 1 kΩ, then triggering on a 2 A output current means a shunt resistor of the following value:

$$R_{shunt} = \frac{V_{be}(R_3 + R_2)}{I_{out}R_3} = \frac{650m(10k + 1k)}{10k \times 2} = 357\,\text{m}\Omega \tag{7-136}$$

Unfortunately, the power dissipated by the shunt reaches

$$P_{shunt} = I_{out}{}^2 R_{shunt} = 4 \times 0.357 = 1.43\,\text{W} \tag{7-137}$$

This power dissipation can be explained by the voltage drop needed across the shunt to trip the circuit. It is true that a germanium transistor would offer a better alternative, but who remembers the AC127 found in our old car radios (ahem, and the OC70)?

Also, as explained, despite a rather good distribution of the transistor V_{be}, its value changes with the junction temperature with a slope of −2.2 mV/°C. It might not represent a problem with a loose output current limit specification, say, ±15%, but in some cases, it might not be acceptable. A way to circumvent this problem is to select a dedicated controller such as the MC33341 or the more recent NCP4300 from ON Semiconductor (V_{drop} = 200 mV).

7.11.11 Improving the Drive Capability

The transistor turn-off time also takes its share of the total propagation delay. When you are using a large Q_G MOSFET, pulling down the gate requires a certain amount of current that the controller can sometimes have problem absorbing. In that case, a low-cost 2N2907 can help to speed up the gate discharge. Figure 7-54a depicts the way to wire it; Fig. 7-54d shows the improvement.

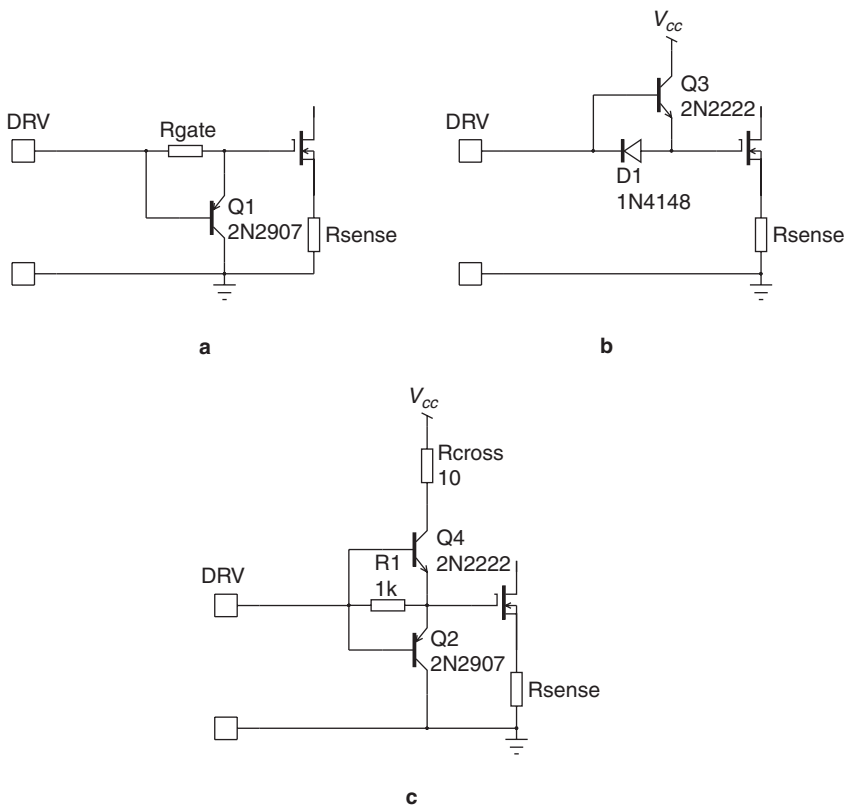

FIGURE 7-54a, b, and c Adding low-cost bipolars can dramatically improve the driving performance and ease the controller burden in presence of large Q_G MOSFETs.

We have seen through Eq. (7-110) that the controller dissipation can reach a few hundred milliwatts in the presence of important V_{cc} voltages and big MOSFETs. To remove the driving burden from the controller, a simple external NPN transistor wired as an emitter follower can reduce the package temperature (Fig. 7-54b). The diode D_1 ensures a fast discharge of the gate. Finally, if you need both fast charge and fast discharge performance, Fig. 7-54c might represent a solution. The resistor in series with V_{cc} limits the cross-conduction current, a heavy noise generator that can often disturb the controller. If this low-cost buffer is not enough in terms of current, you can always select a dedicated dual driver such as the MC33151/152, which is able to deliver 1.5 A peak.

By the way, why does the UC384X output stage always deliver more than the new CMOS-based controllers found on the market? Well, this is mainly due to the bipolar nature of the UC384X driver which behaves as a real current source. When the upper or lower transistor

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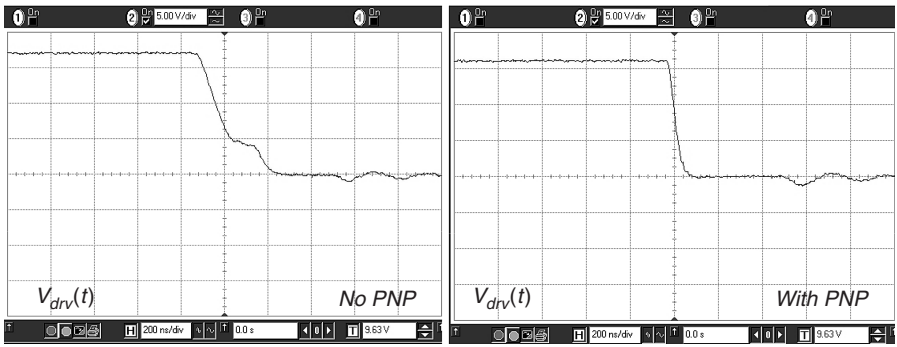

FIGURE 7-54d This picture shows the difference in turn-off times when a small PNP is added as recommended in the text.

closes, to either bias or discharge the gate, the transistor becomes a current source whose value stays relatively independent of its V_{ce} (see Early effect). With a output stage made of MOSFETs, when closed, the upper-side MOSFET offers a non linear resistive path. The current available to drive the flyback transistor gate thus depends on the gate-source level itself.

$$I_{gate}(t) = \frac{V_{cc} - V_{GS}(t)}{R_{DS(on)}} \tag{7-138}$$

In this formula, the resistive term in the denominator behaves in a nonlinear manner, and its value depends on the die temperature: when a CMOS-based controller heats up, its driving capability reduces. It can explain why the EMI signature changes after a warm-up sequence or why the switching noise on the controller also improves after this period: as both lower and upper side $R_{DS(on)}$ have increased, the shoot-through current has diminished.

7.11.12 Overvoltage Protection

An overvoltage protection (OVP) circuit protects the load, and the converter itself, when the loop control is lost, for instance, when the optocoupler breaks or a wrong solder joint is made in production. It the controller sometimes hosts its own OVP circuitry, it often does not and you need to design it as a separate circuit. Depending on your end customer, since an OVP detection is considered a dangerous event, most of designs are latched and remain off when such a situation arises. The reset occurs when the user unplugs the converter from the wall outlet. Figure 7-55a and b offers two possibilities to detect these OVPs: you can either observe the secondary voltage image on the auxiliary winding or detect the information via the output voltage directly. In the latter, you need an optocoupler to transport the secondary side information to the primary side: the cost is obviously higher, but it does not suffer from coupling problems (see Fig. 7-44 for leakage problems). Observing the auxiliary voltage always refers to the leakage term. In Fig. 7-55a, the monitored voltage is physically separated from the V_{cc} line. Thus, we can easily install a filter without interacting with the controller supply. Then a voltage divider made up of R_9 and R_{10} selects the level at which the circuit must latch. When the voltage over R_9 reaches $\approx$0.65 V at $T_j = 25$ °C, then the discrete *silicon-controlled rectifier* (SCR) latches and pulls V_{cc} down to ground. Make sure an adequate margin exists, especially on transient load removals or start-up sequences, to avoid false tripping of the latch. A 100 nF (C_5) capacitor helps to improve the noise immunity. As the controller V_{cc} rail can be of rather low impedance, it is necessary to locally degrade it via resistor R_4, set to 47 Ω in this example; otherwise the SCR could suffer from an overcurrent problem.

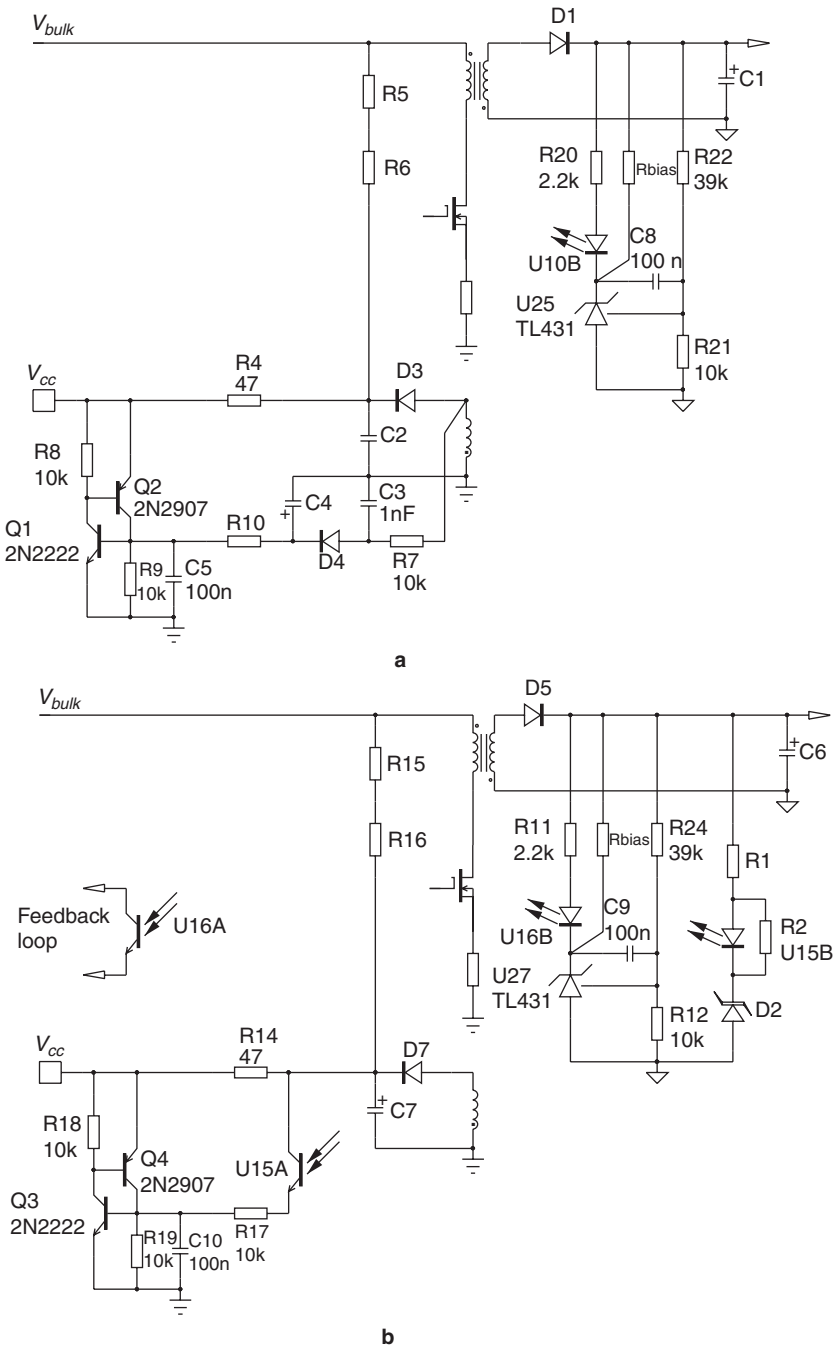

FIGURE 7-55 A discrete SCR latches off in the presence of an OVP event.

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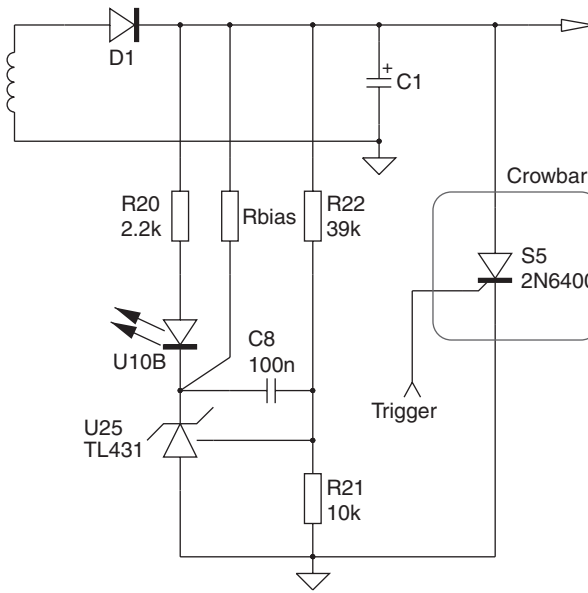

FIGURE 7-56 A crowbar circuit immediately short-circuits the converter output in case of loop failure. The trigger signal can come from a dedicated controller such as the MC3423.

Figure 7-55b does not differ that much, except that the order to latch comes from the secondary side. The optocoupler LED will pass current when the output voltage reaches the zener voltage (D_2) plus a 1 V drop from the LED itself. At this moment, the U_{15A} emitter will go up and bias the SCR to protect the converter.

In case the load cannot suffer any voltage runaway, the crowbar option might represent a possible choice (Fig. 7-56). The circuit detects the OVP as Fig. 7-55b does, but it triggers a powerful thyristor to actually short-circuit the converter supply. If the power supply features a short-circuit protection, hiccup mode will be entered until the supply is stopped. Readers interested in this device can have a look at the MC3423, a dedicated crowbar driver from ON Semiconductor.

7.12 STANDBY POWER OF CONVERTERS

Since the days when Thomas Edison powered the first lightbulb in 1879, electricity has been considered a gift, and our modern consumer lifestyles show this to be true. Unfortunately, freedom always comes at a price. International agencies have now been set up to regulate energy production amid concerns that atmospheric emissions from power stations could be the cause of many weather-related problems. Solutions need to quickly emerge which reduce energy bills while helping us consume electricity in a clever way. Working closely with technical committees such as the International Energy Agency (IEA) [7], some semiconductor companies offer new, ready-to-use integrated solutions to tackle the standby power problem. This paragraph reviews the roots of the standby losses and presents currently available solutions to help designers easily meet new coming standards or so-called codes of conduct.

7.12.1 What Is Standby Power?

Let us start by defining standby power so as to avoid any of the common misunderstandings between designers and final users. We can distinguish different kinds of standby power depending on the type of equipment concerned:

1. *When the active work of an apparatus connected to the mains has come to an end, the power drawn by this apparatus should ideally tend to* 0 W. By *active work*, we mean a function for which the apparatus is designed, for instance, charging a battery. When the user disconnects a cell phone from the charger and leaves it plugged in the mains outlet, the charger should become inert, drawing nearly zero power. If you want to check for this parameter, just touch a charger or an ac adapter case (your notebook's, for example) and feel its temperature through your hand. You will be surprised how hot some of these can be, clearly revealing their poor standby power performance!
2. *When the active work of an apparatus connected to the mains has been temporarily deactivated, either automatically or through a user demand, the power drawn from this apparatus shall be the smallest possible*. Again, by active work, we can take the example of a TV set left in standby via a remote control order, but whose circuitry (including the shining front LED!) shall be kept alive to respond to a wake-up signal as soon as the user wishes it. It is the designer's duty to keep the internal consumption very low (using low-power μPs, high-efficiency LEDs, etc.). However the final element remains the switch-mode power supply (SMPS) connected to the ac supply. Unfortunately, most of current SMPS efficiencies drop to a few tens of percent when operated well below their nominal power. If you have a 25% efficiency at 500 mW output power, then you consume close to 2 W. A lot of electronic apparatus spend most of their time in this mode. So the power consumed represents a significant fraction of the domestic power budget at around 5%.

Documents and various links pertinent to standby power can be found on the Web site via Refs. 7 and 8.

7.12.2 The Origins of Losses

Figure 7-57 portrays the typical arrangement of the flyback converter, one of today's most popular converter topologies used in consumer products. Components are symbolically represented for a better understanding of the process. Suppose that the power supply switches at 100 kHz and

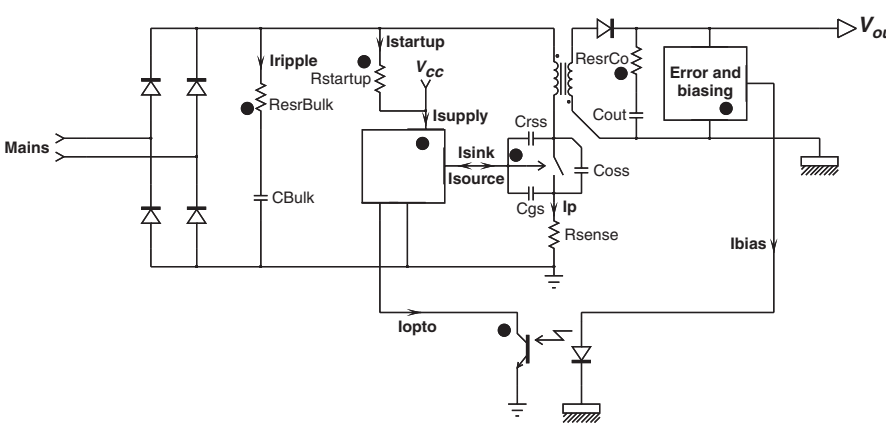

FIGURE 7-57 The various losses that the converter is the seat of. Every spot on the picture is a source of loss.

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delivers 12 V nominal dc output voltage. With no load on its output, i.e., in a standby mode, the controller will naturally reduce the duty cycle to ensure the right output level. Let us now try to identify the loss contributors. If we start from the right side, we first have a feedback network whose function is to ensure that the output level stays within given specifications. A TL431-based network requires at least 1 mA to properly operate plus a few microamperes flowing through the sensing network. You also need to bias the optocoupler LED in order to instruct the primary side controller to reduce the power transfer. Including all these secondary losses, we come to an output power of around 24 mW in no-load situation if we consider a total secondary side current of 2 mA.

A few other milliwants is circulating through various other resistive elements (secondary diode, capacitor ESRs, etc.) but since we assume that the rms current is low, they can be neglected. On the primary side, every time the power MOSFET closes, it discharges the drain node parasitic capacitance consisting of MOSFET C_{oss} and C_{rss}, transformer stray capacitance, etc. Each capacitor C is charged to a voltage V and discharged at a given switching frequency F_{sw}. The average losses generated by these elements are defined by

$$P_{loss} = 0.5CV^2F_{sw} \tag{7-139}$$

Here C and V are fixed elements and thus difficult to modify. However, since the switching frequency can be selected, it represents a first possible trail to follow. The MOSFET itself presents ohmic losses and dissipates an average power given by (conduction losses in DCM)

$$P_{MOSFET,cond} = \frac{1}{3}I_{peak}{}^2DR_{DS(on)} \tag{7-140}$$

The pulse width modulator (PWM) controller, the heart of the SMPS, needs power to beat. If the device is a bipolar UC384X based, it is likely to consume around 20 to 25 mA in total, which from a 12 V source gives 240 mW best case. The driving current also represents an important part of the budget. Operating a 50 nC MOSFET at 100 kHz requires a 5 mA average current [Eq. (7-110)] directly consumed from the controller V_{cc}, whatever the duty cycle. Another 60 mW of power... The biggest portion of all? The naughty start-up resistor which ensures at least 1 mA of start-up current needed for these bipolar controllers! On a 230 Vrms mains, another 300 mW is wasted in heat.

If we sum up all contributors, including front-stage losses (diode, bulk capacitor ESR, etc.) and drain clamp losses, we can easily end up with a no-load standby power of around 1 W.

7.12.3 Skipping Unwanted Cycles

We have seen that the switching frequency plays a significant role in the power loss process. Since we do not transmit any power in standby (or just a little depending on the application), why bother the MOSFET with a continuous flow of pulses? Why not just transmit the needed power via a burst of pulses and stay quiet the rest of the time? We would surely introduce a bit of output ripple because of this quiet period, but a lot of switching losses would fade away! This is the principle of skip-cycle regulation: the controller skips unnecessary switching cycles when entering the standby area. Figure 7-58 depicts how skip cycle takes place in low standby controllers from ON Semiconductor (NCP120X series). The controller waits until the output power demand goes low and then starts skipping cycles. Skipping a cycle means that some switching cycles are simply ignored for a certain time. Figure 7-59 gives the basic circuitry needed for this technique. When the feedback voltage on the FB pin passes below the skip source V_{skip}, the comparator CMP1 resets the internal latch. As all pulses are now stopped, the output voltage starts to drop, leading to a movement of the feedback voltage. When the skip comparator detects that the FB voltage has gone above the skip source V_{skip}, pulses are released, bringing V_{out} toward the target. At this moment, the FB voltage falls again below the skip source value and a hysteretic regulation takes place. If V_{skip} equals 1 V and the FB pin can swing up to 3 V (current-sense limit

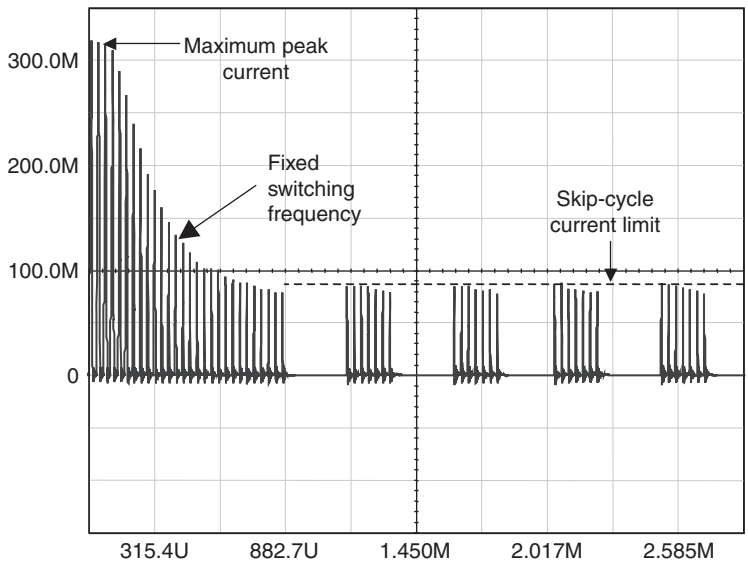

FIGURE 7-58 Skip-cycle takes place at low peak currents which guarantees noise-free operation.

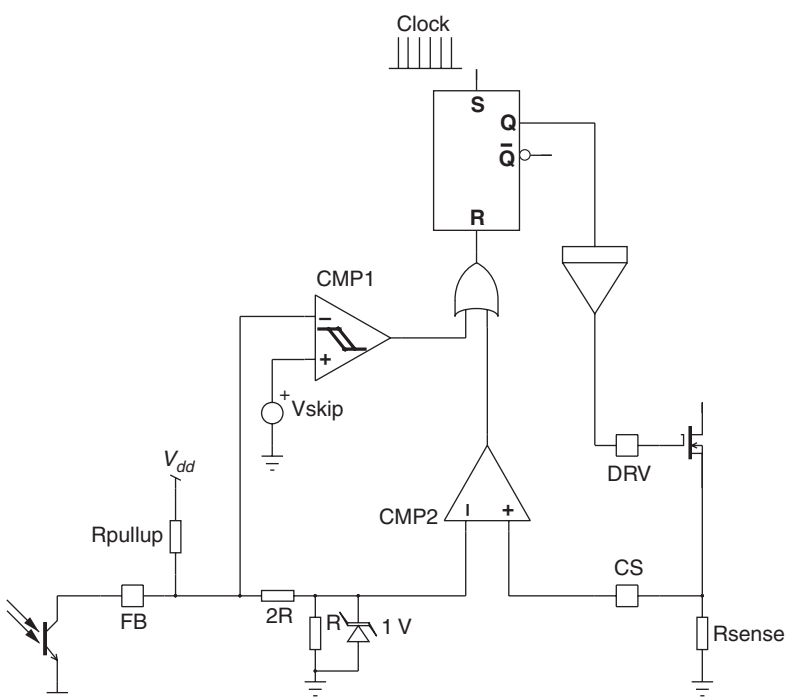

FIGURE 7-59 A simple comparator observing the feedback loop is enough to implement skip-cycle.

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of 1 V), then the skip operation occurs at 30% of the maximum authorized peak current. When the power demand increases again, the pulse bunches come closer to each other until the controller goes back to a full PWM pattern with a variable peak current.

Given the hysteretic nature of the regulation in skip mode, you have no control over the way pulse packets are arranged by the controller. What matters is the loop bandwidth, the load level, and the hysteresis on the skip-cycle comparator. The best standby is obtained when only a few pulses occur, separated by several milliseconds of silence (see Fig. 7-43). Of course, it then becomes difficult to maintain the self-supply, and all losses must be chased. If the peak current level at which skip-cycle occurs is selected low enough, you will not have audible noise issues but standby will suffer. Noise comes from the mechanical resonance of the transformer (or the *RCD* clamp capacitor, especially disk types), excited by (1) the audible frequencies covered during the hysteretic regulation and (2) the sharp discontinuity associated with the pulse packet appearance. However, circuits such as the NCP120X series naturally minimize the noise generation because you can select the skip-mode peak current.

7.12.4 Skipping Cycles with a UC384X

Of course you can skip cycles with a UC384X! Using a low-cost LM393, Fig. 7-60a shows how to stop operations of the PWM controller by lifting up its current-sense pin. Thanks to the absence of an internal LEB, if the current-sense pin is pulled higher than 1 V, the circuit fully stops pulsing. Let us now have one of the comparator input observing the feedback voltage and the other receiving a portion of the reference level—our skip reference source V_{skip} in the previous example. Add a simple PNP transistor to the comparator output and the trick is done. As the comparator noninverting pin (FB node) reaches the voltage set by R_6, Q_1 base is pulled down and the controller stops and restarts the switching operations to a pace imposed by the feedback loop: skip-cycle is born. Figure 7-60b shows the captured waveforms at different output levels, P_{out1} being the lowest one. Thanks to this circuit, we were able to divide the no-load standby power by 2.

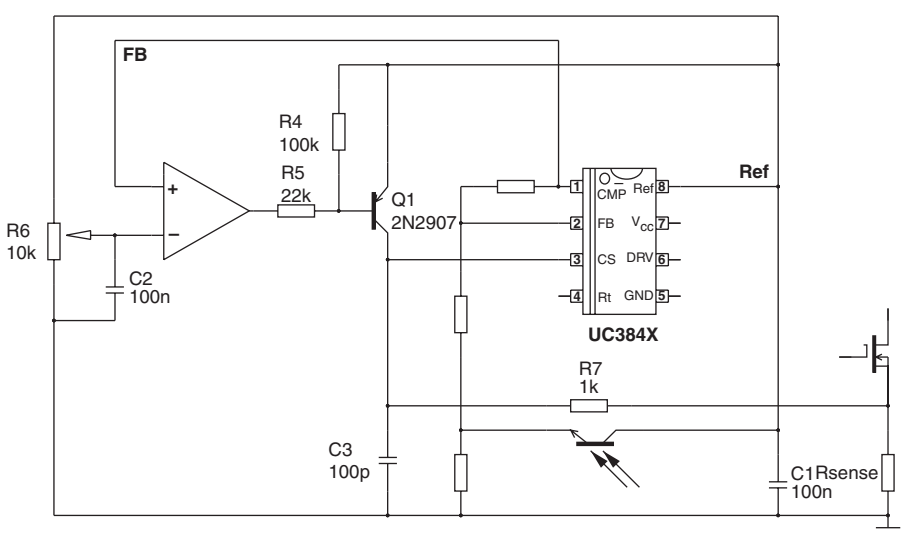

FIGURE 7-60a A simple comparator brings skip-cycle to the UC384X controller.

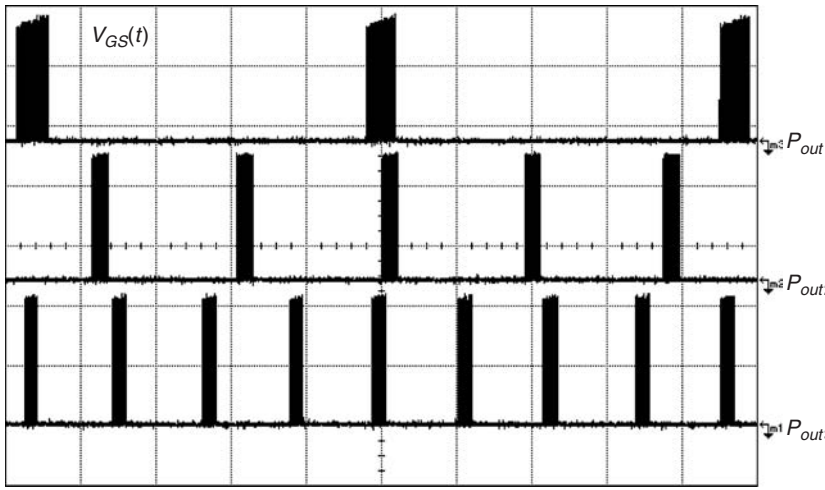

FIGURE 7-60b Once implemented, the standby power was divided by 2, dropping below 1 W.

7.12.5 Frequency Foldback

The frequency foldback technique offers another interesting alternative to the skip-cycle operation. Rather than artificially slice the switching pattern, a *voltage-controlled oscillator* (VCO) starts to act when the imposed peak current reaches a certain low point. As the controller does not allow this current to further decrease, the only way to reduce the transmitted power lies in a switching frequency reduction. This solution is usually implemented in partnership with a quasi-resonant flyback converter. As the frequency naturally increases when the load gets lighter, an internal oscillator monitors the minimum switching period. Usually, the designer forbids the frequency to exceed 70 kHz for EMI concerns. When the peak current freezes (around 30% of the maximum allowed peak current), the frequency can no longer increase as the feedback loses current control (the current is now fixed). The VCO thus takes over and linearly decreases the frequency to a few hundred hertz if necessary. Figure 7-61a shows the frequency versus output power plot whereas Fig. 7-61b plots a few operating waveforms from the NCP1205, a controller implementing this principle.

7.13 A 20 W, SINGLE-OUTPUT POWER SUPPLY

This design example describes how to calculate the various component values for a 20 W flyback converter operated on universal mains with the following specifications:

$V_{in,min}$ = 85 Vrms
$V_{bulk,min}$ = 90 Vdc (considering 25% ripple on the bulk capacitor)
$V_{in,max}$ = 265 Vrms
$V_{bulk,max}$ = 375 Vdc
V_{out} = 12 V
$V_{ripple} = \Delta V$ = 250 mV
V_{out} drop = 250 mV maximum from I_{out} = 0.2 to 2 A in 10 μs

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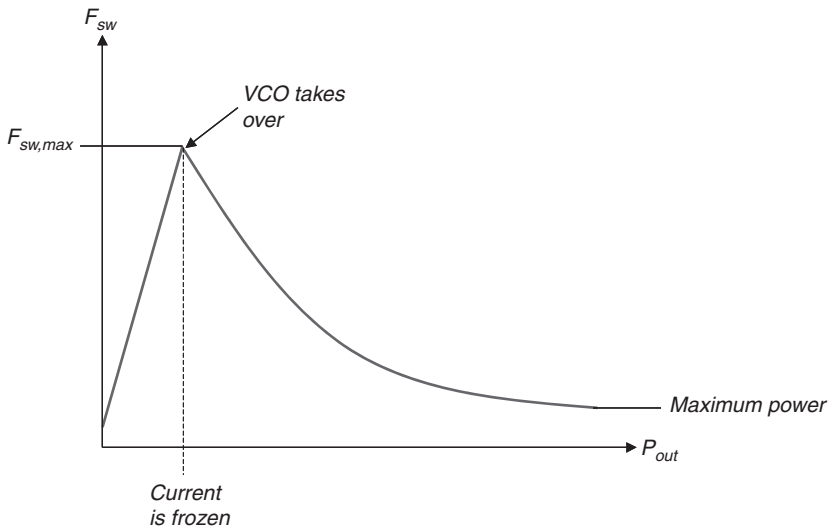

FIGURE 7-61a The QR flyback sees its frequency going up as the load current goes down. At a certain point, since the peak current cannot decrease anymore, the controller folds the frequency back.

$I_{out,max}$ = 1.66 A
MOSFET derating factor k_D = 0.85
Diode derating factor k_d = 0.5
RCD clamp diode overshoot V_{os} = 15 V

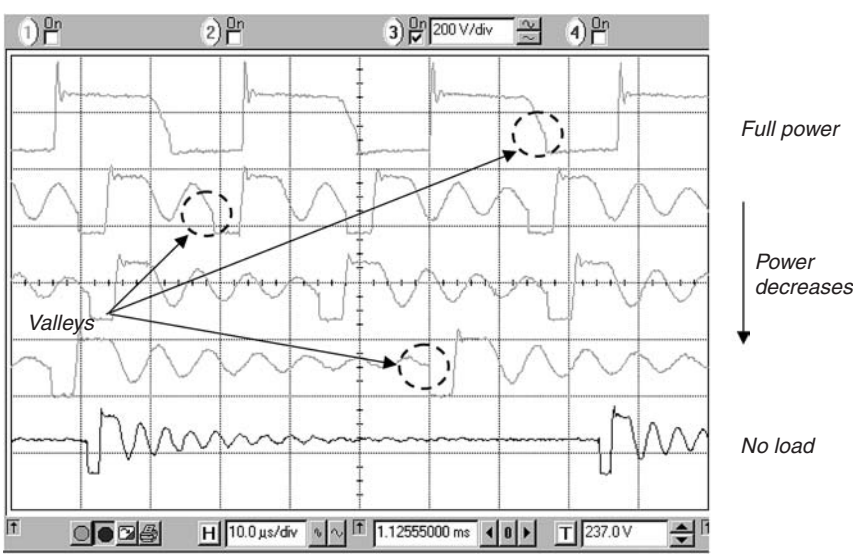

FIGURE 7-61b Here, several drain-source waveforms were captured at different output power levels. Please note the frequency reduction as explained and the valley switching even at light loads.

First, we are going to select peak current-mode control for several reasons:

1. The market offer in terms of controllers is rich.
2. Current-mode control inherently offers superior input voltage rejection.
3. The primary current is permanently monitored.
4. DCM-to-CCM mode transition is not a problem for this operating mode.

The switching frequency will be selected to be 65 kHz. It offers a good compromise among switching losses, magnetic size, and EMI signature. Given that the conducted EMI standard CISPR-22 specifies an analysis between 150 kHz and 30 MHz, having a 65 kHz switching frequency implies a second harmonic below 150 kHz and a third harmonic already reduced in amplitude. For your information, the vast majority of ac–dc adapters for notebooks are operated at 65 kHz.

Now, the operating mode: DCM or CCM? This is obviously the key point. Each mode has its advantages, and the points below offer a brief summary of pros and cons:

DCM

- Small inductor.
- No RHPZ in the low-frequency portion, higher crossover frequency achievable.
- First-order system, even in voltage mode, simple to stabilize.
- Simple low-cost secondary diode does not suffer from t_{rr} losses.
- No turn-on losses on the MOSFET—$I_D = 0$ at turn-on (not considering capacitive losses).
- Valley switching is possible in quasi-resonant mode.
- It is easier to implement synchronous rectification on the secondary side.
- It is not subject to subharmonic oscillations in current mode.
- Large ac ripple, inducing conduction losses on the MOSFET and other resistive paths (ESRs, copper wires).
- Bigger hysteresis losses on the ferrite material.

CCM

- Low ac ripple, smaller conduction losses compared to DCM.
- Low hysteresis losses due to operation on B-H minor loops.
- Low ripple on the output.
- t_{rr} related losses on both the secondary side diode and the primary side MOSFET.
- Requires fast diodes or Schottky to avoid excessive losses.
- Turn-on losses on the MOSFET—$I_D \neq 0$ at turn-on, overlap of $V_{DS}(t)$ and $I_D(t)$.
- Requires a compensation ramp in peak current-mode control when duty cycle is above 50%.
- It is more difficult to stabilize in voltage mode.
- RHPZ hampers the available bandwidth.
- Despite similar energy storage, the inductance increases in CCM and so does the transformer size.

Well, reading these notes, you probably see more arguments in favor of the DCM operation than the CCM. This is true for the low-power range where DCM represents the easiest way to go. Generally speaking, CCM concerns low output voltages with high current, e.g., 5 V at 10 A, whereas DCM would be suited for higher voltages and lower currents. Most of the cathode ray

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tube–based TVs are running a DCM flyback converter delivering 130–160 V/1 A or less. Why DCM? Because high-V_{RRM} inexpensive diodes are usually slow and CCM would induce a lot of switching losses.

Based on what is seen on the market, below 30 W, you can design DCM without any problems. Above, ac losses often become predominant in your design, especially if the converter size prevents you from using large aluminum cans featuring low ESRs. As such, adopting CCM helps reduce the stress on the secondary side capacitors and the transformer wires. If this is true for low line where CCM seems to be unavoidable, what about high line? Well, a good tradeoff consists of running CCM in low-line conditions and entering DCM in the upper voltage range, reducing turn-on losses, which is less problematic at low bulk voltages. This is what was demonstrated in Ref. 5 and is often implemented in high-power designs of 60 to 100 W ac–dc adapters. Nevertheless, some designers still prefer to operate in critical conduction mode (so-called boundary mode or quasi-square wave resonant mode), even in high-power designs because of (1) the reduced switching stress on semiconductors such as the secondary diode or the primary MOSFET and (2) the ease of implementation of synchronous rectification.

Ok, let us go all DCM for this small 20 W converter. As usual, a few steps will guide us through the design procedure. For a flyback, it is good practice to start with the transformer turns ratio.

We explained in this chapter that the turns ratio is intimately connected to the maximum allowable drain–source voltage of the MOSFET. In the industry, it is common practice to select 600 V MOSFETs for universal mains operations. It will be our choice here. Then, if we assume a good transformer featuring a leakage inductance below 1% of the primary inductance, a k_c of 1.5 seems to be a reasonable number. Combining Eqs. (7-37a) and (7-37b), we have

$$N = \frac{k_c(V_{out} + V_f)}{BV_{DSS}k_D - V_{os} - V_{bulk,max}} = \frac{1.5 \times (12 + 0.6)}{600 \times 0.85 - 15 - 375} = 0.157 \qquad (7\text{-}141)$$

Let us pick a turns ratio of 0.166 or $1/N = 6$. In the above equation, we assumed the diode forward drop to be 0.6 V.

By using the equation derived in Chap. 5 [Eq. (5-118)] and tweaking it to account for the transformer turns ratio, we have an equation which delivers the peak current to be in DCM boundary mode at the lowest input voltage:

$$I_{peak} = \frac{2\left(V_{min} + \dfrac{V_{out} + V_f}{N}\right)(V_{out} + V_f)N}{\eta V_{bulk,min}R_{load}} \qquad (7\text{-}142)$$

In this equation, the term $V_{bulk,min}$ relates to the minimum voltage seen on the bulk rail, also called V_{min} in Fig. 6-4. Assume our bulk capacitor obeys Chap. 6 recommendations and lets the maximum ripple be around 25% of the rectified peak. In that case, the minimum input voltage seen by the converter is

$$V_{min} = V_{bulk,min} = 0.75 \times 85 \times \sqrt{2} = 90 \text{ Vdc} \qquad (7\text{-}143)$$

After Fig. 6-4 notations, the average low-line bulk voltage will be

$$V_{bulk,avg} = \frac{V_{peak} + V_{min}}{2} = \frac{85 \times \sqrt{2} + 90}{2} = 105 \text{ V} \qquad (7\text{-}144)$$

Updating Eq. (7-142) with real values leads to a peak current of

$$I_{peak} = \frac{2 \times \left(90 + \dfrac{12 + 0.6}{0.166}\right) \times (12 + 0.6) \times 0.166}{0.85 \times 90 \times 7.2} = 1.26 \text{ A} \qquad (7\text{-}145)$$

Being given the peak current at which we are going to work makes the inductor calculation an easy step:

$$L_p = \frac{2P_{out}}{I_{peak}^2 F_{sw} \eta} = \frac{2 \times 20}{1.26^2 \times 65k \times 0.85} = 456\,\mu\text{H} \tag{7-146}$$

Let us adopt a rounded value of 450 μH. The duty cycle variations can now be deduced as the peak current remains constant at high- and low-line conditions. The variable for the voltage names used below refers to Fig. 6-2b.

$$t_{on,max} = \frac{I_{peak} L_p}{V_{bulk,min}} = \frac{1.26 \times 450u}{90} = 6.3\,\mu\text{s} \tag{7-147}$$

$$D_{max} = \frac{t_{on,max}}{T_{sw}} = \frac{6.3u}{15u} = 0.42 \tag{7-148}$$

$$t_{on,min} = \frac{I_{peak} L_p}{V_{bulk,max}} = \frac{1.26 \times 450u}{375} = 1.5\,\mu\text{s} \tag{7-149}$$

$$D_{min} = \frac{t_{on,min}}{T_{sw}} = \frac{1.5u}{15u} = 0.10 \tag{7-150}$$

However, given the bulk ripple at low line, the duty cycle will also move between minimum and maximum values as given by Eqs. (7-147) to (7-150). To calculate the average conduction MOSFET losses at low line, we should calculate the squared rms current as a function of $D(t)$ and $V_{in}(t)$ since the ripple modulates these variables. Therefore, we should integrate this definition over a complete mains cycle to reach "averaged" power losses dissipated during a ripple cycle. To avoid this tedious calculation (the ripple is not exactly a ramp), we will calculate the rms content at the valley value as an extreme worst case:

$$I_{D,rms} = I_{peak}\sqrt{\frac{D_{max}}{3}} = 1.26 \times \sqrt{\frac{0.42}{3}} = 471\,\text{mA} \tag{7-151}$$

Since our MOSFET sustains 600 V, what $R_{DS(on)}$ must we select? A TO-220 package vertically mounted and operating on free air exhibits a thermal resistor junction-to-air $R_{\theta J\text{-}A}$ of roughly 62 °C/W. The maximum power this package can dissipate, without an added heat sink, depends on the surrounding ambient temperature. In this application, we assume the converter to operate in an ambient of 50 °C maximum. Choosing a maximum junction temperature for the MOSFET die of 110 °C, the maximum power accepted by the package is thus

$$P_{max} = \frac{T_{j,max} - T_A}{R_{\theta J-A}} = \frac{110 - 50}{62} = \frac{60}{62} = 0.96\,\text{W} \tag{7-152}$$

The conduction losses brought by the rms current circulation are

$$P_{cond} = I_{D,rms}^2 R_{DS(on)} @ T_j = 110\,^\circ\text{C} \tag{7-153}$$

From Eqs. (7-152) and (7-153), the $R_{DS(on)}$ at 110 °C must be smaller than

$$R_{DS(on)} @ T_j = 110\,^\circ\text{C} \le \frac{P_{max}}{I_{D,rms}^2} \le \frac{0.96}{0.471^2} \le 4.3\,\Omega \tag{7-154}$$

The MOSFET on resistance stated at a 25 °C junction almost doubles when the junction heats up and reaches 110 to 120 °C. As such, a first indication shows that the selected MOSFET will need a 25 °C $R_{DS(on)}$, which is lower than 2.1 Ω. Of course, switching losses are needed to complete

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the selection. Unfortunately, as they involve numerous stray elements, trying to analytically predict them is an impossible exercise. A SPICE simulation with the right MOSFET and transformer model can give an indication, but bench measurements remain the only way to accurately estimate them. In DCM, turn-on losses should theoretically be null, but the lump capacitor present on the drain discharges through the MOSFET. It induces the following losses, depending where the turn-on occurs: right at the sinusoidal top (maximum losses) or in the valley of the waveform (minimum losses):

$$P_{SW,lump}{}^{\max} = \frac{1}{2} C_{lump} \left(V_{bulk,max} + \frac{V_{out} + V_f}{N} \right)^2 F_{sw} \tag{7-155a}$$

$$P_{SW,lump}{}^{\min} = \frac{1}{2} C_{lump} \left(V_{bulk,max} - \frac{V_{out} + V_f}{N} \right)^2 F_{sw} \tag{7-155b}$$

The lump capacitor value can be extracted following App. 7A. A typical turn-off sequence appears in Fig. 7-62a. The turn-off sequence depends on the environment around the drain node, such as the presence of a snubber capacitor. Figure 7-62b shows an oscilloscope shot at a switch opening event which favorably compared to the simulation data. Until the V_{GS} reaches the plateau level, nothing changes. The drain does not move, but the current starts to bend, depending on the MOSFET transconductance (gm). At the beginning of the plateau, the MOSFET starts to block, the drain voltage rises, and the current further bends. The current keeps circulating in the MOSFET (acting as a linear resistor) until the drain voltage reaches a level where another current path exists (the current must flow somewhere, right?). At this time, the current falls to zero as it has been fully diverted elsewhere. In this particular case (case 1),

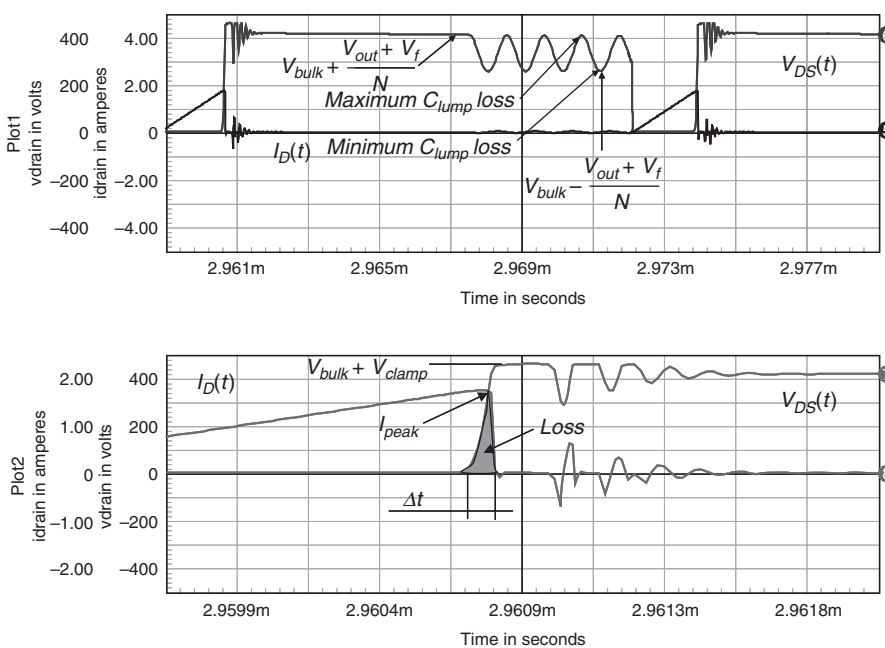

FIGURE 7-62a A typical turn-off sequence for a DCM flyback converter.

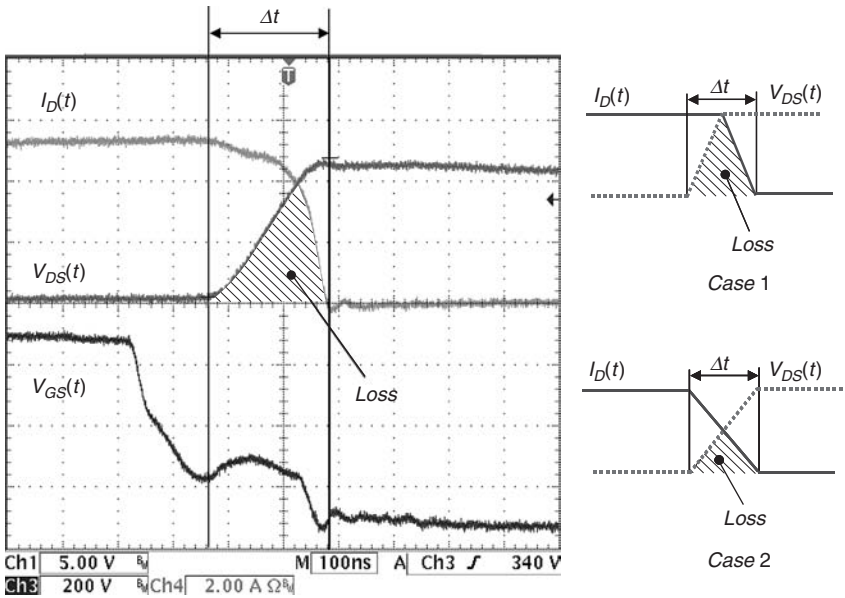

FIGURE 7-62b Worst case occurs when the drain voltage immediately rises up at the switch opening (case 1). If some snubber exists to slow the voltage rise, the idealized case 2 can happen with a more favorable loss budget.

considering the overlapping section as a triangle of Δt width, the average power dissipated by the MOSFET at turn-off is a simple triangle area.

$$P_{SW,off} = F_{sw}\int_0^{\Delta t} I_D(t)V_{DS}(t)\cdot dt = F_{sw}\left[\int_0^{\frac{\Delta t}{2}} I_{peak}(V_{bulk}+V_{clamp})\frac{2t}{\Delta t}\cdot dt\right.$$

$$\left. + \int_{\frac{\Delta t}{2}}^{\Delta t}(V_{bulk}+V_{clamp})I_{peak}\frac{2(\Delta t - t)}{\Delta t}\cdot dt\right]$$

$$P_{SW,off} = \frac{I_{peak}(V_{bulk}+V_{clamp})\Delta t}{2}F_{sw} \tag{7-156a}$$

If some snubber exists, the drain voltage will rise later and the overlap becomes more favorable (case 2). In that operating mode, the power dissipation shrinks to become:

$$P_{SW,off} = F_{sw}\int_0^{\Delta t} I_D(t)V_{DS}(t)\cdot dt = F_{sw}\int_0^{\Delta t} I_{peak}\frac{\Delta t - t}{\Delta t}\left(V_{bulk}+V_{clamp}\right)\frac{t}{\Delta t}\cdot dt$$

$$= \frac{I_{peak}(V_{bulk}+V_{clamp})\Delta t}{6}F_{sw} \tag{7-156b}$$

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On the final prototype, observing both MOSFET voltage and current, you can either extract the overlap time Δt and all needed variables, or have the oscilloscope compute the loss contribution for you. Once all losses are identified, the total MOSFET power dissipation must be calculated at both low- and high-line values. At low line, conduction losses are predominant, whereas at high line, switching losses take the lead:

$$P_{MOSFET} = P_{cond} + P_{SW,lump} + P_{SW,off} \tag{7-157}$$

Depending on the selected MOSFET and the various contributions, you might need to either select a lower $R_{DS(on)}$ type or add a small heat sink if the total power exceeds Eq. 7-152 limit. Considering Eq. 7-154 as a worst case, a MOSFET like the IRFBC30A could be the right choice (BV_{DSS} = 600 V, $R_{DS(on)}$ = 2.2 Ω).

Before closing down the MOSFET section, we can estimate the power dissipation burden on the controller driving stage. To fully turn the IRFBC30A on, a 23 nC electricity quantity (Q_G) needs to be brought to its gate-source space. If the controller operates from a 15 V auxiliary winding at a 65 kHz frequency, the dissipation on the chip is:

$$P_{drv} = F_{sw}Q_GV_{cc} = 65k \times 23n \times 15 = 22\,\text{mW} \tag{7-158}$$

Assuming our controller considers a current limit when the voltage image on its dedicated pin hits 1 V (a very popular value among controllers on the market), the sense resistor value (sometimes called the burden resistor) is evaluated by:

$$R_{sense} = \frac{1}{I_{peak}} \tag{7-159}$$

We need a peak current of 1.26 A. Considering a design margin of 10% (I_{peak} = 1.38 A), the sense resistor value equals:

$$R_{sense} = \frac{1}{1.26 \times 1.1} = 0.72\,\Omega \tag{7-160}$$

Unfortunately, this value does not fit the normalized resistor series E24/E48. Several solutions exist to cure this:

1. Put several resistors in parallel to reach the right value. In this case, two 1.4 Ω resistors would give 0.7 Ω.
2. Select a higher value and install a simple resistive divider. For instance, select a 0.82 Ω resistor. The needed peak current is 1.38 A. Once applied over the 0.82 Ω, it will develop 1.13 V. The divider ratio thus must be $\frac{1}{1.13} = 0.88$. By selecting a series resistor of 1 kΩ, the ground resistor is simply 7.3 kΩ. Figure 7-63 details the arrangement.

Using Eq. (7-151), the power dissipated by the sense resistor reaches

$$P_{R_{sense}} = I_{D,rms}{}^2R_{sense} = 0.471^2 \times 0.82 = 181\,\text{mW} \tag{7-161}$$

Now, we need to protect the MOSFET against the leakage spikes. We have seen how to derive the *RCD* clamp values, so let us put the equations to work. We have slightly tweaked expressions (7-44) to reveal the clamp coefficient k_c:

$$R_{clp} = \frac{(k_c - 1)\left[2k_c(V_{out} + V_f)^2\right]}{N^2F_{sw}L_{leak}I_{peak}{}^2} = \frac{(1.5 - 1)\left[2 \times 1.5 \times (12 + 0.6)^2\right]}{0.166^2 \times 65k \times \frac{450u}{100} \times 1.38^2} = 15.5\,\text{k}\Omega \tag{7-162}$$

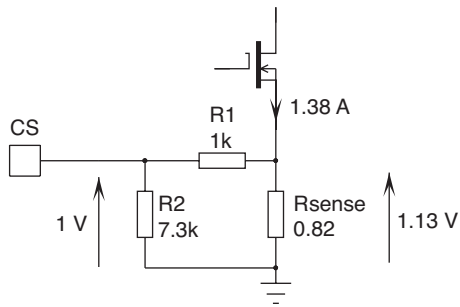

FIGURE 7-63 When a sense resistor requires a value difficult to find, it is always possible to install a divider which artificially increases the sensed voltage, at the cost of efficiency, however.

$$C_{clp} = \frac{k_c(V_{out} + V_f)}{NR_{clp}F_{sw}\Delta V} = \frac{1.5 \times 12.6}{0.166 \times 15.5k \times 65k \times 11} \approx 10\,\text{nF} \tag{7-163}$$

In the above equations:

L_{leak} is the leakage inductance. We selected 1% of the primary inductance for the example. Of course, you would measure it on the transformer prototype, representative of the production series.

ΔV is the selected ripple in percentage of the clamp voltage; 11 V roughly corresponds to 10% of the clamp voltage (≈114 V).

Finally, the power dissipated in the clamp resistor will guide us through the resistor selection:

$$P_{R_{clp}} = 0.5F_{sw}L_{leak}I_{peak}{}^2\frac{k_c}{k_c - 1} = 0.5 \times 65k \times 4.5u \times 1.38^2 \times \frac{1.5}{0.5} = 835\,\text{mW} \tag{7-164}$$

To dissipate 1 W, two 33 kΩ, 1 W resistors in parallel will do.

Having defined what we have on the primary side, let us look at the diode. Given N, we can calculate the secondary diode voltage stress:

$$\text{PIV} = NV_{bulk,max} + V_{out} = 0.166 \times 375 + 12 = 74\,\text{V} \tag{7-165}$$

With a k_d coefficient of 0.5 (diode derating factor), select a diode featuring a 150 V V_{RRM} and accepting at least 4 A of continuous current. An MBRS4201T3 in an SMC package (surface mount) looks like the good choice:

$V_{RRM} = 200$ V
$I_{F,avg} = 4$ A
$V_f = 0.61$ V at $T_j = 150$ °C and $I_{F,avg} = 4$ A
$I_R = 800$ μA at $T_j = 150$ °C and $V_r = 74$ V

The total power dissipation endured by this component is related to its dynamic resistance R_d, its forward drop V_f, and its leakage current (in particular for a Schottky). Total losses are

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defined by

$$P_d = V_f I_{d,avg} + R_d I_{d,rms}^2 + DI_R\text{PIV} \tag{7-166}$$

In our case, with such a derating factor for the reverse voltage, we can neglect the leakage current contribution as it brings very little additional losses. Also, at these small rms currents, the dynamic resistor contributes to almost nothing. Hence, Eq. (7-166) simplifies to

$$P_d = V_f I_{d,avg} = 0.61 \times 1.6 \approx 1\,\text{W} \tag{7-167}$$

Dissipating 1 W on an SMC package can represent a challenge, especially if you cannot benefit from a wide copper area on the board layout. If this is the case, a TO-220 diode such as the MBR20200 (industry standard) can easily dissipate 1 W in free-air conditions, without heat sink [Eq. (7-152)] and could be adopted instead. You could argue that a Schottky diode is not a necessity in this DCM example. A fast diode can also do the job, at the expense of a slightly higher forward drop.

As we have seen in the numerous design examples, we first calculated the capacitor value to obtain the right ripple value (considering the capacitive contribution alone), but the ESR always degraded the result. This time, being in DCM, we should directly evaluate the maximum ESR we can accept to pass the ripple condition of 250 mV. The secondary peak current can be known via the primary peak current and the transformer turns ratio:

$$I_{sec,peak} = \frac{I_{peak}}{N} = \frac{1.26}{0.166} = 7.6\,\text{A} \tag{7-168}$$

Based on this number,

$$R_{ESR} \leq \frac{V_{ripple}}{I_{sec,peak}} \leq \frac{0.25}{7.6} \leq 33\,\text{m}\Omega \tag{7-169}$$

Searching a capacitor manufacturer site (Rubycon, for example), we found the following reference:

680 μF − 16 V − YXG series
Radial type, 10 (φ) × 16 mm
R_{ESR} = 60 mΩ at T_A = 20 °C and 100 kHz
$I_{C,rms}$ = 1.2 A at 100 kHz

Associating several of these capacitors in parallel, we should reach the required equivalent series resistor. Now, keep in mind that the ESR increases as the temperature decreases. To keep the ripple at the right value at low temperatures, you might need to increase the total capacitor value, relax the original specification, or install a small output *LC* filter, as we will see later on. What is the rms current flowing through the parallel combination?

$$I_{C_{out,rms}}{}^2 = I_{sec,rms}^2 - I_{out,avg}^2 \tag{7-170}$$

The secondary side current requires the use of Eq. (7-151) where the off time now enters the picture:

$$I_{sec,rms} = I_{sec,peak}\sqrt{\frac{1 - D_{max}}{3}} = 7.6 \times \sqrt{\frac{1 - 0.42}{3}} = 3.34\,\text{A} \tag{7-171}$$

Substituting this result into Eq. (7-170) gives

$$I_{C_{out,rms}} = \sqrt{3.34^2 - 1.66^2} = 2.9\,\text{A} \tag{7-172}$$

In other words, three 680 μF capacitors have to be put in parallel to accept the above rms current, assuming they share the current equally. The total ESR drops to

$$R_{ESR,\,total} = \frac{60m}{3} = 20\,\text{m}\Omega \tag{7-173}$$

The loss incurred by this resistive path amounts to

$$P_{C_{out}} = I_{C_{out},rms}{}^2 R_{ESR} = 2.9^2 \times 20m = 168\,\text{mW} \tag{7-174}$$

Given all these results, it is time to look at the small-signal response. Using our flyback current-mode template, we can feed it with the calculated values:

$L_p = 450\ \mu\text{H}$
$R_{sense} = 0.7\ \Omega$
$N = 0.166$
$C_{out} = 2040\ \mu\text{F}$
$R_{ESR} = 20\ \text{m}\Omega$
$R_{load} = 7.2\ \Omega$

The application circuit appears in Fig. 7-64 where you can see a TL431 arranged as a type 2 amplifier.

What bandwidth do we need to satisfy our 250 mV drop as expressed in the initial specification?

$$f_c \approx \frac{\Delta I_{out}}{2\pi_c \Delta V_{out} C_{out}} = \frac{1.8}{6.28 \times 0.25 \times 2040u} = 562\,\text{Hz} \tag{7-175}$$

Let us shoot for 1 kHz, a reasonable value to reach also giving us some margin. The steps to follow in order to stabilize a DCM current-mode appear below:

1. The bridge divider calculation assumes a 250 μA current and a 2.5 V reference (TL431). Thus

$$R_{lower} = \frac{2.5}{250u} = 10\,\text{k}\Omega \tag{7-176a}$$

$$R_{upper} = \frac{12 - 2.5}{250u} = 38\,\text{k}\Omega \tag{7-176b}$$

2. Open-loop sweeps the current-mode flyback at the lowest input level (90 Vdc). Make sure the optocoupler pole and its CTR are properly entered to compensate for its presence. The laboratory measurement gave 6 kHz with a CTR varying from 50% to 150%. Figure 7-65 shows the results. In this example, we considered an optocoupler pull-up resistor of 20 kΩ (as in the NCP1200 series, for instance).

3. From the Bode plot, we can see that the required gain at 1 kHz is around +20 dB worst case. The phase lag at this point is −88°.

4. The *k* factor gives good results for the DCM compensation. Its recommendations are the following for a 1 kHz bandwidth and a targeted 60° phase margin:

$R_{LED} = 3\ \text{k}\Omega$
$C_{pole} = 2.2\ \text{nF}$
$C_{zero} = 15\ \text{nF}$

Once applied, Fig. 7-66 shows the compensated gain curves at both input voltages. Further sweeps of ESRs and CTR do not show compensation weaknesses. Do not forget to remove the

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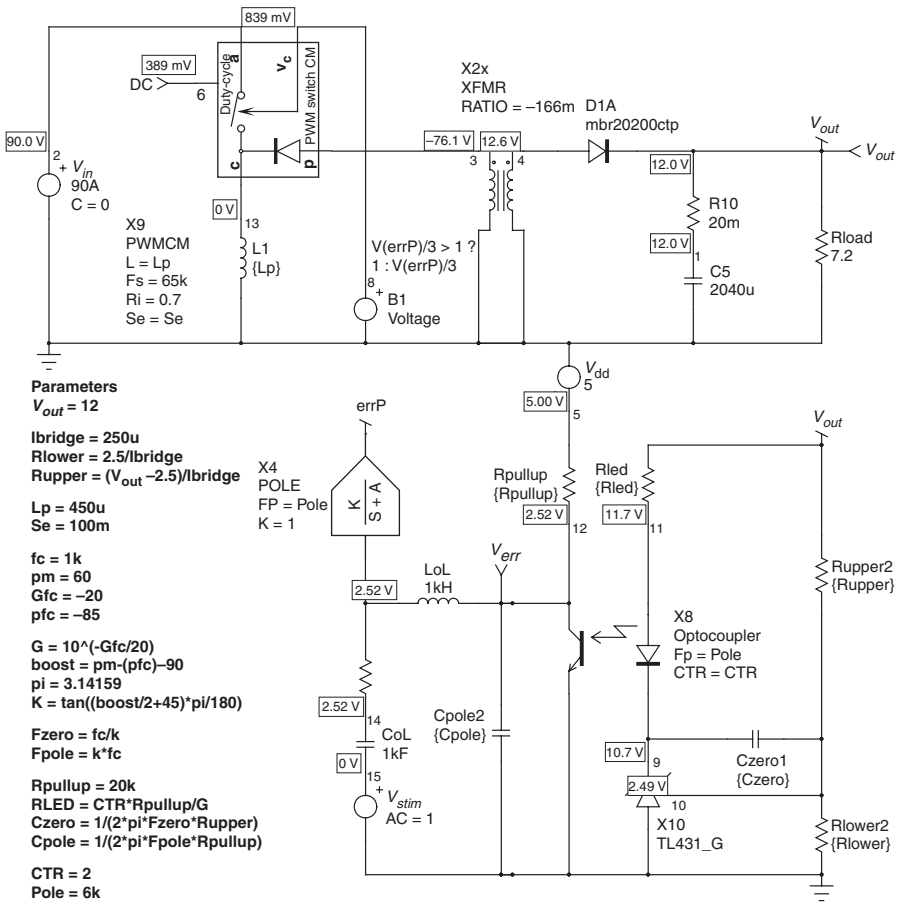

FIGURE 7-64 The ac configuration of the 20 W converter where the optocoupler pole takes place.

optocoupler pole X_4 before running the compensated ac sweeps (see Chap. 3 for more details)! When the board stability is confirmed via a load step on the average template, we can use the current-mode generic model already described in previous chapters. The cycle-by-cycle circuit appears in Fig. 7-67. The optocoupler is wired as an emitter follower, and the external voltage source mimics an internal 5 V V_{dd}. This is the most popular feedback implementation available on numerous controllers. Note the presence of a 300 mV source in series with the optocoupler collector to get rid of the saturation voltage occurring in light-load conditions (remember the two diodes in series in our UC34X representation, Fig. 7-31a). We purposely added an auxiliary winding, assuming the controller needs some self-supply. Given the turns ratio relationship, we assume the auxiliary voltage will reach around 13 V, neglecting the leakage inductance contribution. Figure 7-68 gathers all the pertinent waveforms collected at low line, full power. As you can see, some of the amplitudes confirm our theoretical calculations except the secondary variables. Why? Because a few equations [Eq. (7-171)] assumed a conduction at the boundary between CCM and DCM where $D' = 1 - D$. However, the inductor value and loading conditions impose a more pronounced DCM mode where the dead time appearance bothers Eq. (7-171).

Figure 7-69 depicts the obtained ripple at the lowest input voltage for a 20 W loading. A peak-to-peak measurement confirms a ripple amplitude of 174 mV, in line with the original specification.

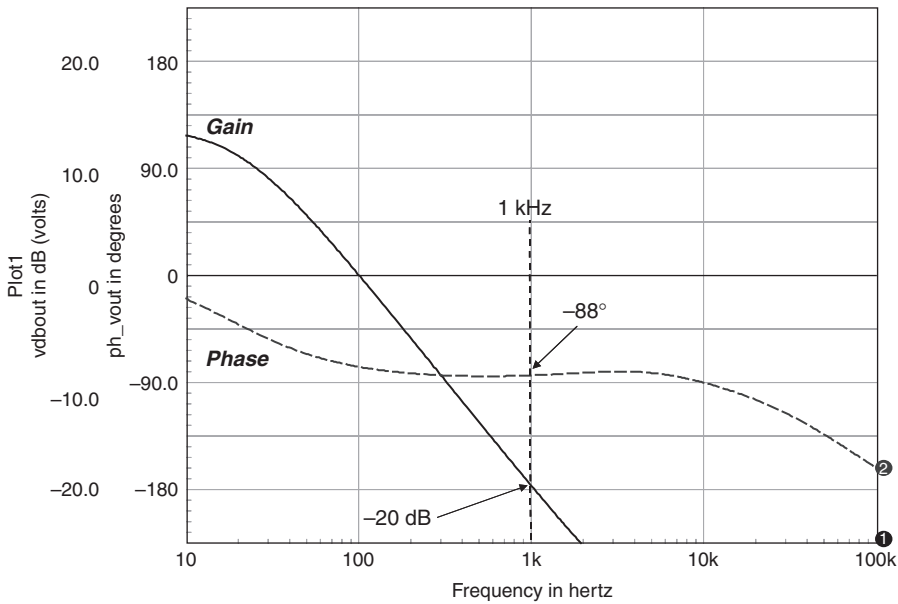

FIGURE 7-65 Open-loop Bode plots at the lowest input voltage, including the optocoupler pole and lowest CTR.

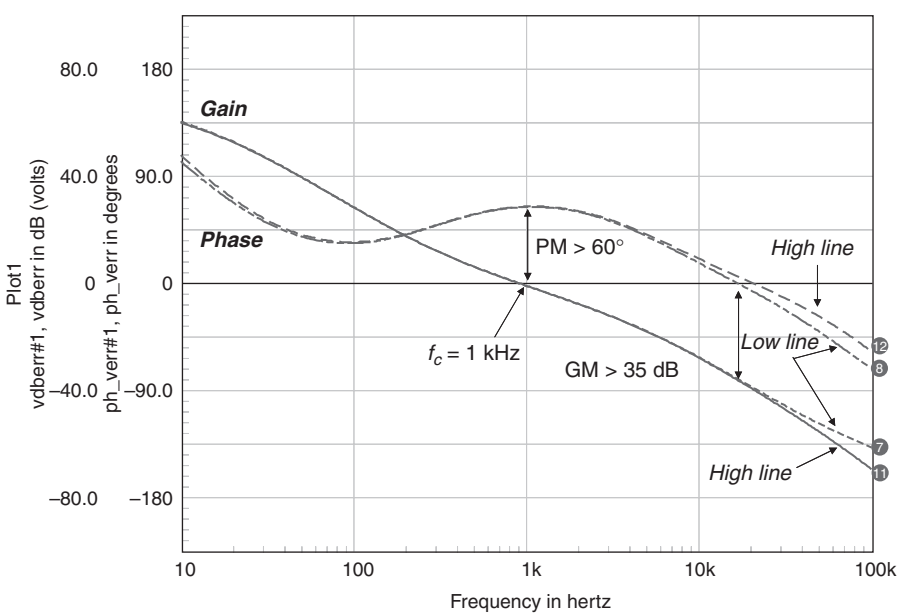

FIGURE 7-66 Once compensated, the Bode plot shows adequate bandwidth and phase margin at 1 kHz.

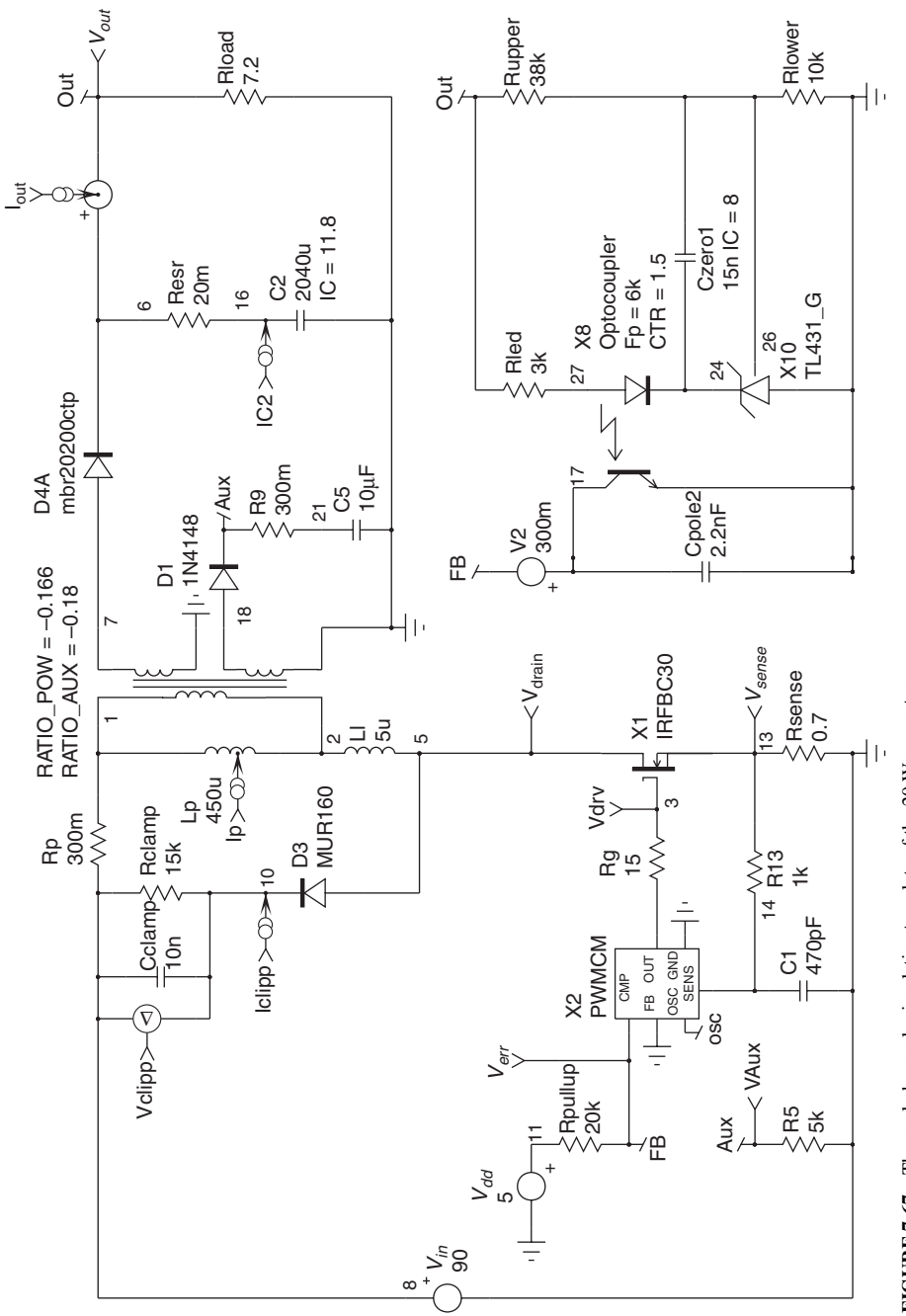

FIGURE 7-67 The cycle-by-cycle simulation template of the 20 W converter.

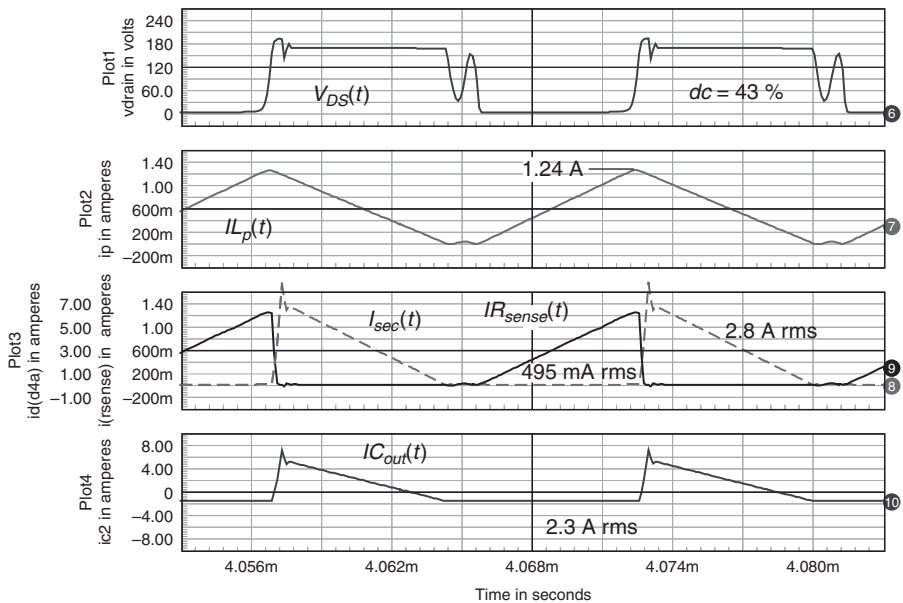

FIGURE 7-68 Cycle-by-cycle results on some pertinent waveforms (V_{in} = 90 Vdc).

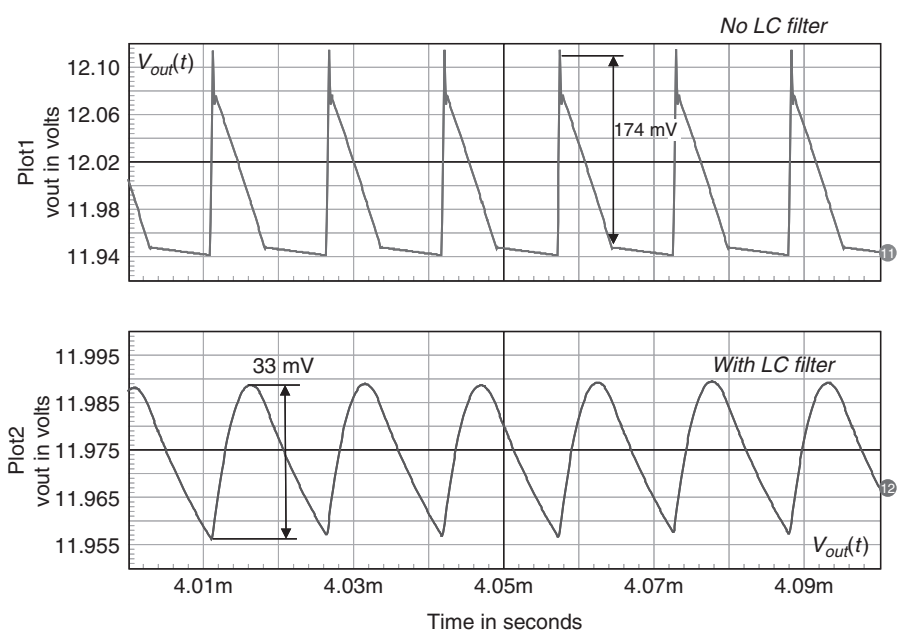

FIGURE 7-69 Output ripple full load, with and without a post *LC* filter.

However, there is almost no margin against unavoidable ESR variations. To improve the situation, we can install a small *LC* filter. The cutoff frequency of this filter must be well above the crossover frequency (at least 2 to 3 times) to avoid further stressing the phase at this point. Here, we put a 2.2 μH 100 μF filter, exhibiting a cutoff value of 10. 7 kHz, 10 times above 1 kHz. The capacitor does not see much ac ripple as all is undergone by the front-end capacitor C_2. Figure 7-70 shows how to wire the TL431: the fast lane (see Chap. 3) goes before the *LC* filter, whereas the R_{upper}/R_{lower} network connection remains unchanged. Failure to keep the fast lane connection as suggested would induce oscillations, given the high-frequency gain shown by this path. Figure 7-69 (lower curve) also portrays the ripple with the *LC* filter installed and shows a 33 mV peak-to-peak amplitude.

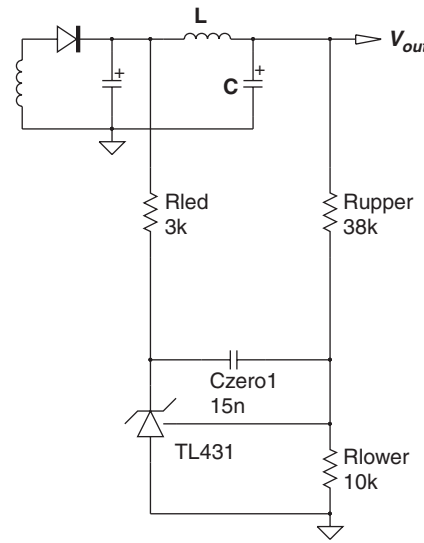

FIGURE 7-70 The insertion of an *LC* filter requires connection care with a TL431.

Finally, a step load confirms the good behavior of our simulated template, in both ac and transient modes (Fig. 7-71).

What controller can we select to build this converter? There are many to chose from. Given the low output power, an NCP1216 in DIP package (for improved thermal performance) from ON Semiconductor can easily do the job. Thanks to its high-voltage capability, there is no need for a transformer featuring an auxiliary winding: the controller is self-supplied by the high-voltage rail. The optocoupler directly connects to the feedback pin. Figure 7-72 portrays the application schematic. A few remarks regarding this implementation are appropriate:

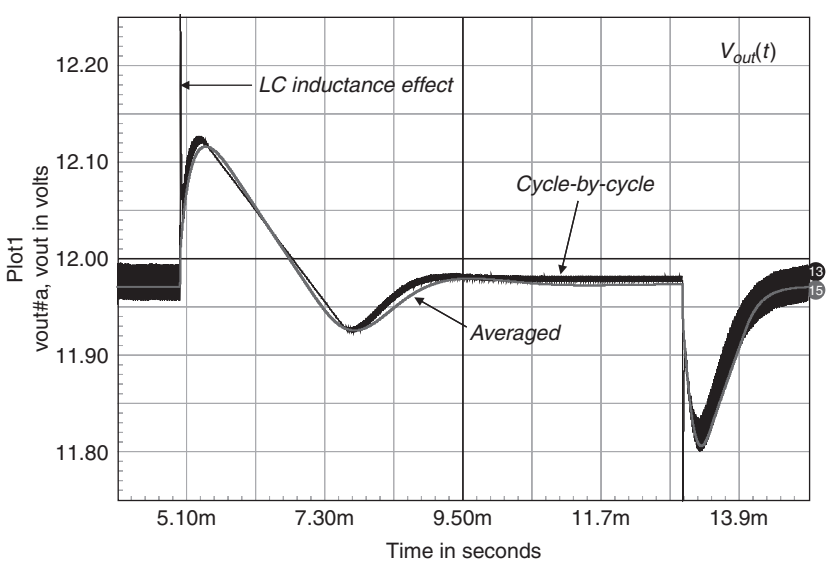

FIGURE 7-71 A 0.2 to 1.6 A load step test confirms the power supply stability at low line. See how the average model response superimposes on the cycle-by-cycle model response.

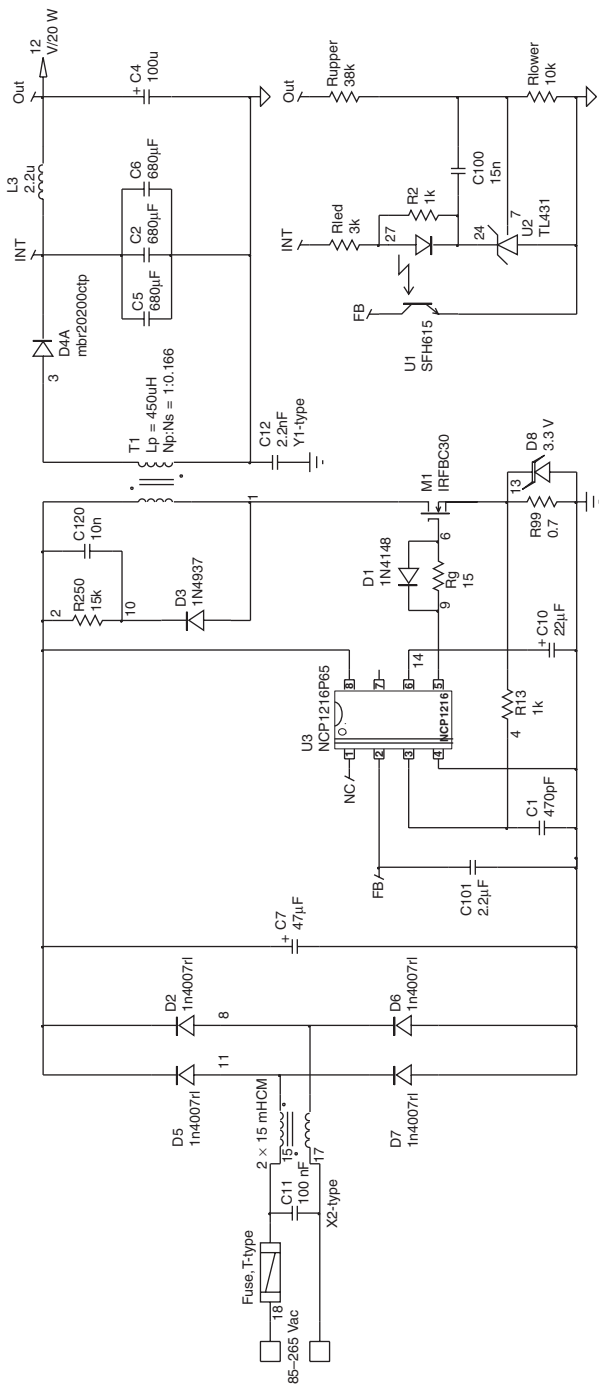

FIGURE 7-72 A typical implementation using a high-voltage controller from ON Semiconductor.

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- The input filter uses the leakage inductance of the common-mode inductors to create a differential mode section with C_7.
- The zener diode D_8 is often found on large-volume consumer products. Its role is to limit the controller current-sense pin voltage excursion in case of a drain–source short-circuit on the main MOSFET. Sometimes, two 1N4007s in series are placed there for increased ruggedness. As the MOSFET source is clamped by the diodes during the fault, the controller does not see a lethal level until the fuse blows. Experience shows that the controller is often spared, thanks to this trick.
- R_2 transforms the optocoupler LED in a constant-current generator ($\approx$1 V/1 kΩ). It provides the bias to the TL431. If we prefer a resistor wired from the TL431 cathode to V_{out}, this solution also works well.
- All capacitors such as C_{101}, C_1, C_{10}, and R_{13} must be placed as close as possible to the controller in order to improve the noise immunity.

For the transformer, there are two options:

1. You select a transformer manufacturer (Coilcraft, Pulse Engineering, Coiltronix, Vogt, Delta Electronics, etc.) and provide the following data:

L_p = 450 µH
$I_{Lp,max}$ = 1.5 A
$I_{Lp,rms}$ = 500 mA
$I_{sec,rms}$ = 3 A
F_{sw} = 65 kHz
V_{in} = 100 to 375 Vdc
V_{out} = 12 V at 1.6 A
N_p:N_s = 1:0.166

Based on this information, the manufacturer will be able to pick up the right core and discuss with you the winding arrangements, the pinout, etc. Ask for an impedance versus frequency plot for both the primary inductance and the leakage inductance. Watch for the inductance falloff as the temperature rises. It might hamper the power capability as the ambient temperature rises.

2. Take a look at App. 7C and follow the building instructions written by Charles Mullett.

7.14 A 90 W, SINGLE-OUTPUT POWER SUPPLY

This second design example describes a 90 W flyback converter operated on universal mains and featuring the following specifications:

$V_{in,min}$ = 85 Vrms
$V_{bulk,min}$ = 90 Vdc (considering 25% ripple on bulk capacitor)
$V_{in,max}$ = 265 Vrms
$V_{bulk,max}$ = 375 Vdc
V_{out} = 19 V
V_{ripple} = ΔV = 250 mV

V_{out} drop = 250 mV maximum from I_{out} = 0.5 to 5 A in 10 μs
$I_{out,max}$ = 5 A
T_A = 70 °C
MOSFET derating factor k_D = 0.85
Diode derating factor k_d = 0.5
RCD clamp diode overshoot V_{os} = 20 V

Given the power rating, we are going to design a converter operating in CCM, at least in the lower range of the input voltage. To design a CCM converter, we can either calculate the primary inductance to obtain a certain inductor ripple current at low line or select the voltage at which the converter leaves CCM to enter DCM. The second option offers greater flexibility to choose the operating mode at a selected input voltage. Before digging into the calculation details, we recall the inductor current when running in CCM. Figure 7-73 portrays the waveform.

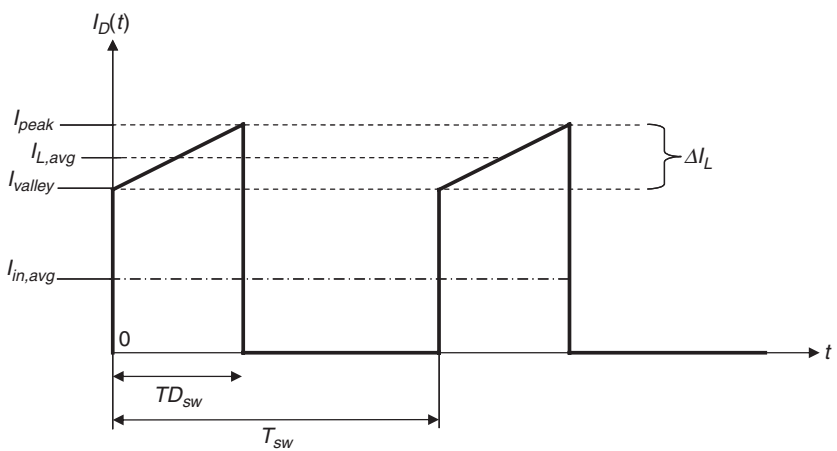

FIGURE 7-73 The inductor current in the continuous conduction mode.

Based on this signal, we derived a design equation, already introduced in Chap. 5 [Eq. (5-97)]:

$$L = \frac{\eta V_{bulk,min}{}^2 \left(\frac{V_{out} + V_f}{N}\right)^2}{\delta I_r F_{sw} P_{out} \left(V_{bulk,min} + \left(\frac{V_{out} + V_f}{N}\right)\right)\left(\left(\frac{V_{out} + V_f}{N}\right) + \eta V_{bulk,min}\right)} \tag{7-177}$$

In the above expression, the term δI_r defines the amount of ac peak-to-peak ripple across the inductor average current:

$$\delta I_r = \frac{\Delta I_L}{I_{L,avg}} \tag{7-178}$$

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and V_{min} illustrates the lowest dc input voltage on the bulk rail (refer to Fig. 6-4). The bulk capacitor will be calculated to let the bulk voltage drop to 90 Vdc.

When equal to 2, the converter runs in full discontinuous mode. Different notations also exist in the literature, for instance, found under K_{RF} in Ref. 9. Despite a 2 in the denominator (to have K_{RF} equal to 1 in DCM), the expression does not basically change. Experience shows that depending on the input voltage range, some δI_r values are recommended to obtain the best design tradeoff:

- For a universal mains design (85 to 265 Vrms), choose a δI_r between 0.5 and 1.
- For a European input range (230 Vrms ± 15%), choose a δI_r between 0.8 and 1.6.

Let us choose $\delta I_r = 0.8$ in this example.

We explained in the previous design the intimate relationship between the turns ratio and the maximum allowable MOSFET drain–source voltage. Again, we will select a 600 V MOSFET for the universal mains operations, together with a derating factor k_D of 0.85. Assuming a good transformer coupling, a k_c of 1.5 represents a reasonable number. Thus, the turns ratio must be larger than

$$N = \frac{k_c(V_{out} + V_f)}{BV_{dss}k_D - V_{os} - V_{bulk,max}} = \frac{1.5 \times (19 + 0.6)}{600 \times 0.85 - 20 - 375} = 0.255 \qquad (7\text{-}179)$$

Let us pick a turns ratio of 0.25 or $1/N = 4$. In the above equation, we assumed the diode forward drop to be 0.6 V. Applying Eq. (7-177), we find an inductor value of

$$L = \frac{0.85 \times 90^2 \times \left(\frac{19.6}{0.25}\right)^2}{0.8 \times 65k \times 90 \times \left[90 + \left(\frac{19.6}{0.25}\right)\right]\left[\left(\frac{19.6}{0.25}\right) + 0.85 \times 90\right]} \approx 320\,\mu\text{H} \qquad (7\text{-}180)$$

From Fig. 7-73, the inductor average current relates to the average input current via the following formula:

$$I_{in,avg} = I_{L,avg}D \qquad (7\text{-}181)$$

The maximum average input current depends on the lowest input voltage V_{min} and the delivered power:

$$I_{in,avg} = \frac{P_{out}}{\eta V_{min}} = \frac{90}{0.85 \times 90} = 1.18\,\text{A} \qquad (7\text{-}182)$$

The duty cycle in Eq. (7-181) obeys the flyback relationship:

$$D_{max} = \frac{V_{out}}{V_{out} + NV_{min}} = \frac{19}{19 + 0.25 \times 90} = 0.46 \qquad (7\text{-}183)$$

Introducing this result into Eq. (7-181) gives the average inductor current

$$I_{L,avg} = \frac{I_{in,avg}}{D_{max}} = \frac{1.18}{0.46} = 2.56\,\text{A} \qquad (7\text{-}184)$$

Based on these results, the salient points of Fig. 7-73 are easily derived:

$$\Delta I_L = I_{L,avg}\delta I_r = 2.56 \times 0.85 = 2.18\,\text{A} \qquad (7\text{-}185)$$

$$I_{peak} = I_{L,avg} + \frac{\Delta I_L}{2} = I_{L,avg}\left(1 + \frac{\delta I_r}{2}\right) = 2.56\left(1 + \frac{0.85}{2}\right) = 3.65\,\text{A} \tag{7-186}$$

$$I_{valley} = I_{L,avg} - \frac{\Delta I_L}{2} = I_{L,avg}\left(1 - \frac{\delta I_r}{2}\right) = 2.56\left(1 - \frac{0.85}{2}\right) = 1.47\,\text{A} \tag{7-187}$$

The primary rms current calculation requires the solution of a simple integral. As usual, the task consists of writing the time-dependent equation of the considered variable. In Fig. 7-73, the valley current ($t = 0$) is actually the peak current minus the ripple. At the end of the on time, the current reaches I_{peak}. The equations are thus

$$t = 0 \rightarrow I_{L_p}(t) = I_{valley} = I_{peak} - \Delta I_L \tag{7-188}$$

$$t = DT_{sw} \rightarrow I_{L_p}(t) = I_{valley} + \Delta I_L \tag{7-189}$$

$$I_{L_p}(t) = I_{valley} + \Delta I_L \frac{t}{DT_{sw}} = I_{peak} - \Delta I_L + \Delta I_L \frac{t}{DT_{sw}} \tag{7-190}$$

After integration of Eq. (7-190), it becomes

$$I_{L,rms} = \sqrt{\frac{1}{T_{sw}} \int_0^{DT_{sw}} \left(\frac{\Delta I_L t}{DT_{sw}} + I_{peak} - \Delta I_L\right)^2 dt} = \sqrt{D\left(I_{peak}{}^2 - I_{peak}\Delta I_L + \frac{\Delta I_L{}^2}{3}\right)} \tag{7-191}$$

Injecting Eqs. (7-183), (7-185), and (7-186) results in Eq. (7-191) gives the final rms current circulating in the transformer primary, the MOSFET, and the sense resistor:

$$I_{L,rms} = \sqrt{D_{max}\left(I_{peak}{}^2 - I_{peak}\Delta I_L + \frac{\Delta I_L{}^2}{3}\right)}$$

$$= \sqrt{0.46\left(3.58^2 - 3.58 \times 2.18 + \frac{2.18^2}{3}\right)} \approx 1.8\,\text{A} \tag{7-192}$$

Given the rms current, we can try to find a suitable MOSFET. For a 90 W output power, there is no way a MOSFET without heat sink can survive in an ambient temperature of 70 °C. Try to find low-$R_{DS(on)}$ devices, such as the following:

Reference	Manufacturer	$R_{DS(on)}$	BV_{DSS}	Q_G
2SK2545	Toshiba	0.9 Ω	600 V	30 nC
2SK2483	Toshiba	0.54 Ω	600 V	45 nC
STB11NM60	ST	0.45 Ω	650 V	30 nC
STP10NK60Z	ST	0.65 Ω	650 V	70 nC
SPP11N60C3	Infineon	0.38 Ω	650 V	60 nC
SPP20N60C3	Infineon	0.19 Ω	650 V	114 nC

Pay attention to the package (an isolated full-pack version is simpler to mount on a heat sink than a nonisolated type) but also to the total gate charge. As the MOSFET becomes bigger (a lot of primary cells in parallel), the amount of gate charge significantly increases and so does the average driving current delivered by the controller. Let us pick an SPP11N60C3 from Infineon, a popular model in ac–dc adapters. The conduction losses at a junction temperature

of 110 °C are

$$P_{cond} = I_{D,rms}{}^2 R_{DS(on)} @ T_j = 110\,°\text{C} = 1.8^2 \times 0.6 \approx 2\,\text{W} \tag{7-193}$$

The switching losses now account for the turn-on term made up of the lump capacitive discharge (already present in DCM) and the current–voltage overlap. This time, the current jumps to the valley term and no longer starts from zero. Figure 7-74a depicts the typical CCM waveforms.

As in the DCM example, a real-case waveform was captured in Fig. 7-74b. The gate-source voltage starts to increase until the plateau level is reached. At that time, the drain voltage falls and the current rises as the MOSFET operates in a linear manner. The driver signal has complete control over the signal steepness, and a resistor can be inserted to slow down this sequence on both variables. It was not the case in the turn-off event where the inductor acted as a constant-current source, imposing the drain voltage slope via the lump capacitor. In CCM, slowing down the turn-on event reduces the secondary side stress for the diode which is abruptly blocked. The resulting spike on the primary side reduces in amplitude and the radiated EMI greatly improves. If we consider a crossing point in the middle of the waveforms, Eq. (7-156b) still holds, except that we should consider the new variables in play at the switch closing time:

- $V_{DS}(t)$ transitions from the plateau voltage to zero
- $I_D(t)$ transitions from zero to the valley level

If we consider Δt the overlap time, switching losses at turn-on are thus

$$P_{SW,on} = \frac{I_{valley}\left(V_{bulk} + \dfrac{V_{out} + V_f}{N}\right)\Delta t}{6} F_{sw} \tag{7-194}$$

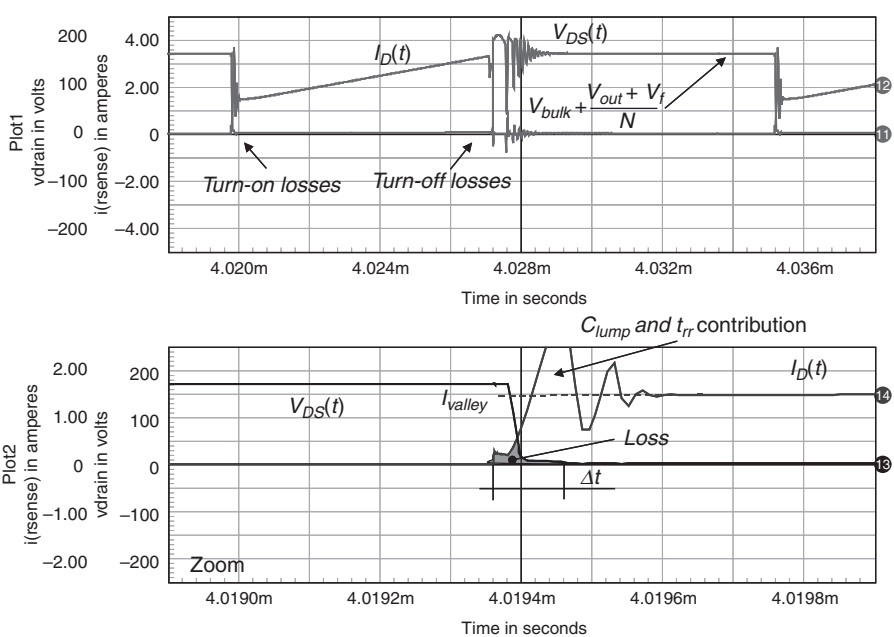
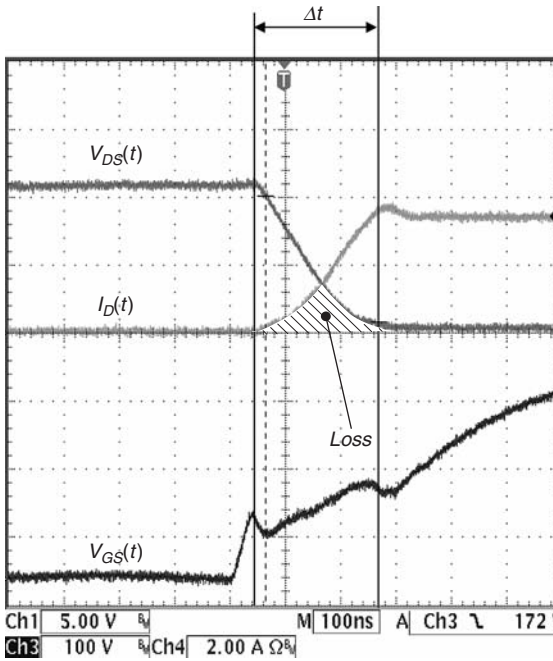


FIGURE 7-74a A simulated typical turn-on sequence in a CCM flyback converter.



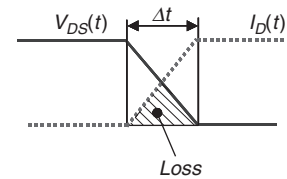


FIGURE 7-74b A real-case turn-on sequence on a CCM converter.

These losses consider a crossing time at the middle of both curves which, in reality, often differs from this ideal case. Again, bench measurements are mandatory to check the total power dissipation budget. Note that measurements will include the lump capacitor and the secondary diode t_{rr} contributions (if any).

The off-time losses still obey Eq. (7-156b). Finally, the MOSFET will dissipate.

$$P_{MOSFET} = P_{cond} + P_{SW,on} + P_{SW,off} \tag{7-195}$$

Based on Eq. (7-193), and without knowing the outcome of Eq. (7-195), our MOSFET will need a heat sink.

The total gate charge of the SPP11NC60C3 amounts to 60 nC. Therefore, the power dissipated by the driver (and not the MOSFET!) when supplied by a 15 Vdc source (the auxiliary V_{cc} voltage) reaches

$$P_{drv} = F_{sw}Q_GV_{cc} = 65k \times 60n \times 15 = 59\,\text{mW} \tag{7-196}$$

As for the DCM example, let us assume the controller considers a current limit when the voltage image of the primary current reaches 1 V. Therefore, the sense resistor value is evaluated by

$$R_{sense} = \frac{1}{I_{peak}} \tag{7-197}$$

We need a peak current of 3.6 A. Considering a design margin of 10% (I_{peak} = 4 A), the sense resistor value equals

$$R_{sense} = \frac{1}{4} = 0.25\,\Omega \tag{7-198}$$

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Given this value and the rms current, the power dissipation of this element amounts to

$$P_{sense} = I_{D,rms}{}^2 R_{sense} = 1.8^2 \times 0.25 = 810\,\text{mW} \tag{7-199}$$

Two 0.5 Ω, 1 W SMD types wired in parallel will do.

The MOSFET protection goes along with clamping elements calculations. The below expressions unveil the resistor and capacitor values by using familiar definitions:

$$R_{clp} = \frac{(k_c - 1)\left[2k_c(V_{out} + V_f)^2\right]}{N^2 F_{sw} L_{leak} I_{peak}{}^2} = \frac{(1.5 - 1)\left[2 \times 1.5 \times (19 + 0.6)^2\right]}{0.25^2 \times 65k \times \dfrac{320u}{100} \times 3.65^2} \approx 3.4\,\text{k}\Omega \tag{7-200}$$

$$C_{clp} = \frac{k_c(V_{out} + V_f)}{N R_{clp} F_{sw} \Delta V} = \frac{1.5 \times 19.6}{0.25 \times 3.4k \times 65k \times 12} \approx 44.3\,\text{nF} \tag{7-201}$$

In the above equations:

L_{leak} is the leakage inductance. We selected 1% of the primary inductance for the example. Of course, you would measure it on the transformer prototype, representative of the production series.

ΔV is the selected ripple in percentage of the clamp voltage; 12 V roughly corresponds to 10% of the clamp voltage (≈117 V).

Finally, the power dissipated in the clamp resistor is

$$P_{R_{clp}} = 0.5 F_{sw} L_{leak} I_{peak}{}^2 \frac{k_c}{k_c - 1} = 0.5 \times 65k \times 3.2u \times 3.65^2 \times \frac{1.5}{0.5} \approx 4\,\text{W} \tag{7-202}$$

To dissipate 4 W, three 10 kΩ, 2 W resistors in parallel will behave ok. Given the converter power, use an ultrafast device such as the MUR160 for the clamp diode rather than a slower diode.

Now, the secondary side diode. The peak inverse voltage needs to be assessed before a selection can be made:

$$\text{PIV} = N V_{bulk,max} + V_{out} = 0.25 \times 375 + 19 = 112.8\,\text{V} \tag{7-203}$$

As usual, with a diode voltage derating factor k_d of 50%, select a diode featuring a 200 V V_{RRM} and accepting at least 10 A. (Its average current is nothing more than the direct output current.) An MBR20200CT in a TO-220 package could be a possible choice.

$V_{RRM} = 200$ V
$I_{F,avg} = 20$ A (two diodes inside, each accepting 10 A)
$V_f = 0.8$ V maximum at $T_j = 125$ °C and $I_{F,avg} = 10$ A
$I_R = 800$ μA at $T_j = 150$ °C and $V_r = 80$ V

The total power dissipation endured by this component is related to its dynamic resistance R_d, its forward drop V_f, and its leakage current (in particular for a Schottky). Total losses are defined by

$$P_d = V_f I_{d,avg} + R_d I_{d,rms}{}^2 + D I_R \text{PIV} \tag{7-204}$$

In our case, the leakage current does not bring significant losses, so we will neglect it. Hence, for each diode, Eq. (7-204) simplifies to

$$P_d = V_f I_{d,avg} = 0.8 \times 2.5 \approx 2\,\text{W} \tag{7-205}$$

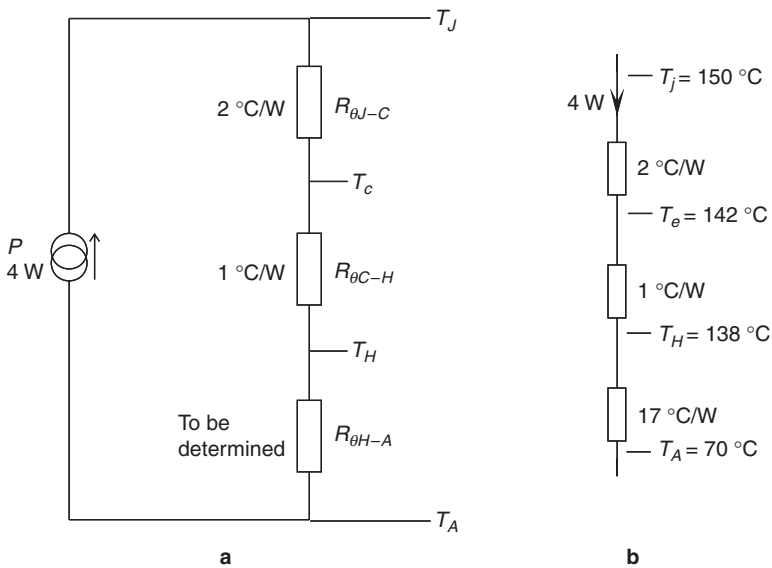

FIGURE 7-75a, b The power can be pictured as a current source feeding thermal resistances in series.

In the above equation, we assumed an equal current sharing between both diodes as they sit on the same die. The total power dissipation is thus twice what Eq. (7-205) states: 4 W. A heat sink is necessary. Figure 7-75a and b portrays the electrical analogy between thermal resistance and resistors. A thermal resistance of 5 °C/W means that the component temperature rises by 5 °C for each watt you put in. The equivalent ohm law still applies, and we can write

$$T_j - T_A = P(R_{\theta J-C} + R_{\theta C-H} + R_{\theta H-A}) \tag{7-206}$$

where T_j and T_A = junction and ambient temperatures, respectively
$R_{\theta J-C}$ = thermal resistance between junction and component case. It is usually around a few degrees Celsius per watt (2 °C/W here)
$R_{\theta C-H}$ = thermal resistance between case and heat sink. If you use a good isolator and grease, less than 1 °C/W is achievable
$R_{\theta H-A}$ = thermal resistance between heat sink and ambient air. This is what you are looking for to select the right type
P = power to be dissipated

The maximum junction temperature depends on several parameters among which the mold compound (the black powder the component is made of) plays a role. For an MBR20200 diode, you can safely limit the maximum temperature to 150 °C ($T_{j,max}$ for the MBR20200 is 175 °C). From Eq. (7-206), we can extract the thermal resistance our heat sink will need to exhibit to maintain the diode junction temperature below 150 °C when it is immersed into an ambient temperature of 70 °C:

$$R_{\theta H-A} = \frac{T_{j,max} - T_A}{P} - R_{\theta J-C} - R_{\theta C-H} = \frac{150 - 70}{4} - 2 - 1 = 17\ °C/W \tag{7-207}$$

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Our diode junction when operated at a 70 °C ambient temperature will thus theoretically increase up to

$$T_j = T_A + PR_{\theta J-A} = 70 + 4 \times (17 + 1 + 2) = 150\,°C \tag{7-208}$$

Once the prototype is assembled, make sure all heat sink temperatures are controlled and comply with your QA recommendations. Some state that all heat sink temperatures must be below 100 °C at the maximum ambient temperature. As Fig. 7-75b shows, we would fail to meet this recommendation and a larger heat sink would be necessary (7.5 °C/W with a junction working at 88 °C).

If for various reasons (cost, reverse voltage, and so on) we could not select a Schottky diode, how would the reverse recovery time impact the diode dissipation budget? It is necessary to understand the diode blocking phenomenon via a simple drawing, as Fig. 7-76 offers [10]. In this figure, we have highlighted several timing intervals. Let us comment on them, one by one:

1. At t_1, the power MOSFET has been switched on, and the diode begins its blocking process. The slope at which the current decays is imposed by the external circuit, mainly the inductance in the mesh.
2. At the beginning of t_a, the diode behaves as a short-circuit, and the charge stored when the diode was conducting (more precisely, a remaining portion since recombination did evacuate

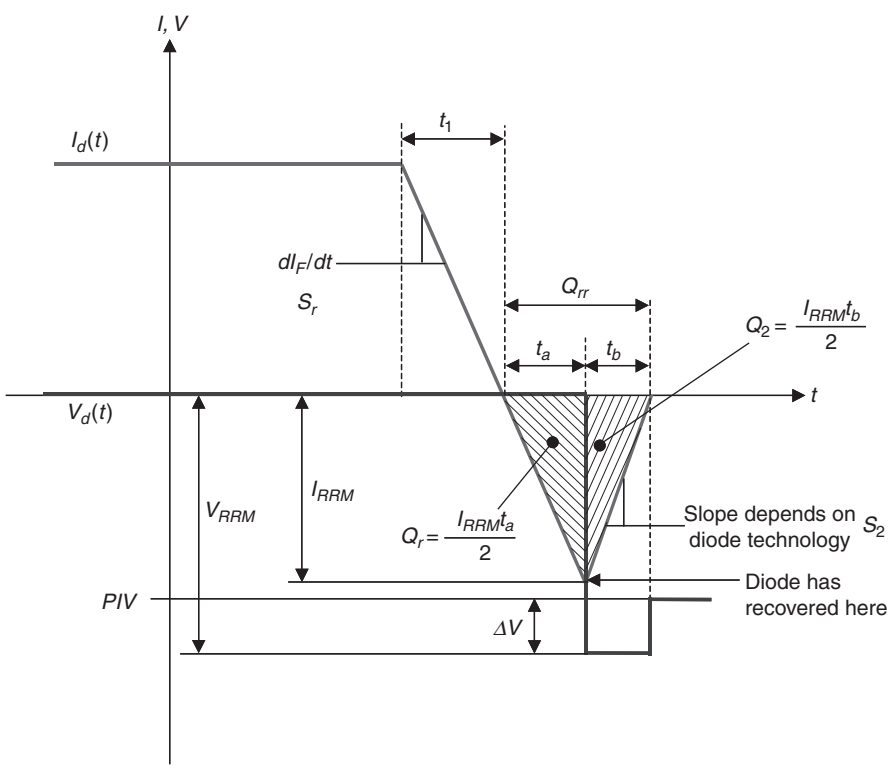

FIGURE 7-76 The diode in a blocking configuration.

a bit of it already) is evacuated via a negative current I_{RRM}. The current amplitude is linked to the blocking slope imposed by the external circuit: the steeper the imposed slope is, the more negative I_{RRM} swings.

$$S_r = -\frac{dI_F}{dt} = -\frac{\text{PIV}}{L} \tag{7-209}$$

3. At the end of t_a, the charge is fully evacuated (Q_r on the drawing) and the diode is going to recover its blocking capability. It must bring a negative charge $-Q_2$ in order to reconstruct the internal barrier.
4. The current quickly decreases to zero via a slope S_2, and a voltage spike occurs across the diode terminals (sudden opening of the circuit). The amplitude of this spike depends on I_{RRM} and the speed at which the current goes back to zero (t_b duration, slope S_2). This speed depends on the technology. One talks about the diode "softness." The softness is actually defined by the ratio t_b/t_a. Diodes can recover in an abrupt, soft, or snappy way, generating more or fewer spikes, ringing, and other EMI unfriendly goodies.
5. Diode specifications state the reverse recovery time t_{rr}, the peak recovery current I_{RRM}, and the total charge Q_{rr} made of Q_r plus Q_2. All these parameters are defined at a given current slope dI_F/dt. It is interesting to note that Q_{rr} increases as the junction temperature goes up (the minority carrier lifetime increases). For instance, a 30EPH06 from International-Rectifier exhibits a Q_{rr} of 65 nC at $T_j = 25$ °C and climbs up to 345 nC for $T_j = 125$ °C!

In the above picture, the power dissipated by the diode appears during the interval t_b:

$$P_{t_b} = F_{sw} V_{RRM} \frac{t_b I_{RRM}}{2} = F_{sw} V_{RRM} Q_2 \tag{7-210}$$

The spike brought by the inductor in the circuit during t_b can be classically evaluated via

$$\Delta V = L \frac{dI_F}{dt} = L S_2 \tag{7-211}$$

Based on Fig. 7-76, the total voltage excursion V_{RRM} can thus be rewritten

$$V_{RRM} = \text{PIV} + L S_2 \tag{7-212}$$

If we divide all terms of Eq. (7-212) by the PIV, and by observing the inverse of S_r [Eq. (7-209)], we obtain

$$\frac{V_{RRM}}{\text{PIV}} = 1 + \frac{LS_2}{\text{PIV}} = 1 + \frac{S_2}{S_r} \tag{7-213}$$

Now, if we define the slopes according to their respective variables, we have

$$\frac{V_{RRM}}{\text{PIV}} = 1 + \frac{\dfrac{I_{RRM}}{t_b}}{\dfrac{I_{RRM}}{t_a}} = 1 + \frac{I_{RRM}}{t_b}\frac{t_a}{I_{RRM}} = 1 + \frac{Q_r}{Q_2} \tag{7-214}$$

From Eq. (7-214), we can extract V_{RRM} and replace it in Eq. (7-210):

$$P_{d,t_{rr}} = F_{sw}\text{PIV}\left(1 + \frac{Q_r}{Q_2}\right)Q_2 = F_{sw}\text{PIV}(Q_r + Q_2) = F_{sw}\text{PIV}Q_{rr} \tag{7-215}$$

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The t_{rr}-related losses are difficult to predict since they depend on the blocking slope, temperature, and diode technology itself. Also, few manufacturers give details on these parameters, making the exercise even more difficult. Final temperature assessment in the worst-case environment is thus mandatory to verify the junction stays within a reasonable value.

Now that we are done with the semiconductor portion, let us discuss the capacitor selection. As for the DCM design, we consider the ESR as the dominant term. The secondary peak current needs to be known before proceeding:

$$I_{sec,peak} = \frac{I_{peak}}{N} = \frac{3.6}{0.25} = 14.4\,\text{A} \tag{7-216}$$

Based on this number,

$$R_{ESR} \leq \frac{V_{ripple}}{I_{sec,peak}} \leq \frac{0.25}{14.4} \leq 17\,\text{m}\Omega \tag{7-217}$$

Searching a capacitor manufacturer site (Vishay), we found the following reference:

2200 μF − 25 V − 135 RLI series
Radial type, 12.5 (φ) × 40 mm
R_{ESR} = 44 mΩ ay T_A = 20 °C and 100 kHz
$I_{C,rms}$ = 2 A at 100 kHz and 105 °C

Placing several of these capacitors in parallel, we should reach the required equivalent series resistor. Now, keep in mind that the ESR increases as the temperature goes down. To keep the ripple at the right value at low temperatures, you might need to increase the total capacitor value, relax the original specification, or install a small output *LC* filter as we will see later on. What is the rms current flowing through the parallel combination?

$$I_{C_{out,rms}}{}^2 = I_{sec,rms}{}^2 - I_{out,avg}{}^2 \tag{7-218}$$

The secondary side current requires the use of Eq. (7-192) where the off time now matters:

$$\begin{aligned} I_{sec,rms} &= \sqrt{(1 - D_{max})\left(I_{sec,peak}{}^2 - I_{sec,peak}\frac{\Delta I_L}{N} + \frac{\Delta I_L{}^2}{N^2 3}\right)} \\ &= \sqrt{(1 - 0.46)\left(14.4^2 - 14.4 \times \frac{2.18}{0.25} + \frac{2.18^2}{0.25^2 \times 3}\right)} = 7.6\,\text{A} \end{aligned} \tag{7-219}$$

Putting this result into Eq. (7-218) gives

$$I_{C_{out,rms}} = \sqrt{7.6^2 - 4.7^2} \approx 6\,\text{A} \tag{7-220}$$

Given the individual rms capability of each capacitor (2 A at 105 °C), we need to put three of them in parallel for a total capability of 6 A. A final bench measurement at the minimum input voltage and maximum current will indicate if the capacitor temperature is within safe limits or not. Given the association of capacitors, the equivalent series resistor drops to

$$R_{ESR,total} = \frac{44m}{3} = 14.6\,\text{m}\Omega \tag{7-221}$$

The total loss incurred by this resistive path amounts to

$$P_{C_{out}} = I_{C_{out},rms}{}^2 R_{ESR} = 6^2 \times 14.6m = 525\,\text{mW} \tag{7-222}$$

Since all our elements are designed, it is time to look at the small-signal response of this converter. The current-mode template can be fed with the following data:

$L_p = 320\ \mu H$
$R_{sense} = 0.25\ \Omega$
$N = 0.25$
$C_{out} = 6600\ \mu F$
$R_{ESR} = 14.6\ m\Omega$
$R_{load} = 4\ \Omega$

Figure 7-77 portrays the application schematic which does not differ from that of the DCM example since the model autotoggles between both modes. The display of operating points confirms the behavior of the simulated circuit (V_{out} = 19 V, duty cycle = 46.7%). For the sake of simplicity, we kept the same optocoupler parameters as in the DCM design.

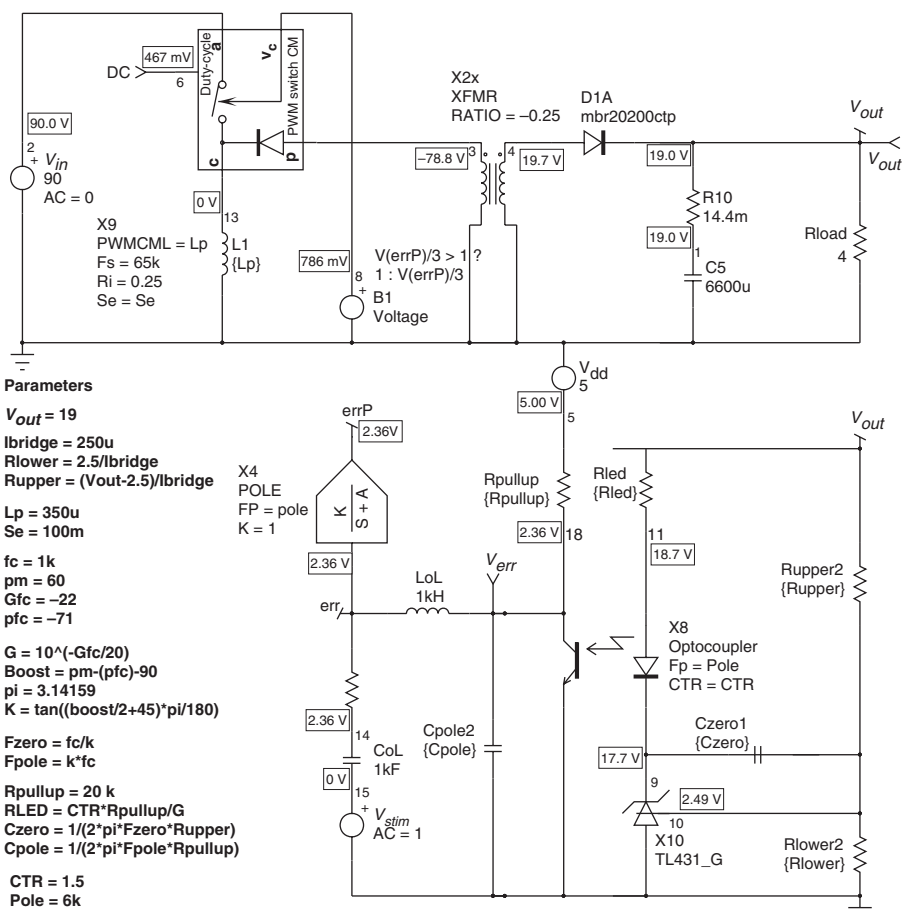

FIGURE 7-77 The CCM converter uses the same current-mode template as for the DCM case.

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What bandwidth do we need to satisfy the 250 mV drop as expressed in the initial specification?

$$f_c \approx \frac{\Delta I_{out}}{2\pi_c \Delta V_{out} C_{out}} = \frac{4.5}{6.28 \times 0.25 \times 6600u} = 434\,\text{Hz} \tag{7-223}$$

Let us select 1 kHz, a reasonable value to reach, also giving us some margin within the recommendation of Eq. (7-223). Is the right half-plane zero far enough to avoid this associated phase lag?

$$f_{z_2} = \frac{(1 - D)^2 R_{load}}{2\pi D L_p N^2} = \frac{(1 - 0.46)^2 \times 4}{6.28 \times 0.46 \times 320u \times 0.25^2} = 20.2\,\text{kHz} \tag{7-224}$$

The answer is yes, we are operating at a crossover frequency located below the 20% of the RHPZ location. What about the converter peaking, since we operate in CCM with a duty cycle close to 50%?

$$Q = \frac{1}{\pi\left(D'\frac{S_e}{S_n} + \frac{1}{2} - D\right)} = \frac{1}{3.14 \times (0.5 - 0.46)} = 8 \tag{7-225}$$

This result suggests that we damp the subharmonic poles to bring the quality coefficient below 1. Extracting the S_e parameter (the external ramp amplitude) leads to

$$\begin{aligned} S_e &= \frac{S_n}{D'}\left(\frac{1}{\pi} - 0.5 + D\right) = \frac{V_{in} R_i}{L_p D'}\left(\frac{1}{\pi} - 0.5 + D\right) \\ &= \frac{90 \times 0.25}{320u \times (1 - 0.46)}\left(\frac{1}{3.14} - 0.5 + 0.46\right) = 36\,\text{kV/s} \end{aligned} \tag{7-226}$$

We will see the effects of this external ramp and how to practically generate it. The steps to follow to stabilize a CCM current-mode appear below:

1. The bridge divider calculation assumes a 250 μA current and a 2.5 V reference (TL431). Thus

$$R_{lower} = \frac{2.5}{250u} = 10\,\text{k}\Omega \tag{7-227a}$$

and

$$R_{upper} = \frac{19 - 2.5}{250u} = 66\,\text{k}\Omega \tag{7-227b}$$

2. Open loop sweeps the current-mode flyback at the lowest input level (90 Vdc). Make sure the optocoupler pole and its CTR are properly entered to compensate for its presence. The laboratory measurement gave 6 kHz with a CTR varying from 50 to 150%. Figure 7-78 unveils the results. In this example, we considered an optocoupler pull-up resistor of 20 kΩ (as in the NCP1200 series, for instance).
3. From the Bode plot, we can see that the required gain at 1 kHz is around +22 dB worst case. The phase lag at this point is −71°.
4. The *k* factor gives good results for the current-mode CCM compensation, generally speaking for first-order behaviors. Its recommendations are the following for a 1 kHz bandwidth and a targeted 80° phase margin:

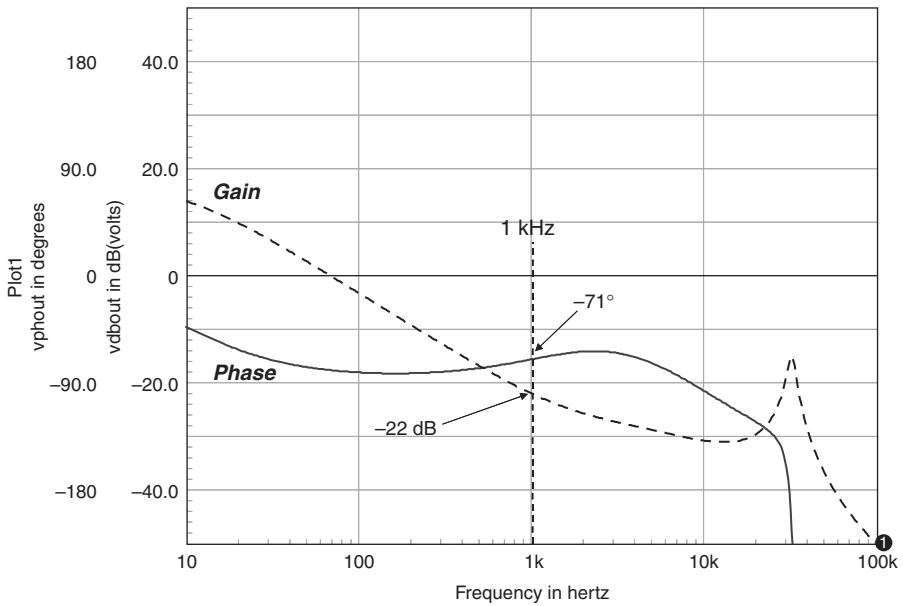

FIGURE 7-78 The ac sweep of the CCM current mode does not reveal any large phase discontinuity, except in the vicinity of the double subharmonic pole.

$R_{LED} = 2.4\ \text{k}\Omega$
$C_{pole} = 2.2\ \text{nF}$
$C_{zero} = 10\ \text{nF}$

Once applied, Fig. 7-79 shows the compensated gain curves at both input voltages. Further sweeps of ESRs and CTR do not show compensation weaknesses. As usual, do not forget to remove the optocoupler pole X_4 before running the compensated ac sweeps (see Chap. 3 for more details)! The simulation reveals a peaking due to the CCM operation and a duty cycle close to 50% at low line, but the associated gain margin seems reasonable. We have then added some ramp compensation from 10 to 30 kV/s, and results appear in the inset graph. A 20 kV compensation looks good enough for our converter. Increasing the ramp level too much could degrade the peak current capability and would prevent the power supply from delivering its full power at low line. Once compensation values are adopted, you can sweep the ESRs between the minimum and the maximum stated in the capacitor data sheets to check that the converter remains stable.

After the ac analysis comes the cycle-by-cycle simulation to verify our assumptions about the voltage and current variables and the stability. Figure 7-80 portrays the transient simulation template we have used. Note the presence of the secondary side *LC* filter which removes all the ESR-related spikes.

To add ramp compensation, we have implemented the Fig. 7-81 solution (introduced by Virginia Tech 20 years ago). It offers excellent noise immunity as it does not touch any oscillator section. You can select the various elements of the ramp generator as you need; we found that the *RC* values of 18 kΩ and 1 nF gave good results for 65 kHz operation. If we make the ramp resistance high enough, constant-current charge equations can thus be used with reasonable accuracy. Hence, referring to Fig. 7-81, we find

$$I_{C_1} = \frac{V_{drv,high}}{R_2} = \frac{15}{18k} = 800\,\mu\text{A} \tag{7-228}$$

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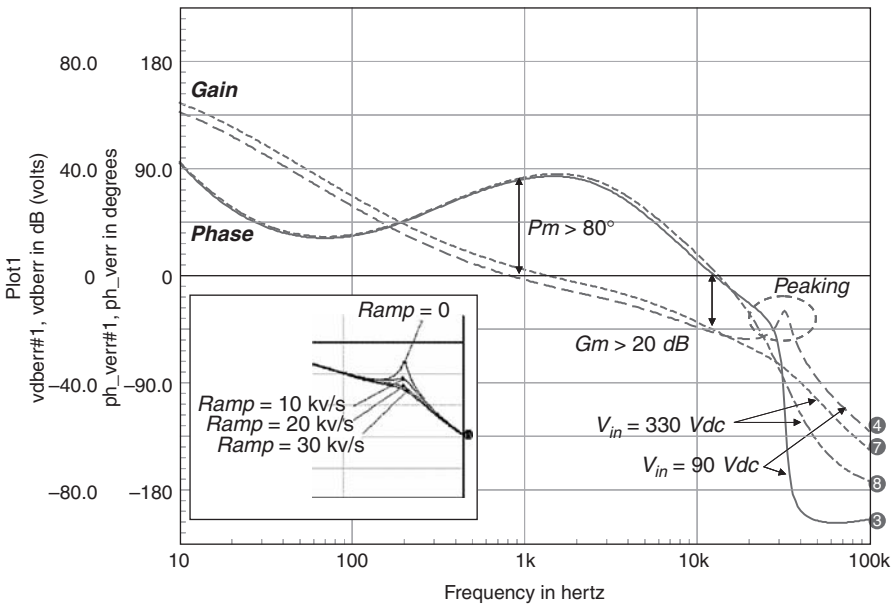

FIGURE 7-79 Once compensated, the converter exhibits a comfortable phase margin at both input levels. The lower left frame shows the effect of ramp compensation on the peaking. A value of 20 kV/s seems to suffice in this case.

For a 0.46 duty cycle and a 15.4 μs switching period, the on-time duration is 7 μs. Thus, the voltage across C_1 ramps up to

$$V_{C_1} = \frac{I_{C_1} t_{on,max}}{C_1} = \frac{800u \times 7u}{1n} = 5.6\,\text{V} \tag{7-229}$$

Its voltage slope is then

$$S_{ramp} = \frac{V_{peak}}{t_{on,max}} = \frac{5.6}{7u} = 800\,\text{kV/s} \tag{7-230}$$

Applying Eq. (5-39) with the above data leads to a ramp resistor of

$$R_{ramp} = \frac{S_{ramp}}{S_e} R_3 = \frac{800k}{20k} 1k = 80\,\text{k}\Omega \tag{7-231}$$

This value is inserted into the Fig. 7-80 simulation. Except the ramp compensation circuit, the application file does not differ that much from the DCM example. Of course, you could replace the generic controller by a real model, but the simulation time would suffer. We recommend to test the whole configuration (check turns ratio, currents, and so on) using a fast model; then, once everything is within limits, you can try a more comprehensive model. Note the presence of the secondary *LC* filter, again inserted to reduce the high-frequency ripple.

As shown by Fig. 7-82, the valley and peak currents on the primary side have smaller values than the ones theoretically calculated. This can be explained by an overall better efficiency compared to the 85% we selected in the original calculation. On SPICE, the MOSFET $R_{DS(on)}$ stays constant despite a higher junction temperature. For instance, the efficiency measurement gives 91%, a rather good value. The MOSFET total loss amounts to 1.3 W, and the diode losses are 3 W.

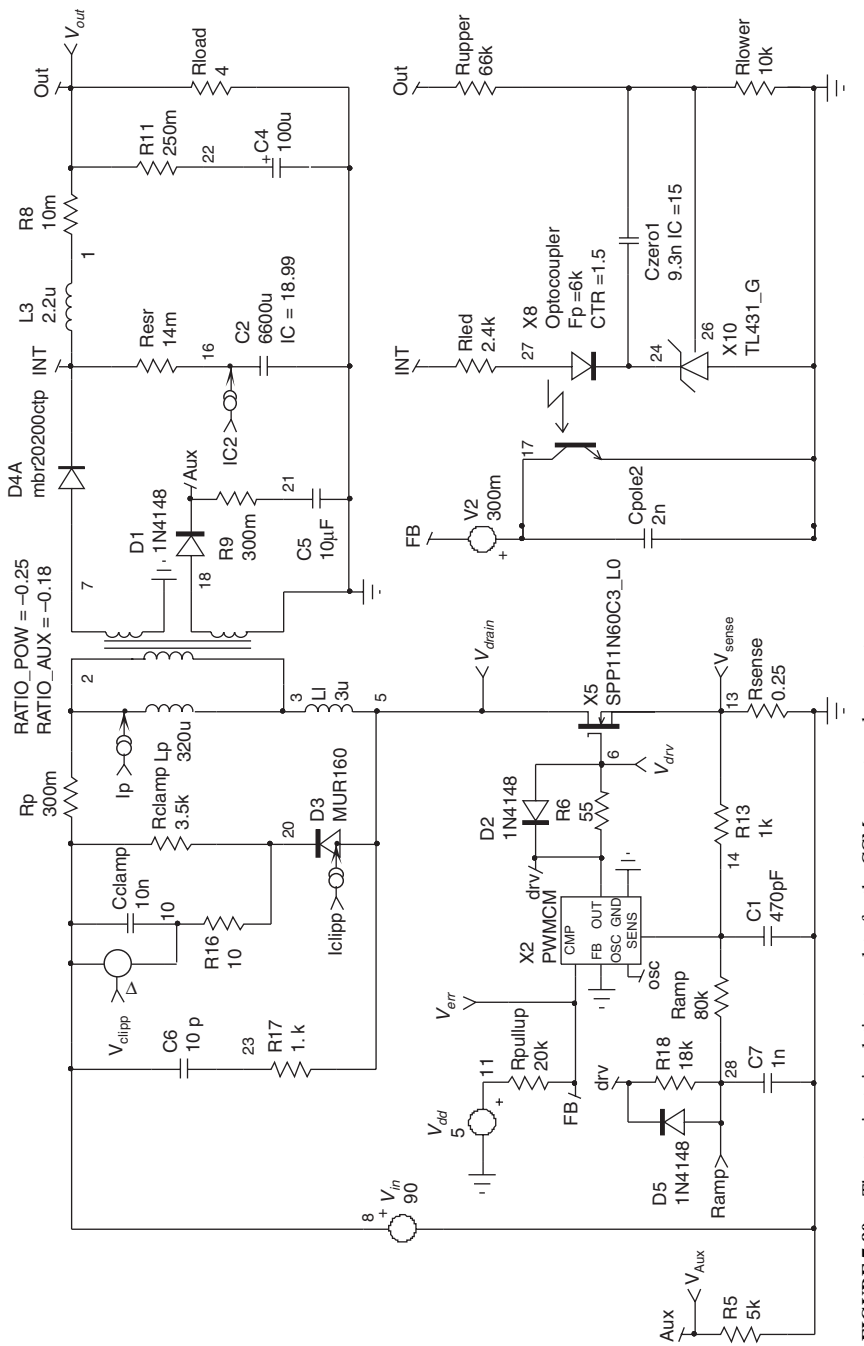

FIGURE 7-80 The transient simulation template for the CCM current-mode converter.

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In this particular example, selecting the components based on the pure theoretical values gives a good design margin from the beginning. Be careful, though, when selecting capacitors with a small margin or without any margin at all, for this can quickly lead to catastrophic failures in production given the dispersions: take margins!

Figure 7-83 portrays the voltage excursion on the MOSFET drain for the highest input voltage (375 V) and shows us that the *RCD* clamp network was properly selected. In the laboratory, if you missed something in this calculation, the power-on sequence usually triggers an ovation in the surrounding audience. In SPICE, all stays quiet (no fireworks!) if you exceed the breakdown voltage and you can discretely readjust values to match your target!

Finally, a load step confirms the compensation calculations by showing an output voltage drop of 100 mV at 90 Vrms (Fig. 7-84).

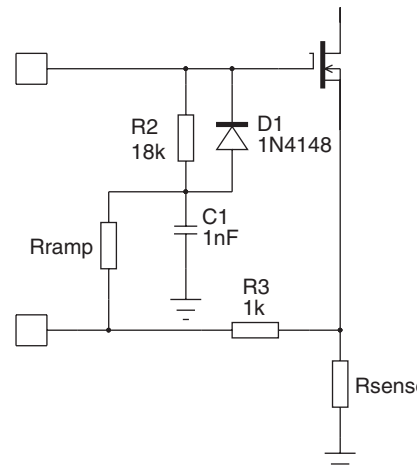

FIGURE 7-81 Deriving the ramp signal from a low-impedance path such as the driver pin is a good way to build the compensation waveform.

The application schematic uses an NCP1230 from ON Semiconductor (Fig. 7-85). This controller includes a lot of interesting features such as a fault timer which offers excellent short-circuit protection, even if the coupling between the auxiliary and the power winding suffers (feedback observation, see Fig. 7-47). Also, given the 90 W output power, if you decide to

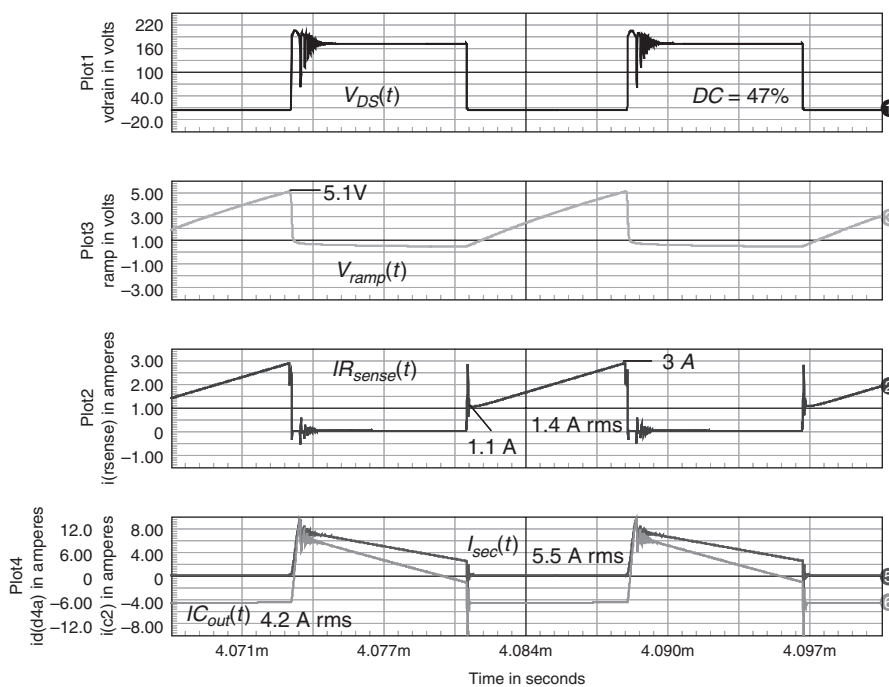

FIGURE 7-82 Simulation results from the Fig. 7-80 template.

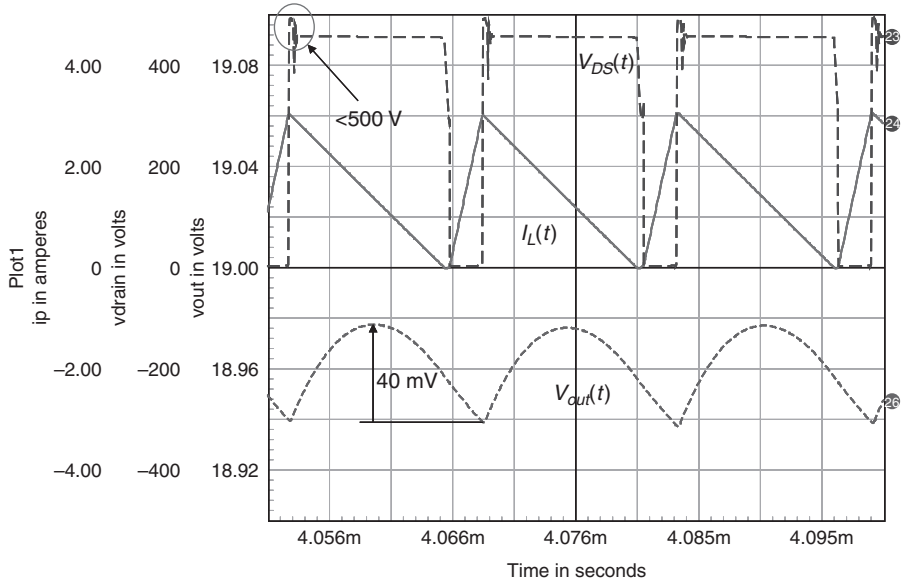

FIGURE 7-83 Drain-source voltage at 375 V of input voltage and maximum load. The diode overshoot does not appear, but as it usually corresponds to 15 to 30 V, there is a lot of margin until 600 V.

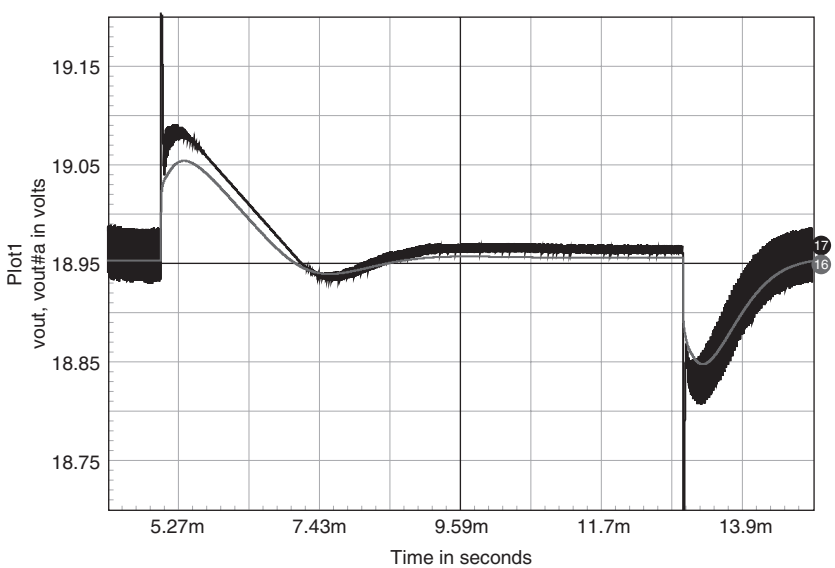

FIGURE 7-84 The transient response shows a converter under control, leading to a drop of roughly 100 mV.

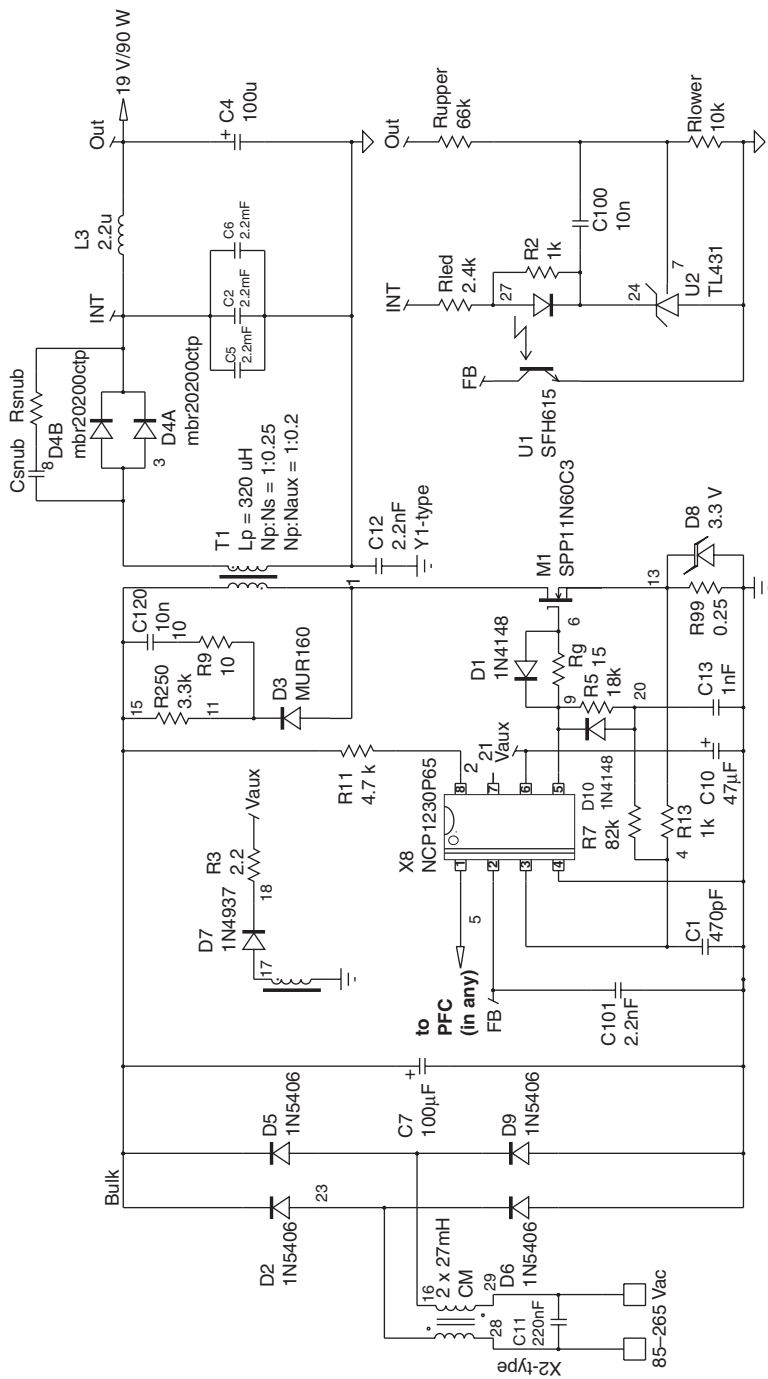

FIGURE 7-85 The final application schematic where the controller includes a V_{cc} for a PFC, if one is installed.

include a PFC front-end stage, then the 1230 can directly shut down the PFC in standby, further saving power. The power supply must still be designed to operate on wide mains (to start up when the PFC is off in low mains condition), but it must thermally be designed for high line only (when the PFC is on). The schematic includes provisions for a snubber installed across the secondary side diode, as ringing often occurs at this location.

The transformer design requires the knowledge of the following data that can be either sent to a transformer manufacturer or used to build the transformer yourself, sticking to the design example available in App. 7C.

L_p = 320 μH
$I_{Lp,max}$ = 4 A
$I_{Lp,rms}$ = 1.8 A
$I_{sec,rms}$ = 8 A
F_{sw} = 65 kHz
V_{in} = 90 to 375 Vdc
V_{out} = 19 V at 4.7 A
N_p:N_s = 1:0.25
N_p:N_{aux} = 1:0.2

7.15 A 35 W, MULTIOUTPUT POWER SUPPLY

This third design example describes a 35 W flyback converter operated on universal mains and featuring the following specifications:

$V_{in,min}$ = 85 Vrms
$V_{bulk,min}$ = 90 Vdc (considering 25% ripple on bulk capacitor)
$V_{in,max}$ = 265 Vrms
$V_{bulk,max}$ = 375 Vdc
V_{out1} = 5 V ± 5%, $I_{out,max}$ = 2 A
V_{out2} = 12 V ± 10%, $I_{out,max}$ = 2 A
V_{out3} = –12 V ± 10%, $I_{out,max}$ = 0.1 A
V_{ripple} = ΔV = 250 mV on all outputs
T_A = 50 °C
MOSFET derating factor k_D = 0.85
Diode derating factor k_d = 0.5

This power supply could suit a consumer product, such as a set-top box, a VCR, or a DVD recorder. Of course, more outputs would be necessary, but this example can be easily translated to other needs. In this application, we are going to use quasi-square wave resonance (so-called QR mode). Why? Because

1. The power supply always operates in DCM, so it is easier to stabilize.
2. You can thus select inexpensive "lazy" diodes, so there are no t_{rr}-related problems.
3. If you switch in the valley, you reduce C_{lump} losses and can sometimes purposely increase this capacitor to get rid of an expensive *RCD* clamp.
4. Secondary side synchronous rectification sees benefits from the guaranteed DCM operation.

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On the other side, the drawbacks of the QR operation are as follows:

1. The operating frequency varies in relation to the input and output conditions.
2. The frequency increases in light-load conditions, as do switching losses.
3. A frequency clamp or an active circuitry must be installed to limit the frequency excursion in light-load conditions; otherwise standby losses can be extremely important.
4. DCM operation incurs higher rms currents compared to the CCM mode.
5. In the lowest line and heaviest loading conditions, the frequency can decrease and enter the audible range, causing acoustical noise troubles.

Despite these drawbacks, a lot of ac–dc adapters and set-top box makers use the QR mode to improve the overall efficiency, mainly thanks to synchronous rectification. To design a QR converter, we must first understand the various signals present in the flyback operated in this mode and derive an equation to design the primary inductor. As usual, the design starts with the turns ratio definition. In a QR design, you strive to reflect a large amount of voltage to the primary side to bring the wave valley (when the secondary diode blocks) as close as possible to the ground. Thus all losses linked to the drain lump capacitor are minimized, if not totally canceled ($V_{DS} = 0$). For this reason, designers often select an 800 BV_{DSS} type of MOSFET to allow maximum reflection.

In moderate power designs, such as this one, it is possible to connect an additional capacitor between drain and source to actually reduce the voltage excursion at the switch opening [see Eq. (7-17) and Fig. 7-5c]. If a sufficient margin exists, then goodbye costly *RCD* clamp! For this reason, the diode overshoot parameter (V_{os}) and k_c disappear from our turns ratio definition to the benefit of a new variable, V_{leak}. Variable V_{leak} corresponds to the voltage excursion brought by the leakage inductance and the capacitor connected between drain and source C_{DS}:

$$V_{leak} = I_{peak}\sqrt{\frac{L_{leak}}{C_{DS}}} \tag{7-232}$$

Figure 7-86 depicts a typical signal captured on a QR converter where no *RCD* clamp has been wired.

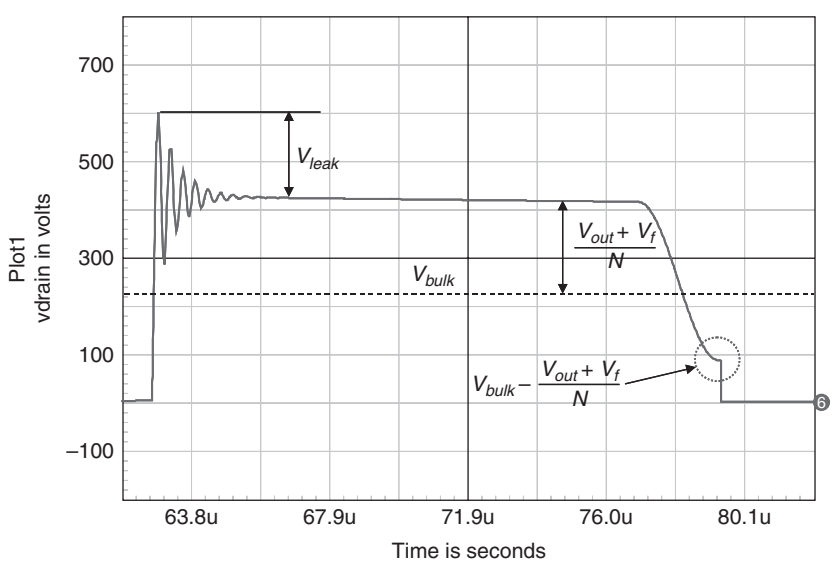

FIGURE 7-86 A QR waveform where the maximum excursion depends on the leakage inductor and the capacitor wired between drain and source.

To take into account this additional parameter, the turns ratio definition can be updated as follows:

$$N = \frac{V_{out} + V_f}{BV_{DSS}k_D - V_{bulk,max} - V_{leak}} \tag{7-233}$$

Let us look now at the primary inductor signals. Figure 7-87 depicts the current flowing in a flyback inductor when operated in QR or borderline mode. One interesting thing, already

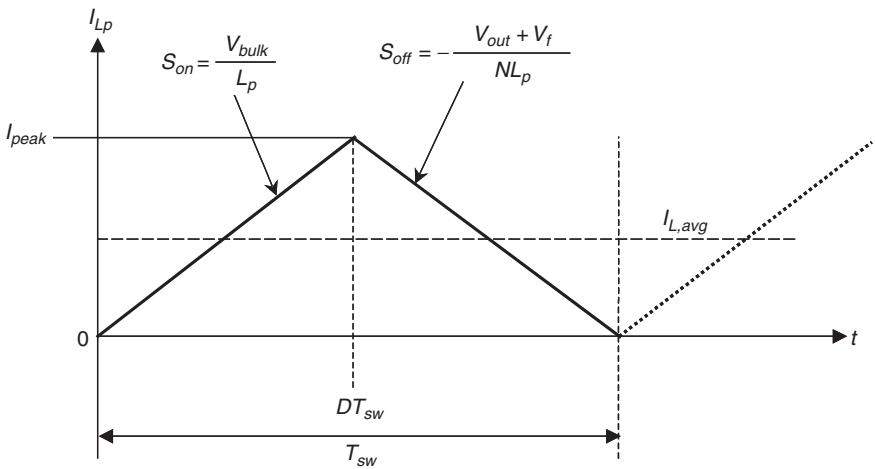

FIGURE 7-87 The inductor current in the borderline mode operation.

highlighted in the PFC section, relates to the inductor average current when QR is employed in the flyback converter:

$$I_{L,avg} = \frac{I_{peak}}{2} \tag{7-234}$$

Looking at the input current, Fig. 7-88 shows how it evolves with time. The average value delivered by the source becomes

$$I_{in,avg} = \frac{I_{peak}D}{2} \tag{7-235}$$

To derive the inductor equations, let us use the slope definitions in Fig. 7-87 to find the on- and off-time durations:

$$t_{on} = I_{peak}\frac{L_p}{V_{bulk}} \tag{7-236}$$

$$t_{off} = I_{peak}\frac{NL_p}{V_{out} + V_f} \tag{7-237}$$

As the converter operates in BCM, the DCM power conversion formula perfectly holds:

$$P_{out} = \frac{1}{2}L_p I_{peak}^2 F_{sw}\eta \tag{7-238}$$

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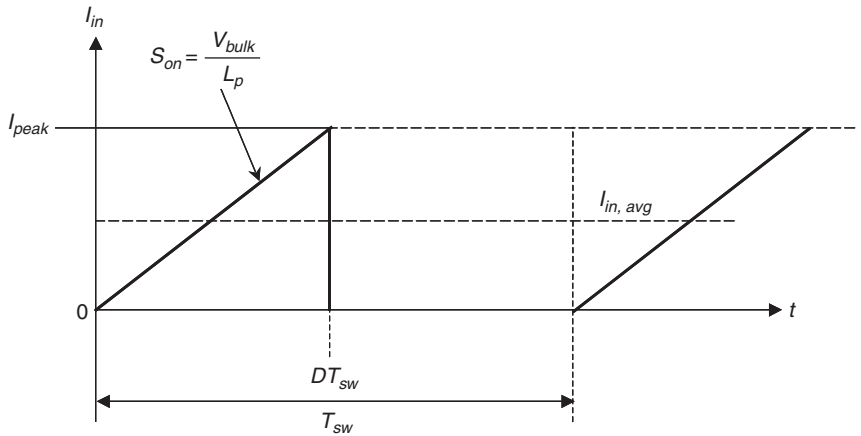

FIGURE 7-88 The input current (or drain current) in the borderline mode operation.

From this we can extract the peak current definition:

$$I_{peak} = \sqrt{\frac{2P_{out}}{F_{sw}L_p\eta}} \tag{7-239}$$

If we sum up Eqs. (7-236) and (7-237) to obtain the switching frequency, further replacing the peak current by the Eq. (7-239) definition, we have

$$\frac{1}{F_{sw}} = t_{on} + t_{off} = \sqrt{\frac{2P_{out}}{F_{sw}L_p\eta}}\,L_p\left(\frac{1}{V_{bulk}} + \frac{N}{V_{out} + V_f}\right) \tag{7-240}$$

As the minimum frequency occurs when the bulk voltage is minimum (low line), then extracting the switching frequency and the inductor leads to

$$L_p = \frac{\eta(V_{out} + V_f)^2 V_{bulk,min}{}^2}{2P_{out}F_{sw,min}(V_{out} + V_f + NV_{bulk,min})^2} \tag{7-241}$$

$$F_{sw,min} = \frac{\eta(V_{out} + V_f)^2 V_{bulk,min}{}^2}{2P_{out}L_p(V_{out} + V_f + NV_{bulk,min})^2} \tag{7-242}$$

where $F_{sw,min}$ represents the minimum switching frequency at low line ($V_{bulk,min}$) and full power. Equation (7-242) shows how the frequency varies:

- Full load, the frequency is minimum and can enter the audible range. Conduction losses are prominent over switching losses.
- Light load, the frequency quickly increases and degrades the efficiency by switching loss contribution.

Figure 7-89 portrays the typical frequency evolution versus load variations for a QR converter.

The next step consists of assessing the rms current, worst case again, low line and full power. The formula remains similar to the one used in the DCM design:

$$I_{D,rms} = I_{peak}\sqrt{\frac{D_{max}}{3}} \tag{7-243}$$

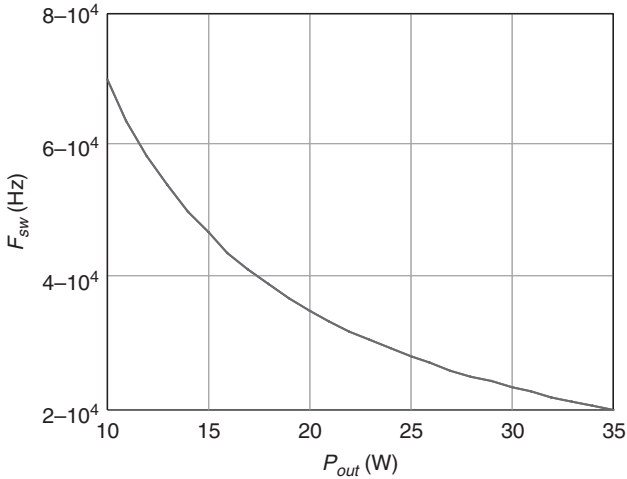

FIGURE 7-89 As the load changes, the frequency also adjusts to keep the DCM mode.

To derive the duty cycle, Eq. (7-235) can be tweaked:

$$\frac{P_{out}}{V_{bulk,min}\eta} = \frac{I_{peak}D_{max}}{2} \tag{7-244}$$

From this D_{max} is extracted:

$$D_{max} = \frac{2P_{out}}{I_{peak}V_{bulk,min}\eta} \tag{7-245}$$

Substituting this equation into Eq. (7-243) gives

$$I_{D,rms} = \sqrt{\frac{2I_{peak}P_{out}}{3\eta V_{bulk,min}}} \tag{7-246}$$

Using Eq. (7-246), we can compute the conduction losses of the MOSFET:

$$P_{cond} = I_{D,rms}{}^2 R_{DS(on)} @ T_j = 110\ ^\circ\text{C} \tag{7-247}$$

As we connect an additional capacitor from the drain to the source, it will result in additional switching losses. Assuming we switch the MOSFET on right in the wave valley (Fig. 7-86), the associated switching losses at the highest line input are

$$P_{sw} = 0.5\left(V_{bulk,max} - \frac{V_{out} + V_f}{N}\right)^2 C_{DS}F_{sw,max} \tag{7-248}$$

where $V_{bulk,max}$ represents the bulk voltage at the highest line input (375 Vdc in this example). In that case, the converter is assumed to operate at a frequency defined by Eq. (7-242) where $V_{bulk,min}$ is replaced by $V_{bulk,max}$. Depending on the controller, this frequency can be achieved or clamped if it exceeds a certain value (usually less than 150 kHz for EMI issues).

The design now comes to a point where we need to select a turns ratio to derive the rest of the variables. To select this particular number N, we first need to list the constraints we have:

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$F_{sw,min}$: This is the minimum switching frequency at full power and low line. If selected too low, it can bring the converter into the audible range and generate acoustical noise problems. Too high, it can quickly push the power supply into the upper range of switching frequencies, and switching losses will dominate. 40 kHz can be a number to start with.

$F_{sw,max}$: As emphasized above, we do not want a very high switching frequency because Eq. (7-248) will lead the MOSFET power dissipation budget. Also, for EMI reasons, keeping the frequency around 70 kHz can be a good point. Let us stick to this value for the maximum frequency.

L_{leak}: This is the leakage inductance. We assume it to be 1% of the primary inductance:

$$L_{leak} = \frac{L_p}{100}$$

V_{leak}: This is the key number that we need to optimize. If it is selected too low, the C_{DS} capacitor increases to keep the drain excursion within control, and again the MOSFET suffers from switching losses at high line. If it is too high, we reflect less voltage on the primary side and the conduction losses now become dominant at low line.

To help select the right V_{leak} value, we will plot both switching and conduction losses, respectively, at high- and low-line conditions, as a function of V_{leak}. We could also plot the total contribution $P_{sw} + P_{cond}$ at low- and high-line conditions, but we considered switching and conduction losses separately here for the sake of simpler equations. We then select the point at which both contributions equal, in order to obtain a balanced budget between switching and conduction losses at the two input voltage extremes. The iteration exercise also includes several values for the $R_{DS(on)}$ in order to dissipate, at the end, a reasonable amount of power on the MOSFET, at an acceptable cost. A few trials indicated that an $R_{DS(on)}$ of 1.5 Ω could be the right choice, leading to a dissipated power of 2 W. Based on this $R_{DS(on)}$ figure, Fig. 7-90 portrays the curves obtained through the definition of conduction and switching

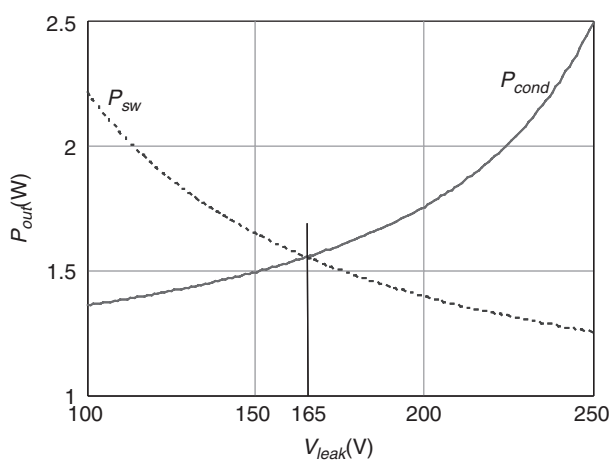

FIGURE 7-90 Curves showing the evolution of switching losses (high line) and conduction losses (low line) as a function of the selected drain voltage overshoot. The intersection corresponds to a point where individual contributions are equal. The point could be refined by plotting total losses at both input voltage extremes but at the expense of more complicated formulas.

losses as functions of V_{leak}:

$$P_{cond}(V_{leak}) = \frac{4P_{out}{}^2R_{DS(on)}}{3(V_{out} + V_f)(\eta V_{bulk,min})^2}\left(V_{out} + V_f + \frac{(V_{out} + V_f)V_{bulk,min}}{BV_{DSS}\alpha - V_{bulk,max} - V_{leak}}\right) \quad (7\text{-}249)$$

$$P_{sw}(V_{leak}) = \frac{P_{out}F_{sw,max}(2V_{bulk,max} - BV_{DSS}\alpha + V_{leak})^2}{100V_{leak}{}^2F_{sw,min}\eta} \quad (7\text{-}250)$$

Reading Fig. 7-90 [or equating Eqs. (7-249) and (7-250)], we find a V_{leak} value of 165 V. We can now substitute this number into the above design equations to obtain the recommended values:

$$N = \frac{V_{out} + V_f}{BV_{dss}\alpha - V_{bulk,max} - V_{leak}} = \frac{5 + 0.8}{800 \times 0.85 - 375 - 165} = 0.041 \quad (7\text{-}251)$$

We will select a turns ratio of 25, or $N = 0.04$. Knowing the turns ratio, we can calculate the inductor value given the minimum operating frequency we have chosen (40 kHz):

$$L_p \le \frac{\eta(V_{out} + V_f)^2V_{bulk,\,min}{}^2}{2P_{out}F_{sw,\,min}(V_{out} + V_f + NV_{bulk,\,min})^2}$$

$$\le \frac{0.8 \times (5 + 0.8)^2 \times 90^2}{2 \times 35 \times 40k \times (5 + 0.8 + 0.041 \times 90)^2} \le 864\,\mu\text{H} \quad (7\text{-}252)$$

Selecting a 860 μH indicator; the maximum peak current at low line is found to be

$$I_{peak} = \sqrt{\frac{2P_{out}}{F_{sw,min}L_p\eta}} = \sqrt{\frac{2 \times 35}{0.8 \times 40k \times 860u}} = 1.6\,\text{A} \quad (7\text{-}253)$$

The corresponding rms current then reaches a value of

$$I_{D,rms} = \sqrt{\frac{2I_{peak}P_{out}}{3\eta V_{bulk,min}}} = \sqrt{\frac{2 \times 1.6 \times 35}{3 \times 0.8 \times 90}} = 0.72\,\text{A} \quad (7\text{-}254)$$

Based on our $R_{DS(on)}$ trial, we have selected an 800 V MOSFET, the STP7NK80Z from ST:

$BV_{DSS} = 800$ V
$R_{DS(on)}$ at $T_j = 25\,^\circ\text{C} = 1.5\,\Omega$
$Q_g = 56$ nC

According to Eq. (7-254), the low-line conduction losses on the MOSFET amount to

$$P_{cond} = I_{D,rms}{}^2R_{DS(on)}@T_j = 110\,^\circ\text{C} = 0.72^2 \times 3 = 1.55\,\text{W} \quad (7\text{-}255)$$

Assuming a leakage inductor being 1% of L_p (8.6 μH, then), we can calculate the capacitor to be installed between drain and source to satisfy Eq. (7-232):

$$C_{DS} = \left(\frac{I_{peak}}{V_{leak}}\right)^2L_{leak} = \left(\frac{1.6}{165}\right)^2 \times 8.6u = 808\,\text{pF} \quad (7\text{-}256)$$

Select an 820 pF, 1 kV type.

The worst-case switching losses occur at high line, in the valley [Eq. (7-248)] for a properly tweaked converter, when the switching frequency reaches the selected limit, 70 kHz in this

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design example:

$$P_{sw} = 0.5\left(V_{bulk,max} - \frac{V_{out} + V_f}{N}\right)^2 C_{DS} F_{sw,max}$$

$$= 0.5 \times \left(375 - \frac{5.8}{0.04}\right)^2 \times 820p \times 70k = 1.52\,\text{W} \quad (7\text{-}257)$$

With these numbers on hand, we can now assess the MOSFET dissipation at both input voltage extremes:

$$P_{tot}@V_{bulk,min} = P_{cond} + P_{SW} = 1.55 + 0 \approx 1.55\,\text{W} \quad (7\text{-}258a)$$

$$P_{tot}@V_{bulk,max} = P_{cond} + P_{SW} = 0.5 + 1.52 \approx 2\,\text{W} \quad (7\text{-}258b)$$

At low line, as the reflected voltage exceeds the bulk voltage, the MOSFET body diode conducts, and we have perfect zero-voltage switching: there are no turn-on switching losses. In high-line conditions, conduction losses go down but switching losses dominate. In both cases, we neglected turn-off losses, given the snubbing action of C_{DS} whose presence delays the rise of $V_{DS}(t)$. Bench measurements can confirm or deny this design assumption. For a dissipated power of 2 W, we need to choose a heat sink offering the following thermal resistance:

$$R_{\theta H-A} = \frac{T_{j,max} - T_A}{P} - R_{\theta J-C} - R_{\theta C-H} = \frac{110 - 50}{2} - 2 - 1 = 27\,^{\circ}\text{C/W} \quad (7\text{-}259)$$

We need a peak current of 1.6 A. The sense resistor can therefore be calculated, accounting for a 10% margin on the peak current selection:

$$R_{sense} = \frac{1}{I_{peak} \times 1.1} = \frac{1}{1.6 \times 1.1} = 0.57\,\Omega \quad (7\text{-}260)$$

You might need to slightly decrease this value on the bench (or use a divider, Fig. 7-63). This is so because the minimum switching frequency does not account for the delay needed to switch right in the drain–source valley. This delay artificially decreases the switching frequency, and a higher peak current is needed to pass the power at low line.

The sense element will dissipate:

$$P_{R_{sense}} = I_{D,rms}{}^2 R_{sense} = 0.72^2 \times 0.57 = 295\,\text{mW} \quad (7\text{-}261)$$

Select three 1.8 Ω, 0.25 W resistors wired in parallel.

We have three windings, and the first turns ratio for the 5 V output is already known. To obtain the other ratios, we have the choice between three options described by Fig. 7-91:

- The normal way imposes three distinct windings, asking a set of two connecting points on the secondary-side bobbin. Despite a good coupling between the windings, this is the least performing in terms of cross-regulation. Each wire is sized according to its own individual current requirement.
- The ac stack consists of stacking the winding before the rectifying diode. It can work on secondaries sharing the same ground and a similar polarity. The number of turns goes down, compared to the previous solution. The wire size of the lower output winding (5 V) must be sized according to the rms currents drawn from the above winding (12 V).
- The dc stack, on the other hand, connects the windings on the dc output, starting from the lowest voltage. In Fig. 7-91, we have stacked the 12 V output on top of the 5 V one. Experience shows that this solution offers superior cross-regulation performance compared to the ac stack. It is often found on multioutput printer power supplies. Given the arrangement, the 12 V diode sees a reduced voltage stress compared to the normal solution. We will come back to this in the secondary study.

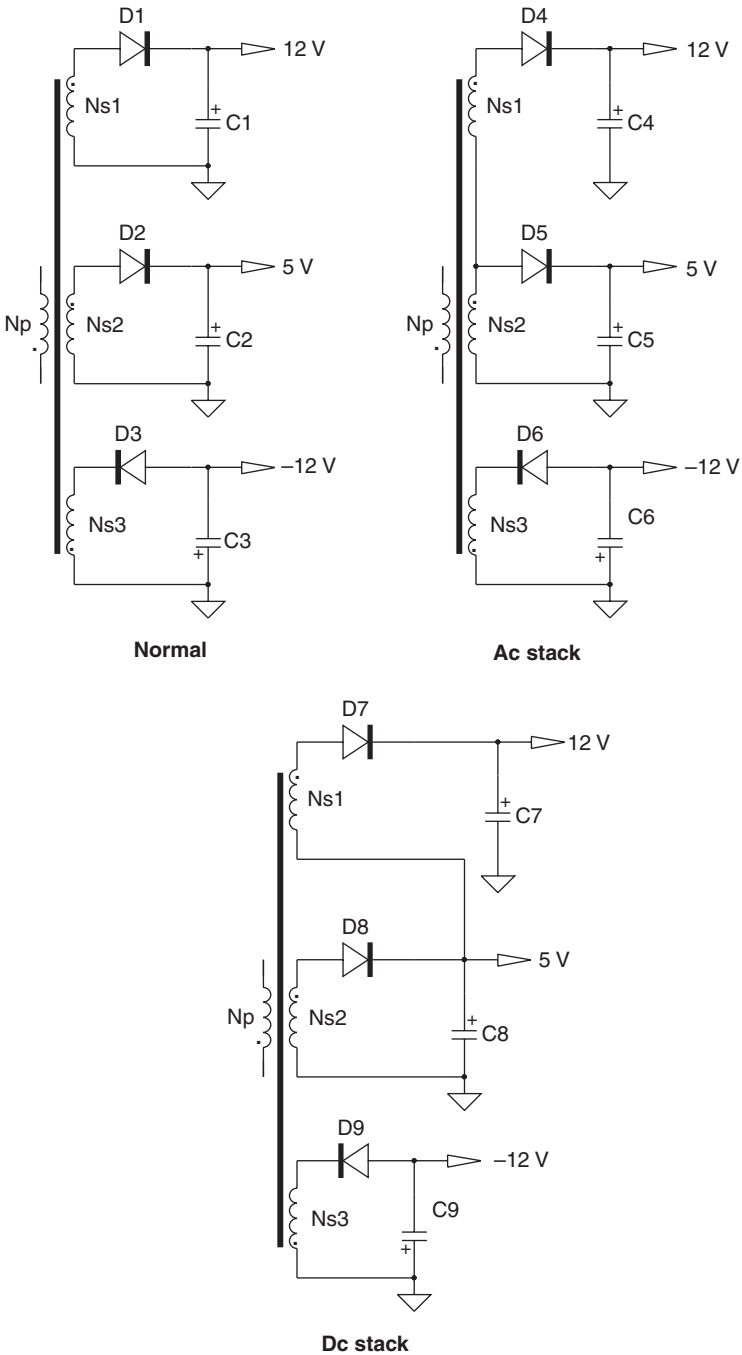

FIGURE 7-91 Three different options to wire the secondary windings.

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Transformer constructions can become complicated using these techniques while ensuring compliance with the international safety standards. Reference 11 presents several solutions on how to arrange the various windings and how that affects performance. In this example, we will adopt the dc stack solution.

With an original turns ratio of 1:0.04 for the 5 V output, we can quickly derive the turns ratios of the other windings. The negative 12 V winding ratio is simply

$$N_p{:}N_{s,12neg} = 1{:}N_{s,5}\frac{12}{5} = 1{:}0.04 \times 2.4 = 1{:}0.096 \tag{7-262}$$

The 12 V being stacked on top of the 5 V, it must deliver 7 V. Thus

$$N_p{:}N_{s,12pos} = 1{:}N_{s,5}\frac{7}{5} = 1{:}0.04 \times 1.4 = 1{:}0.056 \tag{7-263}$$

What is the problem here? We do not account for the forward drop of each diode at the selected output current. Either we update Eqs. (7-262) and (7-263) to include this V_f information or we go through average simulations, using the selected diodes, and adjust the ratios to fit the targets.

Regarding these diodes, what are their respective stresses and losses? For the 5 V output, the peak inverse voltage is the following:

$$\text{PIV} = V_{bulk,\,max}N + V_{out} = 375 \times 0.04 + 5 = 20\,\text{V} \tag{7-264}$$

Select a 40 V Schottky diode, sustaining 6 A at least. Remember, given the stacked configuration, the 5 V diode also sees the output current of the 12 V line ($I_{d,avg} = 2 + 2 = 4$ A)! An MBRF2060CT fits the bill:

MBRF2060CT
TO-220 full pack
V_f at [$T_j = 100$ °C and $I_d = 4$ A] = 0.5 V
Maximum junction temperature = 175 °C

Its associated conduction losses are then

$$P_{cond} = V_f I_{d,avg} = V_f I_{out} = 0.5 \times 4 = 2\,\text{W} \tag{7-265}$$

For a 2 W dissipation need, a small heat sink must be added. It should have a thermal resistance of

$$R_{\theta H-A} = \frac{T_{j,max} - T_A}{P} - R_{\theta J-C} - R_{\theta C-H} = \frac{150 - 50}{4} - 2 - 1 = 22\,°\text{C/W} \tag{7-266}$$

For the negative winding, −12 V, the reverse voltage reaches

$$\text{PIV} = V_{bulk,max}N + V_{out} = 375 \times 0.04 + 12 = 27\,\text{V} \tag{7-267}$$

Select a 60 V, 1 A diode, fast switching type given the low output current (100 mA). We found that an MBR160LRG was a good choice:

MBR160T3G
SMA package
V_f at [$T_j = 100$ °C and $I_d = 0.1$ A] = 0.3 V

Its associated conduction losses are

$$P_{cond} = V_f I_{d,avg} = V_f I_{out} = 0.3 \times 0.1 = 30\,\text{mW} \tag{7-268}$$

For the positive 12 V winding, the PIV slightly differs as the +5 V comes in series with the winding when it swings negative. Thus

$$\text{PIV} = V_{bulk,max}N - 5 + V_{out} = 375 \times 0.04 + 12 - 5 = 22\text{ V} \tag{7-269}$$

For a 2 A output and a 40 V breakdown, the MBRS540T3G looks good (5 A diode):

MBRS540T3G
SMC package
V_f at [T_j = 100 °C and I_d = 2 A] = 0.35 V

Its associated conduction losses are then

$$P_{cond} = V_f I_{d,avg} = V_f I_{out} = 0.35 \times 2 = 700\,\text{mW} \tag{7-270}$$

If we install the diode over a 3.2 cm^2 copper frame for each lead, the junction-to-ambient thermal resistance drops to 78 °C/W. The diode junction in a 50 °C ambient thus reaches

$$T_j = T_A + R_{\theta J-A}P_{cond} = 50 + 78 \times 0.7 = 104\,°\text{C} \tag{7-271}$$

The secondary side capacitors must now be chosen, given the ripple characteristics for each output. We usually calculate the capacitor constraints by estimating the peak (ESR-linked ripple) and the rms (losses) currents flowing through them. Unfortunately, on a multioutput flyback converter, it is extremely difficult to predict current wave shapes and derive their associated peak and rms values. The presence of multiple leakage inductances degrades the whole picture, and using the standard T model would lead to errors. Figure 7-92 shows the cantilever

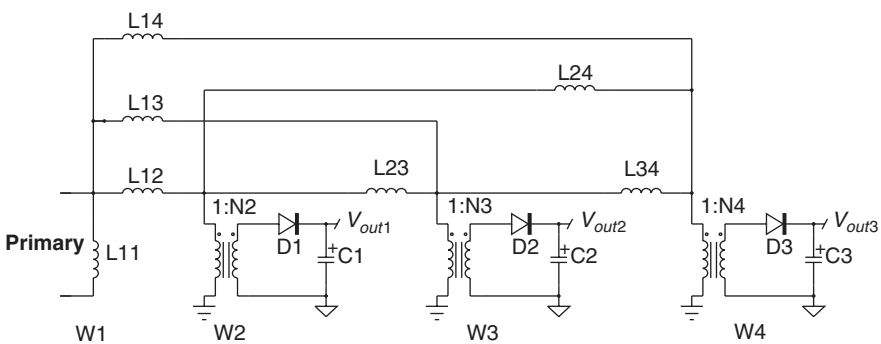

FIGURE 7-92 The upgraded cantilever model accounts for the multiple leakage inductors brought by the transformer construction.

model developed by CoPEC and presented in Ref. 12. This model leads to a good agreement between the simulated waveforms and the observed oscilloscope signals, but finding its parameters experimentally is a difficult and long exercise. The configuration and the way transitions occur depend on the installed clamping circuit. It is possible to show that at the switch opening event, the magnetizing current splits between the winding at a pace imposed by the leakage inductances L_{12}, L_{13}, and L_{14} and not by the individual output currents. As a result, the secondary side currents are sometimes far from the classical triangular wave shapes, and the simple equations that we derived no longer hold. On this particular design, given the low current on the third winding, we can try to find the rms and peak currents by using a simple two secondary winding equivalent arrangement, assuming truly triangular waveforms.

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In other words, the results given below are approximate, and bench experiments are mandatory to individually check the assumptions.

We first need to calculate the maximum duty cycle at low line [Eq. (7-245)]:

$$D_{max} = \frac{2P_{out}}{I_{peak}V_{bulk,min}\eta} = \frac{2 \times 35}{1.6 \times 90 \times 0.8} = 0.61 \tag{7-272}$$

Now, as we operate in DCM, the current flowing in the 5 V diode, which also includes the 12 V, 2 A loading current as they are dc stacked, peaks to the following value, again assuming a plain triangular shape:

$$I_{sec,peak5V} \approx \frac{2(I_{out1} + I_{out2})}{1 - D_{max}} = \frac{2 \times 4}{1 - 0.61} = 20.5\,\text{A} \tag{7-273}$$

As both direct currents are equal on the 5 V and 12 V lines, we consider that they perfectly split in two, leading to a 10 A peak current on their respective diodes. Please keep in mind that this is just a rough approximation given the role of the leakage inductances of Fig. 7-92 which force different turn-off times on all diodes. Based on this result, for both 5 V and +12 V outputs, the capacitor ESRs must be smaller than

$$R_{ESR} \leq \frac{V_{ripple}}{I_{sec,peak}} \leq \frac{0.25}{10.5} \leq 24\,\text{m}\Omega \tag{7-274}$$

Searching a capacitor manufacturer's site (Rubycon), we found the following references:

5 V output:

2200 μF − 10 V − YXG series

Radial type, 12.5 (φ) × 20 mm

R_{ESR} = 35 mΩ at T_A = 20 °C and 100 kHz

$I_{C,rms}$ = 1.9 A at 100 kHz

12-V output:

1500 μF − 16 V − YXG series

Radial type, 12.5 (φ) × 20 mm

R_{ESR} = 35 mΩ at T_A = 20 °C and 100 kHz

$I_{C,rms}$ = 1.9 A at 100 kHz

Putting two capacitors in parallel for each output must give the ESR we are looking for. The rms current flowing in the 5 V line, which also includes the 12 V consumption, can be roughly evaluated via

$$I_{sec,rms5V} \approx I_{sec,peak5V}\sqrt{\frac{1 - D_{max}}{3}} = 20.5 \times \sqrt{\frac{1 - 0.61}{3}} = 7.4\,\text{A} \tag{7-275}$$

Assuming an equal split between currents, we can use Eq. (7-170) to calculate each capacitor rms current:

$$I_{C_{out,rms}} \approx \sqrt{\left(\frac{I_{sec,rms5V}}{2}\right)^2 - I_{out,avg}{}^2} = \sqrt{3.7^2 - 2^2} = 3.1\,\text{A} \tag{7-276}$$

In other words, the combination of two capacitors in parallel fits the rms current figure. The total ESR drops to

$$R_{ESR,total} = \frac{35m}{2} \approx 18\,\text{m}\Omega \tag{7-277}$$

The loss incurred by this resistive path amounts to

$$P_{C_{out}} = I_{C_{out},rms}{}^2 R_{ESR} = 3.1^2 \times 18m = 173\,\text{mW} \tag{7-278}$$

We are now set for the capacitors, at least for the two main outputs. Given the transformer leakage behavior, we cannot predict the rms and peak currents for the −12 V output. Therefore, a cycle-by-cycle simulation will bring us additional information. However, we will arbitrarily put a 470 μF capacitor for the average simulation.

For the average simulations, we are going to use the borderline model already tested in the PFC applications.

$L_p = 860\ \mu\text{H}$
$R_{sense} = 0.5\ \Omega$
$N_p{:}N_{s1} = 0.04$, 5 V/2 A, $R_{load} = 2.5\ \Omega$
$N_p{:}N_{s2} = 0.053$, 12 V/2 A, $R_{load} = 6\ \Omega$
$N_p{:}N_{s3} = 0.088$, −12 V/100 mA, $R_{load} = 120\ \Omega$
$C_{out1} = 4400\ \mu\text{F}$, $R_{ESR} = 18\ \text{m}\Omega$
$C_{out2} = 3000\ \mu\text{F}$, $R_{ESR} = 18\ \text{m}\Omega$
$C_{out2} = 470\ \mu\text{F}$, $R_{ESR} = 250\ \text{m}\Omega$ (arbitrarily selected)

In this design, given the multiple-output configuration, we want to implement weighted feedback. That is, the TL431 will observe several outputs, each affected by a certain weight depending on its required tolerance. Figure 7-93 shows how to wire these resistors on the 5 V and the +12 V outputs.

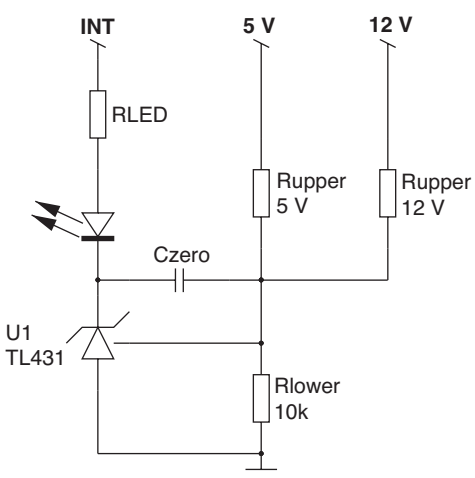

FIGURE 7-93 Weighted feedback offers superior performance in multioutput configurations.

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The calculation is similar to the regular way, except that a coefficient—the weight—is affected to the upper-side resistors. In this example, the 5 V needs to be the most precise (±5%), but the 12 V cannot drop below 10.8 V. An initial trial where we assign 70% (W_1) to the 5 V and 30% (W_2) to the 12 V can be tested. The calculation is as follows:

1. Choose a bridge current. We usually select 250 μA, leading to a lower-side resistor of

$$R_{lower} = \frac{V_{ref}}{I_{bridge}} = \frac{2.5}{250u} = 10\,\text{k}\Omega \tag{7-279}$$

2. The upper-side resistors follows the same procedure as for a single-output calculation, except that the final result is divided by the corresponding weight:

$$R_{upper5V} = \frac{V_{out1} - V_{ref}}{I_{bridge}W_1} = \frac{5 - 2.5}{250u \times 0.7} = 14.3\,\text{k}\Omega \tag{7-280}$$

$$R_{upper12V} = \frac{V_{out2} - V_{ref}}{I_{bridge}W_2} = \frac{12 - 2.5}{250u \times 0.3} = 126.6\,\text{k}\Omega \tag{7-281}$$

What bandwidth do we need, given the capacitor selection? Let us use the same formula which links the output drop (neglecting ESR effects) to the available bandwidth. In lack of specification for the output current changes, we will assume a step from 200 mA to 2 A on the 5 V and 12 V lines. We select the output featuring the lowest capacitance in this case.

$$f_c \approx \frac{\Delta I_{out}}{2\pi_c \Delta V_{out} C_{out}} = \frac{1.8}{6.28 \times 0.25 \times 3000u} \approx 382\,\text{Hz} \tag{7-282}$$

We will adopt a 1 kHz bandwidth, giving us a comfortable margin. Here, we do not need to worry about an RHPZ as it does not exist (in the low-frequency domain at least), thanks to the permanent BCM operation. The complete ac circuit appears in Fig. 7-94 and requires some comments:

1. We assume an internal division by 3, as for the other controllers used in design examples 1 and 2. If you choose an NCP1207A or an NCP1337 from ON Semiconductor, this is the case.
2. As we use weighted feedback, we cannot observe a single output since two are used for the loop. We will thus observe the total result, made of the sum of the 5 and 12 V lines, affected by the chosen weight. The observed point is labeled OLW.
3. As for the previous design, we first sweep with the optocoupler in the loop path to account for its pole and the additional phase shift it brings. It is then further removed to check the final result. We kept the pole at 6 kHz with a CTR of 1.5. Of course, these parameters will change depending on the type of component you use here (see Chap. 3 for more details on the optocoupler).
4. The bias points show a switching frequency of 45 kHz and a peak current of 1.4 A (V_c/R_i).
5. Observing an on time of 13.4 μs with a 45 kHz switching gives a duty cycle of 60.3%, in agreement with Eq. (7-272).

The resulting Bode plot appears in Fig. 7-95. At a 1 kHz point, the deficit in gain is −32 dB, and the phase lags by 83°. The *k* factor method gives acceptable results for a first-order system like this QR flyback. Hence, thanks to the automated method, the compensation can be quickly made following the procedure recommendations (see other design examples and Chap. 3 for more details):

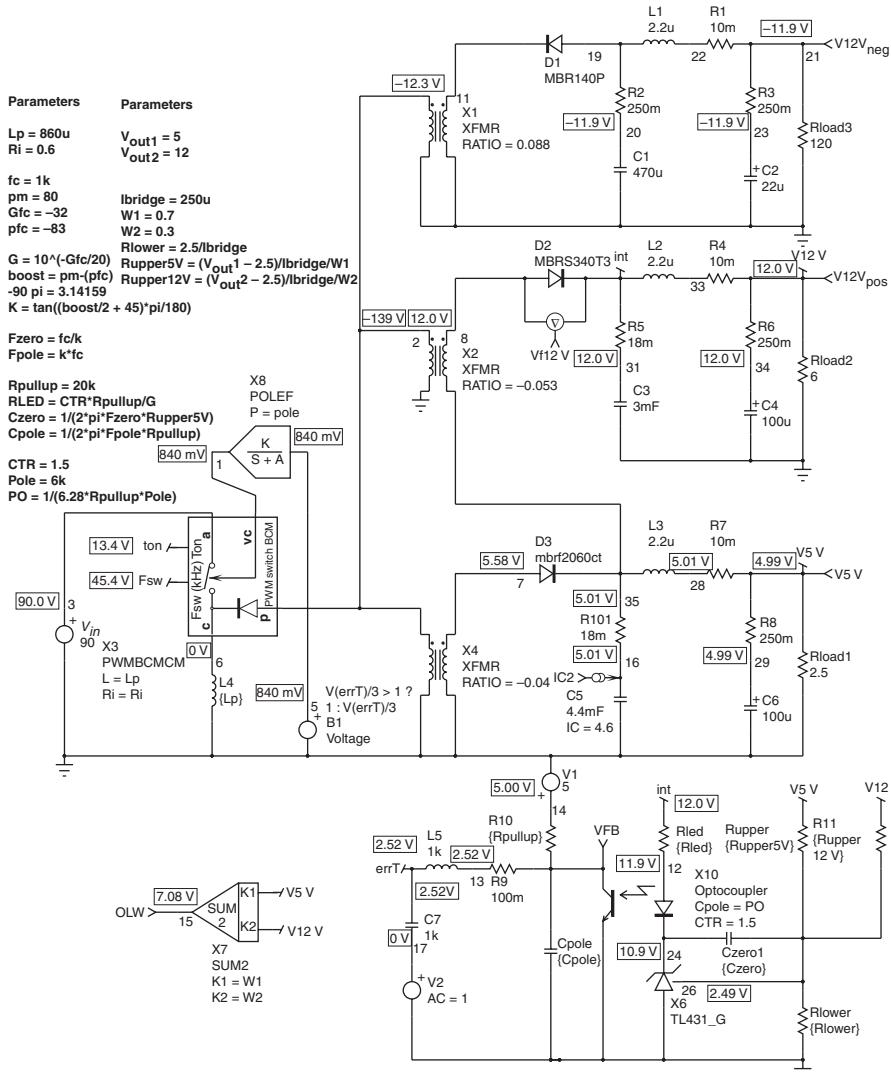

FIGURE 7-94 The complete ac circuit for the multioutput flyback converter where the optocoupler pole purposely appears in the chain.

1. We place a pole at 7 kHz, $C_{pole} = 1.2$ nF.
2. A zero is located at 150 Hz, $C_{zero} = 75$ nF.
3. The LED resistor is calculated to offer a 32 dB gain boost at 1 kHz. $R_{LED} = 750\Omega$.

For the above calculation, we have arbitrarily selected the 5 V output upper resistor to calculate the zero location. Since we have two loops, this placement will obviously affect the other loop (the 12 V path), but as long as the final result observed on the feedback pin gives adequate phase margin, we are safe. Figure 7-96 confirms this assumption by plotting the open-loop gain after

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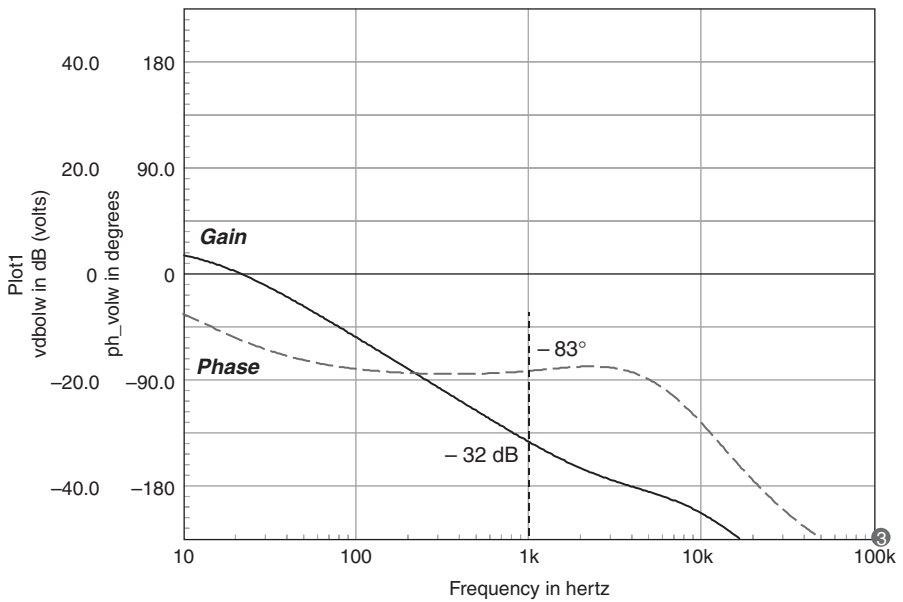

FIGURE 7-95 The open-loop small-signal response of the multiple-output flyback converter operated in QR.

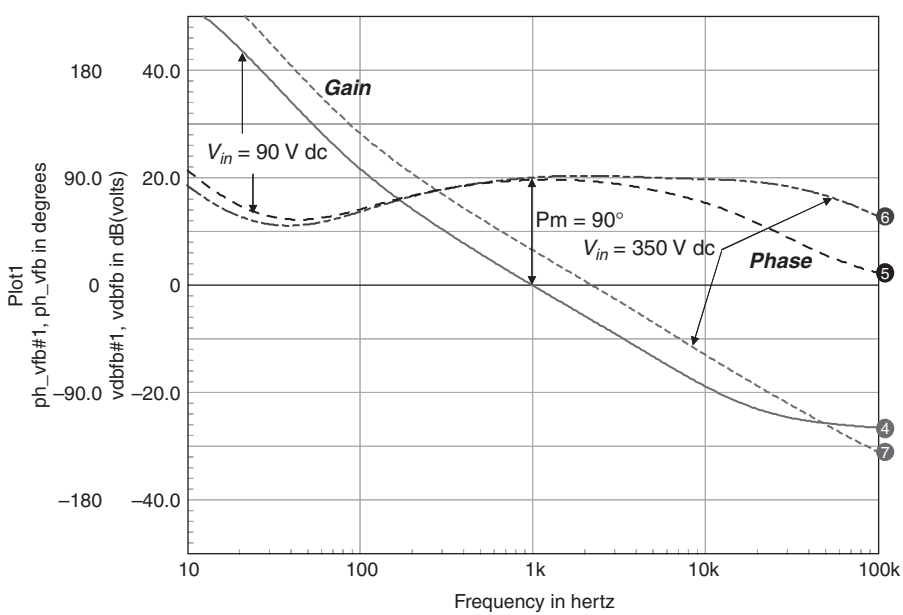

FIGURE 7-96 The final loop gain shows the right crossover frequency with a good phase margin.

proper compensation (observed on the optocoupler collector). As usual, all stray parameters such as ESRs must now be swept to check that they do not threaten the phase margin in any case.

We can now assemble the cycle-by-cycle model and verify a few key parameters such as rms currents and the peak voltage on the drain at the maximum line input. Figure 7-97 depicts the adopted schematic. The core reset detection is obtained via an auxiliary winding to which an *RC* delay is added (R_9C_9, on pin 1 of the controller). This delay helps to switch right in the minimum of the drain wave and slightly reduces the switching frequency, leading to a higher peak current.

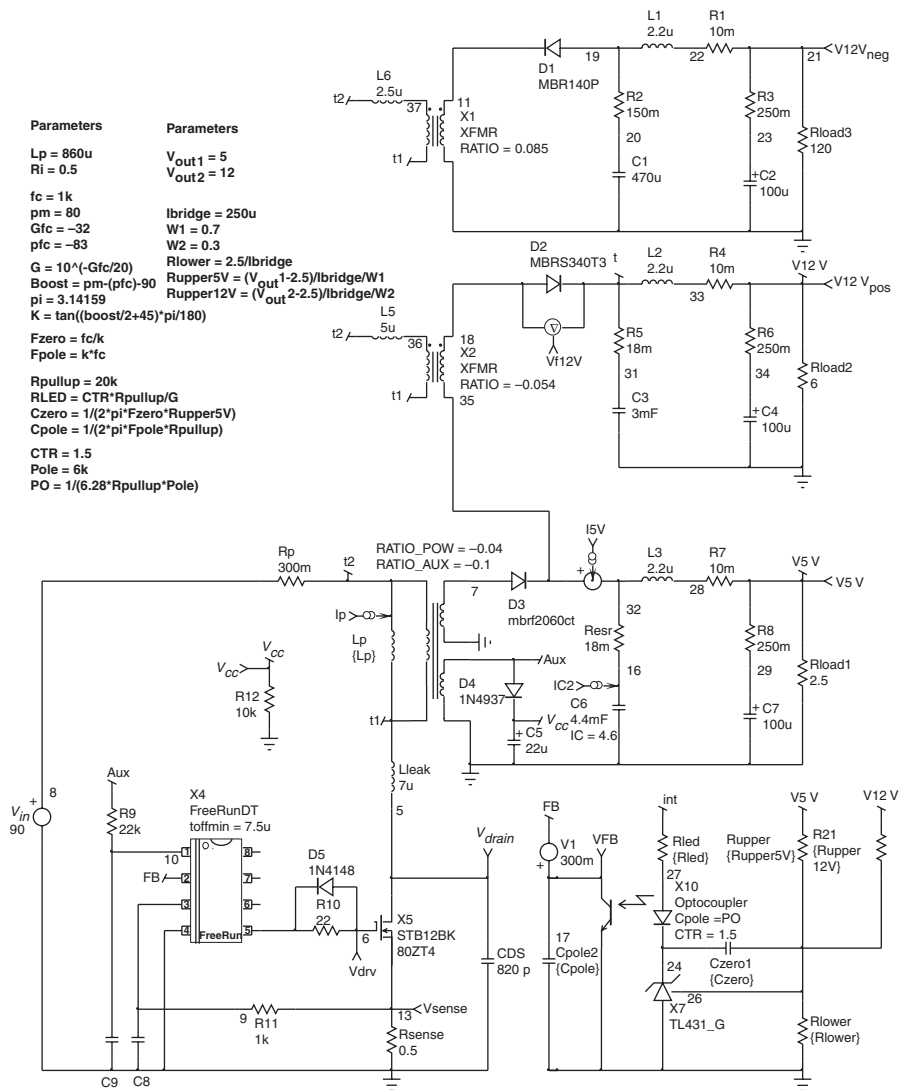

FIGURE 7-97 The cycle-by-cycle simulation circuit. We purposely added some leakage inductances on the transformer model, as described in App. 4B.

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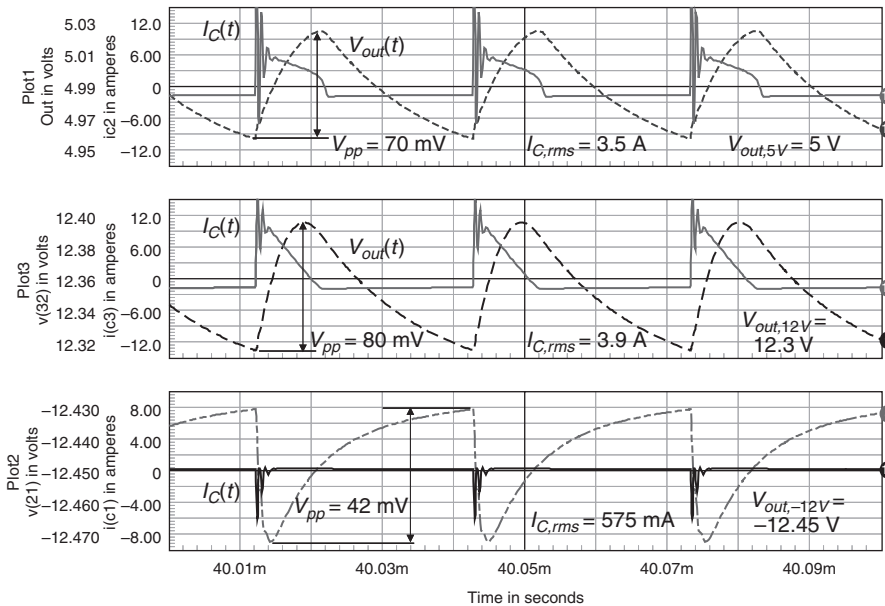

FIGURE 7-98 The simulation schematic for the QR converter. The simulation makes use of the FreerunDT model.

Simulation results appear in Fig. 7-98, showing the output voltages and their associated main capacitor ripples (before the *LC* filter). The capacitor rms currents are slightly above the analytical prediction, mainly because of the primary current split at the switch opening which induces a non triangular shape. The negative line requires a capacitor capable of accepting an rms current of around 600 mA, with a peak reaching 6 A. Note the short pulse duration on this particular winding. The primary current now climbs up to 1.7 A, for a 33 kHz operating frequency.

Figure 7-99 offers simulation results on the MOSFET drain signal. At low line, as we reflect more than the input voltage, the body diode is biased and the switch turns on at zero voltage: there are no switching losses at turn-on. At high line, the delay introduced by R_9C_9 makes us switch right in the valley, limiting switching losses. The delay after DCM detection lies around 3 μs. Thanks to the capacitor installed between drain and source, the peak voltage reaches 580 V, well below the 800 V limit. Needless to say, your transformer manufacturer must not change the transformer construction once the final prototype and its associated leakage inductance have been qualified!

Finally, a low-line transient response on the 5 V line will let us know if our design is properly stabilized, at least on the computer! The 5 V output is stepped from 1 to 2 A in 10 μs. Figure 7-100 portrays the transient response delivered by the cycle-by-cycle simulation. All drops are within the specification limits. Given the simplified transformer model used here, bench validations are necessary on both small-signal and transient aspects.

Figure 7-101 depicts the final application schematic involving an NCP1207A or the more recent NCP1337. The auxiliary winding serves the purpose of core reset detection only, as the 1207A is self-supplied by its internal dynamic self-supply (DSS). Make sure, however, that the Q_G and the maximum switching frequency are compatible with the DSS current capability. To cope with the eventuality of a weak supply, a simple diode wired to the auxiliary winding can permanently supply the controller.

The following transformer information can then be passed to the manufacturer for the prototype definition. RMS results are obtained from a low-line simulation:

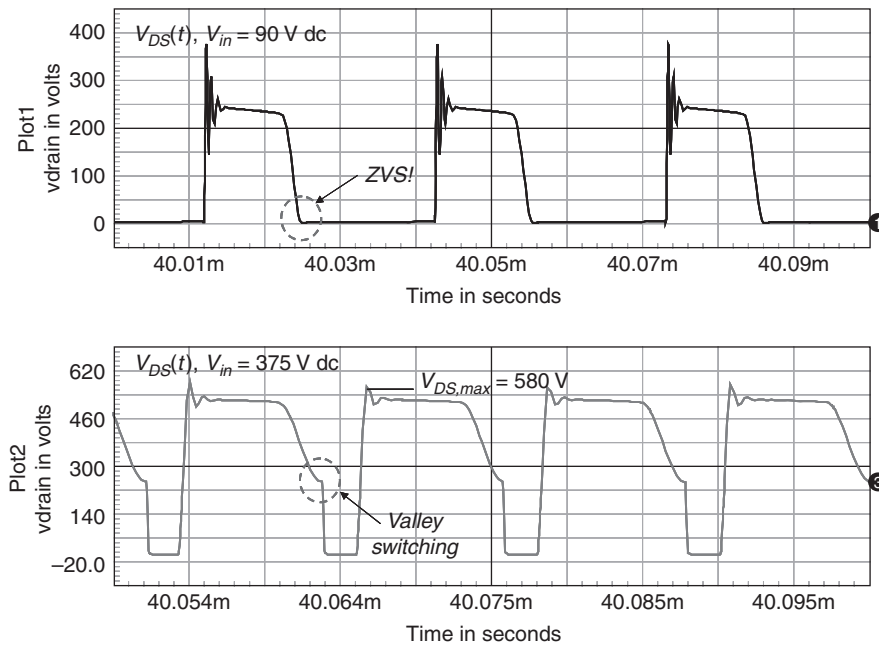

FIGURE 7-99 The drain-source voltage waveforms at low line and high line. The peak stays under control with the simple drain–source capacitor.

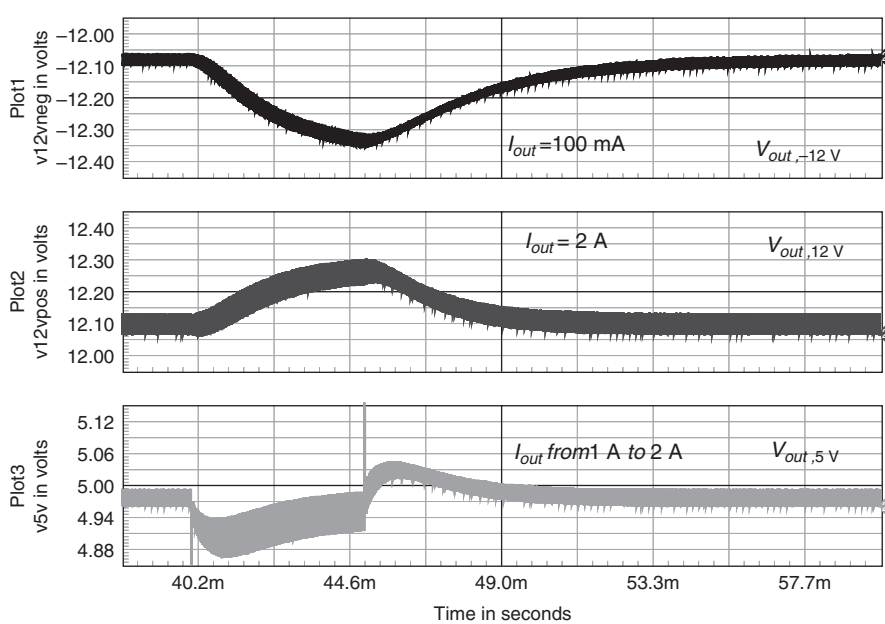

FIGURE 7-100 The transient response shows a well-stabilized converter.

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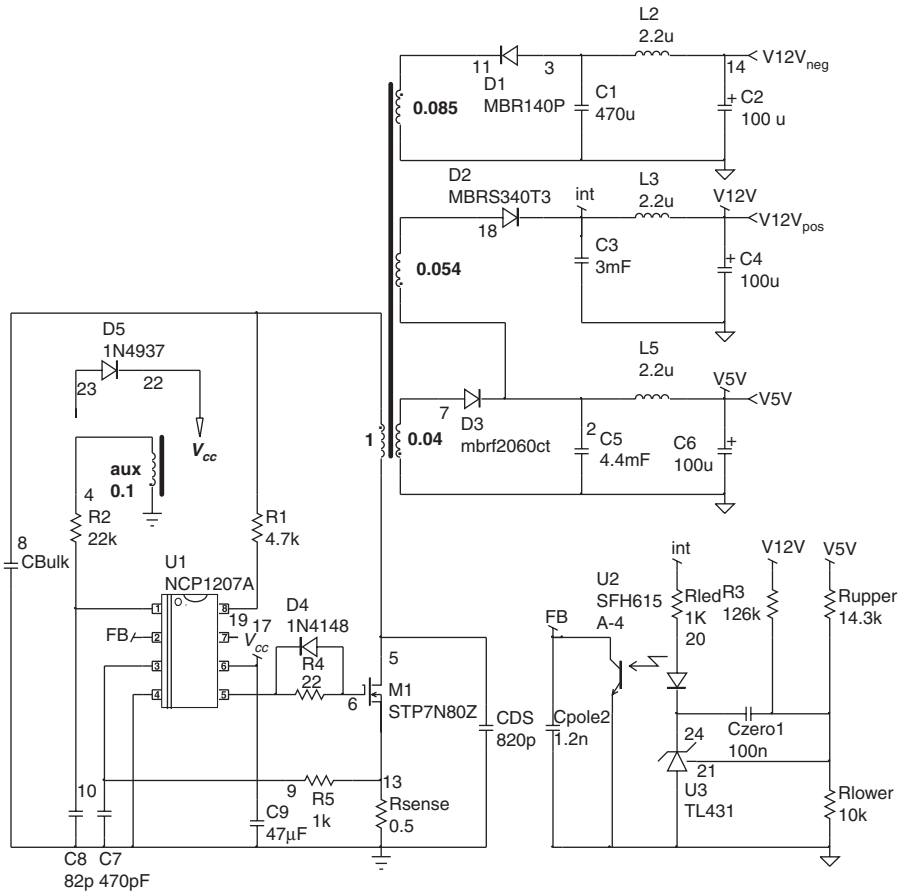

FIGURE 7-101 The final converter circuit using an NCP1207A. An option exists to wire the auxiliary winding as an auxiliary V_{cc} in case the DSS were too weak.

L_p = 860 µH, $I_{p,rms}$ = 800 mA, I_{peak} = 1.75 A
N_p:N_{s1} = 1:0.04, 5 V/2 A, $I_{sec1,rms}$ = 8 A
N_p:N_{s2} = 1:0.053, 12 V/2 A – dc stacked on N_{s1}, $I_{sec2,rms}$ = 4.3 A
N_p:N_{s3} = 1:0.088, – 12 V/100 mA, $I_{sec3,rms}$ = 580 mA
F_{sw} = 40 kHz

7.16 COMPONENT CONSTRAINTS FOR THE FLYBACK CONVERTER

To complete the flyback design examples, we have gathered the constraints seen by the key elements used in this configuration. These data should help you select adequate breakdown voltages of the diode and the power switch. All formulas relate to the CCM and DCM operations.

MOSFET
$BV_{DSS} > V_{in,max} + \frac{V_{out} + V_f}{N} + V_{clamp} + V_{OS}$ Breakdown voltage
$I_{D,rms} = \sqrt{D_{max}\left(I_{peak}{}^2 - I_{peak}\Delta I_L + \frac{\Delta I_L{}^2}{3}\right)}$ CCM
$I_{D,rms} = I_{peak}\sqrt{\frac{D}{3}}$ DCM
Diode
$V_{RRM} > V_{out} + NV_{in,max}$ Peak repetitive reverse voltage
$I_{F,avg} = I_{out}$ Continuous current
Capacitor
$I_{C_{out},rms} = I_{out}\sqrt{\frac{D_{max}}{1 - D_{max}} + \frac{D_{max}}{12}\left(\frac{1 - D_{max}}{\tau_L}\right)^2}$ CCM
$I_{C_{out},rms} = I_{out}\sqrt{\frac{2}{3}\left(\frac{\sqrt{1 + 2D_{max}{}^2/\tau_L} - 1}{D_{max}}\right) - 1}$ DCM
with $\tau_L = \frac{L_{sec}}{R_{load}T_{sw}}$ and $L_{sec} = L_pN^2$

WHAT I SHOULD RETAIN FROM CHAP. 7

The flyback converter is certainly the most widespread converter on the consumer market. Given its simplicity of implementation, many designers adopt it for power levels up to 200 W. Throughout this chapter, we have reviewed a few important things to keep in mind when you are thinking about a flyback:

1. The leakage inductance plagues any transformer design. As power goes up, if your leakage term does not stay under control, your clamping network might dissipate too much power for a given printer circuit board (pcb) area. Make sure the manufacturer you have selected understands this and guarantees a constant low-leakage term.
2. Watch out for the maximum voltage seen by the semiconductors, and in particular, the primary MOSFET. Adopt a sufficient design margin from the beginning, or failures may occur in the field. The same applies for the secondary diode: do not hesitate to place dampers across diodes to calm dangerous oscillations.
3. Often overlooked is the rms current on the secondary side capacitors, as it greatly affects their lifetime. The problem becomes huge if you design in DCM or in quasi-resonant mode.
4. The small-signal study leads to an easier design for peak current-mode converters compared to voltage-mode ones. Transition from one mode to the other is well handled for current-mode control power supplies whereas it becomes a more difficult exercise for voltage-mode based converters.

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5. Simulation does not lend itself very well to multioutput converters, unless you can plug a good transformer model. Thus, bench measurements are even more important to check the rms currents found in the various secondaries.
6. The standby power criterion is becoming an important topic these years. We recommend that your designs already include low standby power conversion techniques; that is, pick up less power-greedy controllers implementing skip-cycle or off-time expansion in light loads and so on. UC384X-based designs are really poor on the power-saving performance and should be left over for no-load operated power supplies permanently connected to the mains. So-called green controllers are generally slightly higher priced than the standard controllers, but the benefit for the distribution network is incomparable.

REFERENCES

1. http://www.ridleyengineering.com/snubber.htm
2. C. Nelson, LT1070 Design Manual, Linear Technology, 1986.
3. http://scholar.lib.vt.edu/theses/available/etd-71398-22552/
4. D. Dalal, "Design Considerations for Active Clamp and Reset Technique," Texas-Instruments Application Note, slup112.
5. M. Jovanovic and L. Huber, "Evaluation of Flyback Topologies for Notebook AC-DC Adapters/Chargers Applications," *HFPC Proceedings,* May 1995, pp. 284–294.
6. R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an Active-Clamp Circuit to Achieve Soft Switching in Flyback Converters," *Power Electronics, IEEE Transactions,* vol. 11, Issue 1, pp. 162–169, January 1996.
7. http://www.iea.org/
8. http://www.eu-energystar.org/en/index.html
9. AN4137, www.fairchild.com
10. J.-P. Ferrieux and F. Forest, "Alimentation à Découpage Convertisseurs à Résonance," 2d ed., Masson, 2006.
11. AN4140, www.fairchild.com
12. B. Erickson and D. Maksimovic, "Cross Regulation Mechanisms in Multiple-Output Forward and Flyback Converters," http://ece.colorado.edu/~pwrelect/publications.html
13. http://www.mag-inc.com/pdf/2006_Ferrite_Catalog/2006_Design_Information.pdf
14. http://www.unitconversion.org/unit_converter/area-ex.html

APPENDIX 7A READING THE WAVEFORMS TO EXTRACT THE TRANSFORMER PARAMETERS

Observing the drain–source waveform of a flyback converter can teach the designer a lot. First, you can immediately see if the power supply operates in DCM or CCM: identifying some ringing at the end of off time as in Fig. 7A-1 unveils a DCM mode. Second, measuring the various slopes and frequencies in play leads to extracting the parameters pertinent to the transformer. Figure 7A-1 represents the signal captured on a flyback converter supplied from a 300 Vdc input source, the drain voltage, but also the primary current. To determine the transformer elements, we have several equations we can use:

The primary slope S_{Lp}, indirectly delivered by measuring the di/dt of the drain current, equals

$$S_{L_p} = \frac{V_{in}}{L_p + L_{leak}} \tag{7A-1}$$

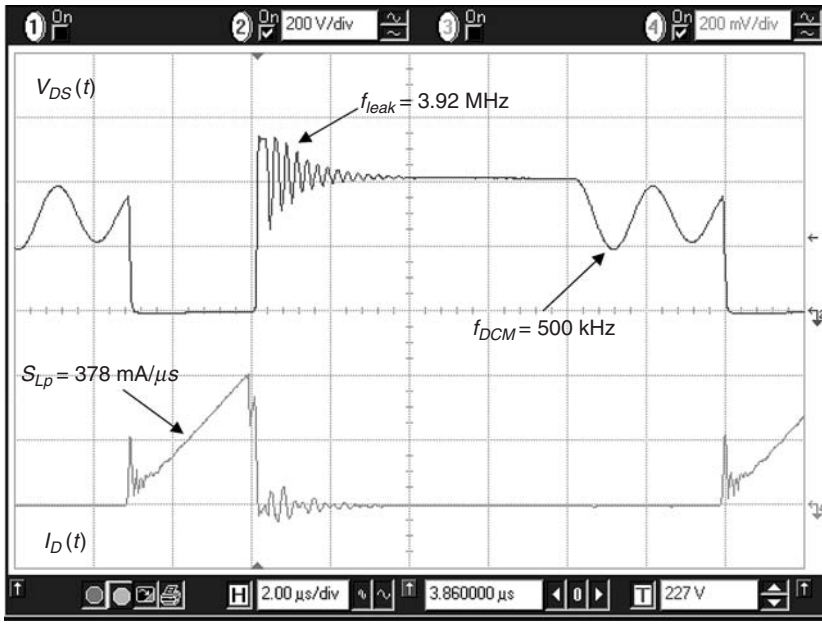

FIGURE 7A-1 A typical flyback wave obtained from a flyback converter.

The ringing frequency at the clamp diode opening involves the leakage inductance and the drain lump capacitor:

$$f_{leak} = \frac{1}{2\pi\sqrt{L_{leak}C_{lump}}} \tag{7A-2}$$

Finally, the DCM frequency also implies the lump capacitor but associated with the sum of leakage and primary inductors:

$$f_{DCM} = \frac{1}{2\pi\sqrt{(L_{leak} + L_p)C_{lump}}} \tag{7A-3}$$

Observing Fig. 7A-1, we found the following values:

$S_{Lp} = 378$ mA/μs
$f_{DCM} = 500$ kHz
$f_{leak} = 3.92$ MHz
$V_{in} = 300$ V

We have a set of three unknowns (L_p, L_{leak}, and C_{lump}) and three equations. Solving this system gives the individual transformer elements:

$$C_{lump} = \frac{S_{L_p}}{4V_{in}f_{DCM}^2\pi^2} = \frac{378k}{4 \times 300 \times 500k^2 \times 3.14^2} = 127\,\text{pF} \tag{7A-4}$$

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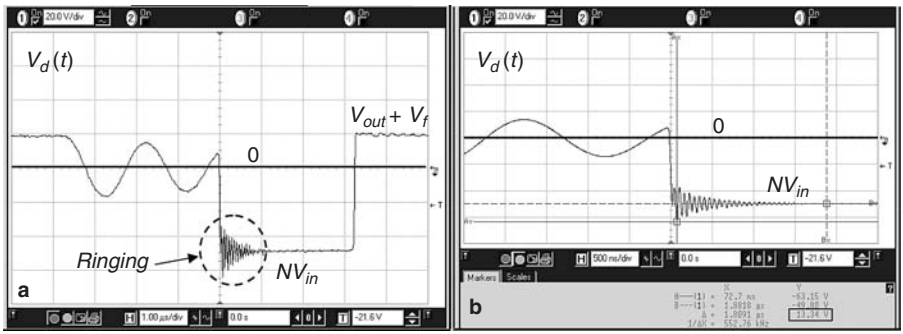

FIGURE 7A-2a and b Secondary side diode anode signal.

$$L_{leak} = \frac{1}{4\pi^2 f_{leak}{}^2 C_{lump}} = \frac{1}{4 \times 3.14^2 \times 3.92Meg^2 \times 127p} = 13\,\mu\text{H} \tag{7A-5}$$

$$L_p = \frac{V_{in} - S_{L_p} L_{leak}}{S_{L_p}} = \frac{300 - 378k \times 13u}{378k} = 780\,\mu\text{H} \tag{7A-6}$$

Looking back to the real transformer data sheet, we have a primary inductor of 770 μH and a leakage term of 12 μH. Our results are within very good limits. Just a final comment: make sure the frequencies read by the oscilloscope do not change too much when you observe the ringing with the probe in close proximity of the drain point (no electrical contact). Otherwise, it would mean the probe capacitance changes the ringing frequency and should be accounted for in the final results.

To obtain the turns ratio of any secondary winding, hook your scope probe on the anode of the secondary side diode of concern and measure the voltage. You should see something like Fig. 7A-2. The voltage drops to the input voltage multiplied by the turns ratio *N*. As we measured around 50 V from a 300 V input voltage, the ratio is simply

$$N = \frac{50}{300} = 166m \tag{7A-7}$$

Looking at Fig. 7A-2b triggers a very important comment. Equation (7-3) defines the peak inverse voltage of the secondary diode without considering any spikes. The figure speaks for itself: we have 13.3 V above what Eq. (7.3) would give us. Thus, always consider a safety margin when you are applying the theoretical formula and run a complete set of measurements on the final prototype to check this margin! Here, the worst-case condition would be the maximum input voltage. Adjust the loading current to check how the ringing amplitude evolves and chose the peak value. Then, apply an ×2 coefficient for the selected diode V_{RRM}.

APPENDIX 7B THE STRESS

The voltage or current stress represents an important factor in a component's lifetime, passive or active. Without entering into the details of energy activation and Arrhenius' law (Svante Arrhenius, Swedish, 1859–1927), there are a few commonsense remarks we can express in this appendix.

7B.1 Voltage

First, the breakdown voltage. Have you ever observed a voltage on a component above what is stated as the maximum rating in the data sheet, for instance, 620 V on a 600 V MOSFET? Why is the component still alive? Maybe I have a good design since it does not fail? Well, this is so because the manufacturer installs some guard bands on the probing program. These guard bands ensure that the worst element found after the wafer diffusion, and accepted for release, satisfies the stated breakdown. For instance, a 600 V MOSFET will be released as long as its leakage current, worst case, at 600 V is less than a few tens of microamperes. Thus, thanks to an extensive characterization work carried at various junction temperatures and including process variations, the manufacturer knows that a permanent 600 V bias will be safe. However, as in the production chain, there can be strong candidates, those whose breakdown is above the ratings (e.g., 630 V) and those which are weak (e.g., breaking down close to 600 V). Do not rely on a higher breakdown voltage considering the safety margin installed by the manufacturer—never! Make sure you apply your own safety margin on top of this one. A lot of SMPS makers derate their own operating voltages and currents by 15% compared to what is stated. This the derating factor k_D used throughout Chap. 7. Hence, for a 600 V MOSFET, tailor your clamping network to stay within 510 V in worst-case conditions. Tough, no? Perhaps a 650 V MOSFET will help, in certain cases. Avoid the 800 V versions; their $R_{DS(on)}$ is larger and they are much more expensive than their 600 V counterparts. Note that BV_{DSS} of MOSFETs and diodes (for a breakdown above 6.2 V) exhibits a positive temperature coefficient.

On the same tone, another important recommendation: do not use the MOSFET body diode avalanche capability as a permanent transient voltage suppressor (TVS). This is the best way to quickly kill the component. First, MOSFET avalanche capabilities are usually stated with an energy obtained from a large inductor and a small current, which is not the reality. Most of the time, you have a small inductor and a large current (thus a strong I_{rms}^2 component) flowing in your circuit. The fuse effect is thus strengthened with a larger rms current. When the MOSFET finally avalanches, a few observations can be made:

- The current flows through the internal parasitic NPN transistor obtained by the vertical diffusion of the die. Its collector–base junction avalanches.
- As the current flows through this path, only a small percentage of the die is activated; hence, there is a resistance to the current flow much larger than if 100% of the die were activated.
- A voltage breakdown is like a lightening strike: you cannot precisely predict where the current will flow in the die. Bad luck might route the avalanche current to weaker portions of the silicon and smoke pops up.

As a summary, you can allow accidental avalanche on the MOSFET, for instance, in the presence of input surges. If this is true for vertical MOSFETs (who remembers the VMOS these days!), never go above the BV_{DSS} for lateral MOSFETs such as those used in monolithic switchers. They also have a body diode, but it cannot accept any avalanche energy. A simple low-energy pulse would thus be lethal to the component.

Similar recommendations apply to the diode. Some data sheets state a nonrepetitive peak reverse voltage (V_{RSM}), again meaning that only an accidental surge is allowed. The safety factor for a diode, denoted by k_d, given the presence of ringing, is 100%. Yes, if you calculate a peak inverse voltage (PIV) of 50 V, select a 100 V diode.

Regarding the MOSFET driving voltage, there is no need to exceed 15 V. Above a V_{GS} of 10 V, the $R_{DS(on)}$ decreases only by a few percent and you dramatically increase the driving losses while reducing the MOSFET lifetime. The approximate heat lost in the MOSFET driver (the PWM controller) can be found from

$$P_{driver} = V_{GS} Q_G F_{sw} \tag{7B-1}$$

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where Q_G represents the total gate charge needed to fully turn on the MOSFET and F_{sw} is the switching frequency.

By the way, the gate charge represents an important value. It directly indicates the switching speed you can expect with a given drive output capability. If your data sheet indicates a total gate charge of 100 nC (a strong power MOSFET), and the driver can deliver a *constant* peak current of 1 A, you turn on in 100 ns!

$$t_{sw} = \frac{Q_G}{I_{peak}} \tag{7B-2}$$

In practice, CMOS-based drivers exhibit a resistive output impedance, and the driving current diminishes as $V_{GS}(t)$ increases. I know, it was not the case with bipolar-based output stages such as those from the UC384X series: the early effect was small enough to make them behave as almost ideal current sources despite V_{ce} variations.

Make sure no drain spikes bring the gate-source voltage above the gate oxide breakdown voltage (± 20 V or ± 30 V depending on the type of MOSFET). A gate-source zener often helps to reduce the associated risks with spikes coupled from the drain to the gate when high-voltage spikes show up. Unfortunately, given the sharpness of the zener, oscillations can sometimes occur and must be carefully observed, especially if you fear a large stray inductance (long wire to the MOSFET gate from the drive output, for instance). Inserting a small resistor close to the MOSFET gate (10 Ω) will help to damp the whole parasitic network.

7B.2 Current

Current stress relates to power dissipation and transient thermal impedance. Again the subject would need a complete book to be properly treated. Basically, the junction temperature of the device must stay within acceptable limits. What are these limits? With a diode or a transistor, for instance, the mold compound (the black plastic around the component leads) represents physical limits beyond which the junction cannot go. Why? Because the mold powder would melt down and deteriorate and contaminate the die. The die itself (at least the silicon) can reach temperatures as high as ≈250 °C, above which the silicon is said to be intrinsic. (It loses its semiconductor properties and becomes fully conducting—if it is not destroyed, it recovers when cooling down.) In TO3 packages, where there is no mold compound, you can allow high operating temperatures. For instance, ON Semiconductor 2N3055 states a maximum junction temperature as high as 200 °C! Put the same die in a traditional TO220 package, and the maximum rating would probably drop to around 150 °C.

A 20% derating on the maximum die temperature represents an acceptable tradeoff. For instance, a TO220 MOSFET accepts a junction temperature up to 150 °C, so make sure the worst-case die temperature stays below 110 to 120 °C. An MUR460 (4 A, 600 V ultrafast diode) accepts a junction temperature up to 175 °C. A 20% derating would lead to a maximum junction temperature of 140 °C. The junction temperature can have another side effect. Some SMPS manufacturers' quality departments (or their end customers) do not accept heat sink or component body temperature above 100 °C in the maximum ambient temperature. Make sure the heat sink calculation, involving the various thermal resistances, leads to the right case temperature. Sometimes, you find that a given MOSFET $R_{DS(on)}$ will pass the specification, but given the size constraints on the heat sink dimensions, you might need to adopt a much lower on resistance type to pass the case temperature requirement.

Another less known phenomenon relates to the so-called thermal fatigue. This occurs when you have important junction temperature excursions within a very short time. Because the energy duration is short, the heat does not have the time to propagate to the case and heat sink, and a local hot spot occurs. The temperature gradient can be so large that it induces a physical

stress on the junction or the connection pads which often give up. For instance, a semiconductor operated at an average junction temperature of 90 °C with a 20 °C ripple on it will suffer less than a 60 °C operated junction subject to a positive 50 °C excursion every 10 ms.

APPENDIX 7C TRANSFORMER DESIGN FOR THE 90 W ADAPTER

Contributed by Charles E. Mullett

This appendix describes the procedure to design the transformer for the 90 W CCM flyback converter described in Chap. 7. Thanks to the derived equations and simulations, we have gathered the following electrical data pertaining to the transformer design:

$L_p = 320\ \mu H$	Primary inductor
$I_{Lp,max} = 4$ A	Maximum peak current the transformer will accept without saturation
$I_{Lp,rms} = 1.8$ A	Primary inductor rms current
$I_{sec,rms} = 8$ A	Secondary side rms current
$F_{sw} = 65$ kHz	Switching frequency
$V_{out} = 19$ V @ 4.7 A	Output voltage and the dc output
$N_p{:}N_s = 1{:}0.25$	Primary to secondary turns ratio
$N_p{:}N_{aux} = 1{:}0.2$	Primary to the auxiliary winding turns ratio

7C.1 Core Selection

Based on the above data, several methods exist to determine the needed core size. In this appendix, we will use the area product definition. The first step therefore consists of finding the required area product W_aA_c, whose formula appears in the Magnetics Ferrite Core catalog available through the Ref. 1 link:

$$W_aA_c = \frac{P_{out}}{K_cK_tB_{\max}F_{SW}J}10^4 \tag{7C-1}$$

where W_aA_c = product of window area and core area, cm^4
P_{out} = output power, W
J = current density, A/cm^2
B_{max} = maximum flux density, T
F_{sw} = switching frequency, Hz
K_c = conversion constant for SI values (507)
K_t = topology constant (for a space factor of 0.4). This is the window fill factor. For the flyback converter, use $K_t = 0.00033$ for a single winding and $K_t = 0.00025$ for a multiwinding configuration.

Some judgment is required here, because the current density and flux density are left to the designer. A reasonable, conservative current density for a device of this power level, with natural convection cooling, is 400 A/cm^2.

The flux density at this frequency (65 kHz), for modern power ferrites such as Magnetics "P" material, is usually around 100 mT (1000 gauss). This can also be approached by choosing a loss

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factor of 100 mW/cm^3 (a reasonable number for a temperature rise of 40 °C) and looking up the flux density on the manufacturer's core material loss data. Doing this for the Magnetics Kool Mμ® material yields a flux density of 45 mT (450 gauss). We will use this for the design.

Therefore we have

$$W_a A_c = \frac{P_{out}}{K_c K_t B_{max} F_{SW} J} 10^4 = \frac{90 \times 10000}{507 \times 0.00033 \times 0.045 \times 65000 \times 400} = 4.6\,\text{cm}^4 \tag{7C-2}$$

Looking at the core-selection charts in the Magnetics Kool Mμ® catalog, we choose the DIN 42/20 E-core. It features an area product of 4.59 cm^4, a very close match to the requirement. For future reference, it has a core area of $A_e = 2.37$ cm^2.

7C.2 Determining the Primary and Secondary Turns

Per the design information in the Magnetics Ferrite Core catalog, and based on Faraday's law, we have

$$N_p = \frac{V_{in,min} 10^4}{4BA_e F_{sw}} \tag{7C-3}$$

where N_p = primary turns
$V_{in,min}$ = minimum primary voltage
B = flux density, T
A_e = effective core area, cm^2
F_{sw} = switching frequency, Hz

This assumes a perfect square wave where the duty ratio D is 50%. In our case, the duty ratio will be limited to 0.46 and will occur at minimum input voltage, or 90 Vdc (85 Vrms considering 25% ripple on the bulk capacitor). One can either correct for these in the equation or use another version that expresses the same requirement in terms of the voltage at a given duty ratio.

$$N_p = \frac{V_{in,min} t_{on,max} 10^4}{2BA_e} \tag{7C-4}$$

where $t_{on,max}$ = the maximum duration of the pulse applied to the winding. And, in the denominator, the 4 is replaced by a 2, due to the fact that the square wave actually applied the voltage during one-half of the period, so it was accompanied by another factor of 2.

In this case,

$$t_{on,max} = D_{max} T_{sw} = \frac{D_{max}}{F_{sw}} = \frac{0.46}{65k} = 7.07\,\mu\text{s} \tag{7C-5}$$

Thus,

$$N_p = \frac{90 \times 7.07u \times 10^4}{2 \times 0.045 \times 2.37} = 30\,\text{turns} \tag{7C-6}$$

Now, applying the required turns ratio to determine the secondary turns gives

$$N_{S1} = 0.25 N_p = 0.25 \times 30 = 7.5\,\text{turns} \tag{7C-7}$$

The other secondary winding, the auxiliary winding, must have a turns ratio of 0.2, so the best fit of turns for these two secondaries is 10 turns (power) and 8 turns (auxiliary). We then round off the main secondary turns to 10 turns and recalculate the primary turns:

$$N_p = \frac{10}{0.25} = 40\,\text{turns} \tag{7C-8}$$

And the auxiliary winding will have 8 turns.

$$N_{S2} = 40 \times 0.2 = 8\,\text{turns} \tag{7C-9}$$

7C.3 Choosing the Primary and Secondary Wire Sizes

The wire sizes can now be determined, based on the previously chosen current density of 400 A/cm^2. In the case of the primary, the stated current is 1.8 A rms, so the required wire area will be

$$Aw(pri) = \frac{I_{L_p,rms}}{J} = \frac{1.8}{400} = 0.0045\,\text{cm}^2 = 0.45\,\text{mm}^2 \tag{7C-10}$$

This corresponds closely to a wire size of 21 AWG, which features an area of 0.4181 mm^2.

Fitting the windings into the bobbin usually requires some engineering judgment (and sometimes trial and error), as one would like to avoid fractional layers (they increase the leakage inductance, meaning that they result in poorer coupling and reduced efficiency) and also minimize skin effect by keeping the diameter below one skin depth. In this case, using two conductors of approximately one-half the area is a wise choice. This suggests two conductors of 24 AWG. The final choice will depend on the fit within the bobbin.

Interleaving the primary winding is also advantageous, as it significantly reduces the leakage inductance and also reduces the proximity losses. With this in mind, we will try to split the winding into two layers of one-half the turns, or 40/2 = 20 turns on each layer, with the secondary windings sandwiched in between the two series halves of the primary. With two conductors of no. 24 wire, the width of the 20-turn layer will be (assuming single-layer insulation on the wire) 0.575 mm dia. × 2 × 20, or 23 mm. The bobbin width is 27.43 mm, so this doesn't leave enough margin at the sides for safety regulation requirements. Reducing the wire size to no. 25 is the answer. The reduction in wire size is well justified, because a fractional layer would surely increase the winding losses.

The secondary current is 8 A rms. For a similar current density of 400 A/cm^2, the wire size will be

$$Aw(\text{sec}) = \frac{I_{sec,rms}}{J} = \frac{8}{400} = 0.02\,\text{cm}^2 = 2\,\text{mm}^2 \tag{7C-11}$$

The corresponding wire size is 14 AWG, which has an area of 2.0959 mm^2. To reduce the skin effect and product a thinner layer (and also spread it over a greater portion of the bobbin), we will use two conductors of no. 17 wire, which will have a total area of 2 × 1.0504 mm^2, or 2.1008 mm^2. Since the diameter of single-insulated no. 17 wire is 1.203 mm, the 10 turns of two conductors will occupy a width of 10 × 2 × 1.203, or 24.06 mm. This does not fit well (allowing for safety margins) within the bobbin width of 26.2 mm. Choose two conductors of no. 18 wire, and check later to see that the copper loss is acceptable.

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7C.4 Choosing the Material, Based on the Desired Inductance, or Gapping the Core If Necessary

Based on the calculations detailed in Chap. 7, the desired primary inductance is 320 μH. The desired inductance factor A_L can now be determined:

$$A_L = \frac{L_p}{N^2} = \frac{320u}{40^2} = 200 \text{ nH/turn}^2 \tag{7C-12}$$

The ungapped A_L of the K4022-E060 core (60*u* material) is 194, so no gap is needed.

7C.5 Designs Using Intusoft Magnetic Designer

Intusoft's Magnetic Designer software is a powerful tool for designing transformers and inductors. It allows the designer to quickly arrive at a basic design, then optimize it by providing fast recalculations of losses, leakage inductance, etc., as the designer experiments with variations in the winding structure, core size and shape, and other design choices.

We have entered the design data into the software, as illustrated by the following two screens (Figs. 7C-1 and 7C-2). Note that the predicted temperature rise is 24.16 °C, and the core window is only 33.43% full. This suggests that a smaller core can be used, without exceeding the 40 °C maximum temperature rise. Figure 7C-2 shows the actual winding structure as computed by the software. The EE 42/15 core might be a good choice. It is available in 90*u* material and has an A_L of 217 nH/turn^2. To achieve the required inductance, raise the turns to 48, 12, and 10. (The 10 turns is hopefully close enough to 9.8.)

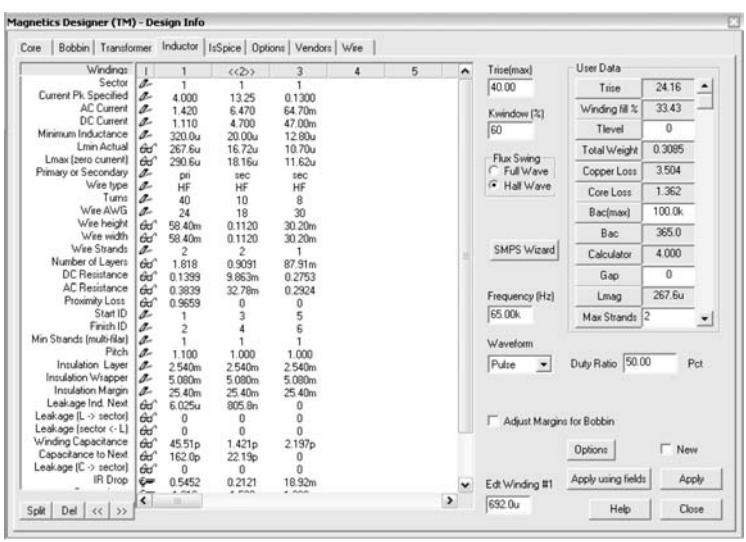

FIGURE 7C-1 Magnetic designer design screen for the present design.

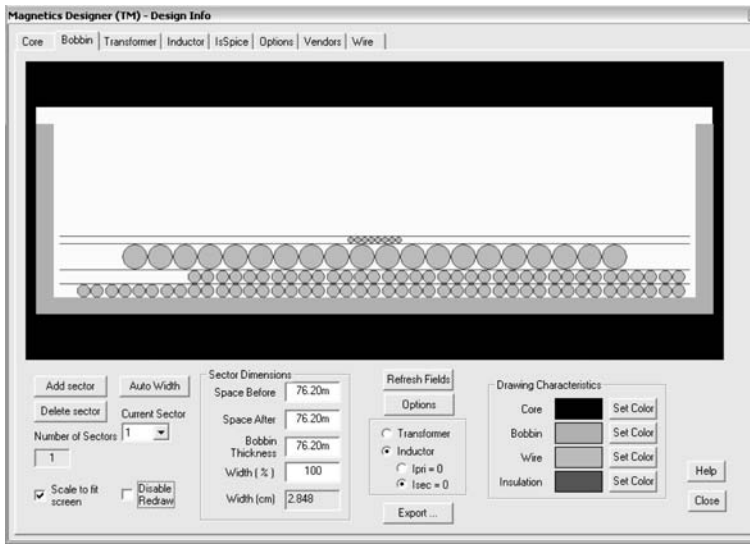

FIGURE 7C-2 The software proposes a winding structure based on the design data.

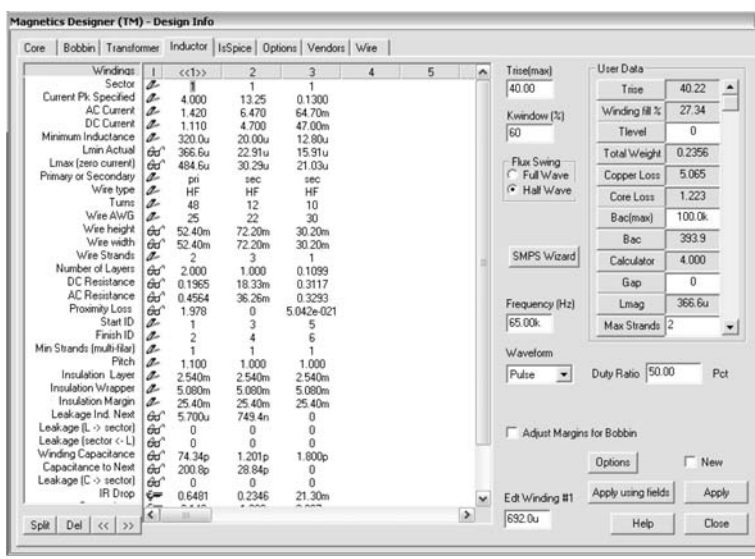

FIGURE 7C-3 Screen shot of design using the EE 42/15 core.

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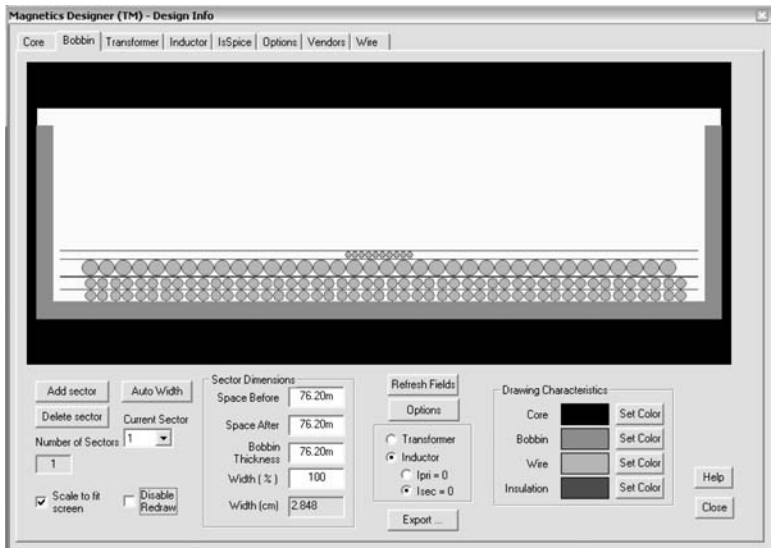

FIGURE 7C-4 Screen shot of the recommended wire arrangement.

Figure 7C-3 shows the design details, with a predicted temperature rise of 40.22 and a fill factor of 27.34%. The bobbin is still not very full, but several attempts led to the conclusion that to fill it further would lead to excessive copper loss. If a higher permeability material were available, a smaller core could be used. The final winding structure is shown in Fig. 7C-4.